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Mira que te mando que te esfuerces y seas valiente; no temas ni desmayes, porque Jehová tu Dios estará contigo en dondequiera que vayas.
Jos 1:9.

Dedicado a mi amada esposa Diana, mi queridos padres Jorge y Martha, mis hermanas Catty y Valeria, mis hermanos, mis tesoros Paula y Victoria, mi familia y todas las personas que aportaron a mi vida durante todo este tiempo. Dios los colme de bendiciones!.

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Rende, novembre 2015 Jorge L. Hernandez Ambato

Abstract

Nowadays electronic applications involve a high density of power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) which represent the major percentage of energy flow to be controlled. Moreover, new technologies, such as Silicon Carbide (SiC), have been well involved in the existing power applications. Therefore, the reliability of power devices is highly demanded.

Since decades, a widely used accelerated test to evaluate the reliability of MOSFETs is the so-called High Temperature Reverse Bias (HTRB). In this stress test, the Devices Under Test (DUTs) are reverse polarized at a certain percentage of the rated breakdown voltage and maintained in this condition at high temperature for a determined long time. A typical HTRB test also incorporates Electrical Characterization Tests (ECTs) of DUTs before and after each stress period, seeking for failed devices. However, time elapsed between ECTs are long and degradation and failure information of DUTs might not be registered.

In this context, an advanced methodology for HTRB test is proposed. The latter consists of applying more stress cycles of short duration together with more frequent ECTs at a relatively high temperature that can be directly compared to that of normal operation in power applications (i. e. 125 °C). With this methodology, more detailed information about degradation trends in electrical parameters, time of failures and stopping of stress test on degrading devices before full breakdown can be performed. The latter can be very useful in R&D stages, where the post-failure analysis of well-degraded devices, but not broken, is important.

An automatized instrumentation, aimed to apply this methodology, has been implemented. The latter utilizes individual Thermal Control Modules (TCMs) to control the test temperature per single DUT. The temperature control is performed through an opposite mini-heater and firmware running on an 8-bit microcontroller. TCMs can be set remotely to apply test temperatures in the range [30-200 °C]. In addition, Switch Matrix Modules (SSMs) are implemented to configure the electrical connections required for HTRB or ECT tests remotely. A PC application controls all the modules through a Master Communication Module (MCM) also implemented. A commercial Source and Measure Unit (SMU) is used for the electrical stress. Full customization of HTRB and

ECTs test parameters can be performed to optimize the stress and degradation data acquisition.

Combining the advanced methodology and instrumentation above mentioned, more stressful conditions can be applied to shorten the overall test time without losing the electrical degradation trends of failing devices. In fact, features of the implemented instrumentation allow for controlling unbeneficial thermal runaway process on the single device, isolating thermal and electric of degraded devices, acquiring frequently electrical parameters data, performing ECTs at a relatively high temperature between shorter stress cycles, managing real-time control of HTRB test. These features are useful to get reliability data in a shorter time than a typical application of HTRB tests while preserving DUTs for post-failure analysis.

The advanced methodology and automatized instrumentation have been applied to Si and SiC power MOSFETs with interesting results, demonstrating to be suitable for both shorter and more accelerated HTRB tests to acquire critical information necessary for the study of degradation processes and reliability in power devices. Moreover, results have demonstrated that degradation trends are not affected when more frequent ECTs at slightly different temperature are performed in the DUTs. In addition, accurate test results have shown that drawbacks of typical HTRB implementation have been solved through the advanced methodology and instrumentation reported.

Complementing the work presented, Low-Frequency Noise Measurements (LFNMs) were also applied as valuable tool to investigate the degradation process in power MOSFETs after stressing them through HTRB test. A correlation between the results from advanced HTRB test and LFNM in power MOSFETs demonstrates that the electrical degradation is represented by a noise spectrum different to that for intrinsic $1/f$ noise.

Riassunto

Le applicazioni elettroniche odierne sono caratterizzate da un'elevata densità di transistori ad effetto di campo di tipo metallo-ossido-semiconduttore (MOSFET) che rappresentano dunque la maggiore sorgente di consumo di energia da gestire. Inoltre, nuove tecnologie, come quella basata sul Silicon Carbide (SiC), sono state impiegate nelle applicazioni ad alta tensione/corrente. L'affidabilità dei dispositivi di potenza è dunque una caratteristica fondamentale.

Da decenni una tipologia di test accelerati largamente impiegata per valutare l'affidabilità dei MOSFET è quella denominata High Temperature Reverse Bias (HTRB). In questi test, i dispositivi da testare sono polarizzati inversamente ad una certa percentuale della tensione di breakdown e mantenuti in queste condizioni ad elevata temperatura per un determinato intervallo di tempo. Tipicamente, prima e dopo ogni ciclo di stress, vengono effettuate delle caratterizzazioni elettriche (Electrical Characterization Tests - ECTs) al fine di valutare eventuali forme di degrado e fallimenti dei dispositivi. Tuttavia, gli ECT sono effettuati ad intervalli di tempo molto lunghi, quindi le informazioni legate ad eventuali forme di degrado e fallimento possono non essere rilevate.

In questo contesto, il lavoro di ricerca si è concentrato principalmente sulla definizione di una metodologia avanzata per la realizzazione dei test HTRB. La procedura proposta consiste nell'applicazione di più cicli di stress a breve durata, intervallati da caratterizzazioni elettriche eseguite a temperature relativamente alte, confrontabili con quelle che si raggiungono normalmente in applicazioni di potenza (cioè, 125°C). Impiegando la metodologia proposta è possibile ottenere informazioni più dettagliate circa l'andamento del degrado dei parametri elettrici ed i tempi di fallimento dei dispositivi. Inoltre, la procedura prevede l'interruzione del test sui dispositivi degradati prima della completa rottura degli stessi. In particolare, quest'ultimo aspetto è rilevante nelle fasi di ricerca e sviluppo, dove l'analisi dei dispositivi danneggiati, ma non totalmente distrutti, consente di ottenere informazioni importanti.

Al fine di applicare la metodologia ideata, è stata sviluppata tutta la strumentazione richiesta. In particolare, questa impiega dei moduli di controllo che consentono di gestire la temperatura dei singoli dispositivi da testare (Thermal Control Module - TCM). Il controllo della temperatura è effettuato attraverso l'uso di adeguati mini-riscaldatori e

di un firmware che è eseguito da un microcontrollore ad 8-bit. Il TCM può essere gestito da remoto in modo da impostare una temperatura di test compresa tra 30 °C e 200 °C. Inoltre, è stato necessario implementare una matrice di switch (Switch Matrix Module - SSM) per poter configurare da remoto le connessioni elettriche richieste durante i test HTRB e gli ECT. Un software dedicato gestisce tutti i moduli attraverso un apposito apparato di comunicazione (Master Communication Module - MCM). Uno strumento di misura commerciale di tipo 'Source and Measure Unit (SMU)' è impiegato per gli stress elettrici. L'apparato implementato consente di scegliere i diversi parametri da impostare durante i test HTRB ed ECT in modo da ottimizzare l'acquisizione dei dati.

Impiegando la metodologia proposta insieme alla strumentazione implementata è dunque possibile applicare condizioni di stress più intense riducendo, contemporaneamente, il tempo totale della misura, senza tuttavia perdere informazioni importanti sull'andamento del degrado dei dispositivi. Infatti, le caratteristiche della strumentazione implementata consentono di controllare eventuali processi di deriva termica dei singoli dispositivi, di isolare i dispositivi degradati, di acquisire frequentemente dati sui parametri elettrici eseguendo gli ECT a temperature relativamente elevate ad intervalli di tempo brevi, di gestire in real-time il controllo dei test HTRB. Queste caratteristiche sono utili per ottenere dati di affidabilità in un tempo più breve rispetto alle applicazione dei tipici test HTRB, permettendo inoltre di eseguire analisi successive ad i fenomeni di degrado.

La procedura descritta è stata applicata a dispositivi MOSFET realizzati in silicio ed in SiC ottenendo risultati interessanti e dimostrando, al contempo, che la metodologia ideata è adatta per l'esecuzione di test HTRB più brevi e più accelerati, in modo da acquisire informazioni necessarie per l'analisi dei processi di degrado e dell'affidabilità dei dispositivi di potenza. Inoltre, i risultati sperimentali hanno dimostrato che l'esecuzione più frequente di ECT a temperature leggermente diverse non impattano sugli andamenti di degrado dei dispositivi. Inoltre, la metodologia implementata consente di risolvere i principali svantaggi legati alle procedure standard di test HTRB.

In aggiunta a questo, il presente lavoro riporta l'applicazione di misure di rumore a bassa frequenza come utile strumento per investigare ed individuare i meccanismi di fallimento indotti dai test HTRB sui dispositivi MOSFET di potenza. Le misure effettuate dimostrano l'esistenza di una correlazione tra lo spettro di rumore dei dispositivi sottoposti a stress ed i relativi test HTRB: in particolare, i risultati ottenuti mostrano che lo spettro di rumore differisce da quello intrinseco rappresentato dal rumore 1/f.

Pubblication List

Conference contributions

1. C. Pace, **J. Hernandez-Ambato**, and C. Giordano, "A Novel Instrumentation for an Advanced High Temperature Reverse Bias (HTRB) Testing on Power Transistors," Applications in Electronics Pervading Industry, Environment and Society (APPLEPIES), 2014. (*in edition*)

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3. G. Consentino, D. De Pasquale, S. Galiano, A. D. Ignoti, C. Pace, **J. Hernandez-Ambato**, M. Mazzeo, and C. Giordano, "Innovative Instrumentation for HTRB Tests on Semiconductor Power Devices," in AEIT Annual Conference, 2013, pp. 1–5, doi: 10.1109/ AEIT.2013.6666814.

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Journal papers

1. C. Pace, **J. Hernandez-Ambato**, D. De Pasquale, and G. Consentino, "Instrumentation for Innovative Semiconductor Power Devices Reliability Tests," Int. J. Eng. Ind., vol. 4, no. 2, pp. 119–127, 2013, doi: 10.4156/ijei.vol4.issue2.14.

Acronyms

ADC Analog to Digital Converter

ADT Accelerated Degradation Testing

AEC Automotive Electronics Council

ALT Accelerated Life Test

CNP Charge Neutrality Point

COTS Commercial On The Shelf

DFT Discrete Fourier Transform

DMOSFET Double Diffused MOSFET

DUT Device Under Test

ECT Electric Characterization Test

EECT Emergency Electric Characterization Test

EVT Electric Verification Test

FIT Failures In Time

GPIB General Purpose Interface Bus

GUI Graphical User Interface

HALT Highly Accelerated Life Testing

HASS Highly Accelerated Stress Screening

HTRB High Temperature Reverse Bias

HTGB High Temperature Gate Bias

HTS High Temperature Storage Life

H3TRB High Humidity High Temperature Reverse Bias

IDE Inter-Digitated Electrode

IEC International Electrotechnical Commission

IGBT Insulated Gate Bipolar Transistor

I^{2}C Inter-Integrated Circuit

JEDEC Joint Electron Device Engineering Council

LFN Low-Frequency Noise

LFNM Low-Frequency Noise Measurement

LPEG Liquid-Phase Exfoliated Graphene

LTS Low Temperature Storage Life

MCM Master Communication Module

MIL-DoD Military Department of Defense of United States

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MS Mechanical Shock

MTTF Mean Time To Failure

MTBF Mean Time Between Failure

NI National Instruments

PC Power Cycling

PCB Printed Circuit Board

PWM Pulse Width Modulation

PID Proportional Integrative Derivative

PSD Power Spectral Density

RAT Reliability Acceptance Test

R&D Research and Development

RDT Reliability Demonstration Test

RTS Random-Telegraph-Signal

SAFeFET Surface Added Feature Field Effect Transistor

SCPI Standard Commands for Programmable Instrumentation

SEM Scanning Electron Microscopy

SMD Surface Mounting Device

SMM Switch Matrix Module

SMU Source and Measuring Unit

TAT Thermal Adjustment Tool

TC Temperature Cycling

TCM Temperature Control Module

TST Thermal Shock Test

UART Universal Asynchronous Receiver-Transmitter

USB Universal Serial Bus

VDMOS Vertical Diffused MOS

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Introduction

In whichever nowadays application, semiconductor devices are more and more present. In particular, in applications where a big density of energy must be handled, power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) constitute the energy flow control. Power MOSFETs are widely used in high voltage/current applications such as DC-AC inverters, DC-DC converters, automotive, aerospace, industrial and consumer electronics among others. In general, the reliability of power devices is evaluated through accelerated stress test. Reliability in semiconductors is defined as the capacity (probability) of a device to work continuously under predetermined operation conditions within a determined period without failures.

With a well spread of applications where power MOSFETs are involved, and in some cases with critical roles, high-reliability requirements of such devices is continuously demanded. In fact, some decade ago, the reliability of a power MOSFET used to be evaluated at 150 °C, but nowadays, the customer requires higher stress factors using 175 °C to assess the power MOSFETs for the automotive field. Even more, emergent technologies, such as Silicon Carbide SiC and Gallium Nitride requires even more stress factors (i. e. 200 °C).

Since decades, the so-called High Temperature Reverse Bias (HTRB) has been used as an accelerated test. In this kind of test, the Devices Under Test (DUT) are reverse polarized at a maximum percentage of the rated breakdown voltage and maintained in this condition at high temperature for a determined time. Thus, an accelerated test is designed to evaluate the reliability of semiconductor devices making them work under worsened operation conditions than normally specified ones during a predefined period. Also, Electrical Characterization Tests (ECTs) of DUTs shall be performed each period of stress seeking for any signal of electrical degradation or even worse for burned devices. In both cases, a DUT failure is defined. According to the methodology and standard adopted for the accelerated test, the failures and time failures are quantified, and the test continues. Instead, if failures are not accepted, the test is stopped and started again with another lot. The first approach is usually used for lifetime prediction on semiconductor devices while the second one is referred to qualification products.

Relating to standards for HTRB test, procedures and methodologies are not clear

and, in some cases, even ambiguous. Thus, usually each manufacturer uses its guideline to perform reliability and qualification tests. Therefore, a direct comparison of reliability data between manufacturers is even more difficult. In fact, some drawbacks related to the typical (and even empirical) application of HTRB can be listed as usual manual operation during the ECTs campaigns, uncertainties of the failure right time because of the not so frequent ECTs campaigns, general control of temperature instead of individual DUT one among others.

Thus, in this work, a brief revision of physical aspects for defining electrical parameters on power MOSFETs that are characterized during the ECTs campaigns is performed. An analysis of the standards regulation of HTRB test is performed, highlighting the ambiguities and drawbacks of such technical reports. An advanced methodology, together with an automatized instrumentation that seeks for improve the practice of HTRB on power MOSFETs is proposed. Furthermore, several experiments to evaluate the efficiency and performance of such a methodology and instrumentation were carried out, and the main results are reported.

Furthermore, a revision of concepts regarding the internal noise sources in electronic devices is performed. In particular, the Low-Frequency Noise (LFN) is presented as a valuable diagnostic tool to investigate the defectiveness inside the micro and nano structures of the semiconductor devices. Experimental measurements of noise inside power MOSFETs and emergent 2D-materials are presented. Experimental investigation on the correlation between HTRB test to accelerate failure mechanisms in power MOSFET devices and LFN measurement as a tool to individuate such a failure mechanisms is also presented.

Chapter 1

Power Semiconductor Devices

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During the last 30 years, the even more diffusion of enhanced power semiconductor devices in Silicon (Si) and Wide Band Gap (WBG) materials, such as a Silicon Carbide (SiC) and Gallium Nitride (GaN), have made up the plateau on which rest the nowadays medium and high voltage-current rated applications (i.e. automotive, power conversion, etc.) [1]–[6]. Obviously, this could not be possible without the continuous efforts oriented to Research and Development (R&D) in materials, structures and devices, which have improved performances in power electronic applications. In this way, the adoption of power devices, such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistor (IGBT), in several application areas has been classified according to either voltage or current application requirements (see Figure 1.1) [1], [6].

In fact, the first category involves applications that require low operating current (typically less than 1 A) levels. Usually in this category, applications require a large

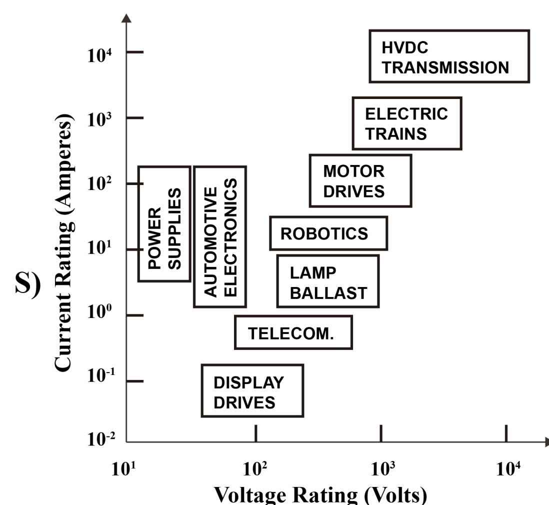


Figure 1.1: Classification for power devices according to voltage and current ratings.

number of transistors that must be capable of blocking up to 300V, such as display drivers. At the same time, the small size of these transistors (due to low current capabilities) allows their integration on a single chip with control circuits to provide a cost effective solution. On the other hand, the second category is applications with relatively small operating voltage (<100 V) and high current densities, such as automotive electronics and computer power supplies. Others characteristics of these category devices are low on-resistance and fast switching frequencies that are implemented by normal silicon (Si) power MOSFETs. Last third category is reserved for high operating voltages (above 200V), where current could also be considerable. In this category, on-resistance of conventional silicon technology is too large. Consequently, power devices have adopted new architectures and manufacturing process that have improved MOSFETs devices to work with several hundreds of volts [2], [7].

In the last decades, new materials, such as Silicon Carbide (SiC) or Gallium Nitride (GaN), have been also studied for implementations of power semiconductors due to their wider energy bandgap of 3.2eV and 3.4eV, respectively [8], compared to the 1.1eV of the Si [8]. These last advances have improved modern power devices to support several thousands of volts (around 5kV) [3]. In fact, more mature manufacturing processes settle the SiC technology as the next generation of power devices to work under extreme conditions where Si has intrinsic limits. First commercial SiC devices have been available since a couple of years but the reduced wafer size (initiated with 3”) governed the high prices of such products. However, it is expected that SiC devices commercialization prices can continue to decrease making possible the substitution of Si in most of the power application [6].

In this chapter the technology of power semiconductor MOSFETs will be discussed: a focus on the basic concepts for the design of power devices will be provided. Specifically,

this chapter will focus on silicon and silicon carbide technologies which represent the most mature semicondutor processes for power devices fabrication. Moreover the electrical characteristics of power MOSFETs will be discussed and some simulations results will be reported in order to clearly define useful parameters to be experimentally measured. Furthermore, conceptualization of internal noise sources in semiconductor devices will be also defined. Such low-frequency noise characterization on power MOSFETs will be presented as a diagnosis tool for reliability purposes [9], [10].

1.1 Electronic Properties of Si and SiC

1.1.1 Carrier Mobility Parameter

Mobility (μ) is an important property of semiconductor materials to be considered during the design of semiconductor devices. Electrons and holes can be seen essentially as free particles (or carriers) inside a semiconductor, whose movement is regulated by scattering mechanisms with vibrating lattice atoms, impurity ions and other scattering centers caused by external agents as electric and magnetic fields, temperature among others [11]. Moreover, mobility also depends on the structure of devices. In fact, a detailed explanation of MOSFET mobility is reported in [12].

Therefore, even if μ is an intrinsic property of semiconductors, its definition and modeling vary according to each scattering phenomenon, carrier transport mode (bulk or surface) and application. However, a net mobility μ can be defined through the Matthiessen's rule as a parallel combination of various mobilities, in which the lowest mobility dominates [13].

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \dots \tag{1.1}$$

Different mobilities are defined in literature [11]–[14]. In this work, only two mobilities are reviewed because of their direct impact on conductivity and maximum current densities of semiconductor material.

Conductive Mobility

Mobility describes how the carriers move in their respective bands inside a semiconductor, and therefore in power devices. Mobility is well related to the conductivity (σ) of a semiconductor through the expression:

$$\sigma = q(\mu_n n + \mu_p p) \tag{1.2}$$

where, n and p are the electron and hole densities of the material, together with their carrier mobilities $\mu_{n,p}$, respectively.

Electric-Field Mobility

As mentioned above, mobility is the definition of how the carriers move inside a semiconductor material. Such movement is related to a velocity. In the absence of an external electric field (E), carriers move with thermal velocities (v_{th}), whose relative *mean value* is *zero* for electron and hole carriers. However, when an electric field (E) is applied, carriers are accelerated between collisions due to the experienced force $\mp qE$ [11], [15]. Due to this acceleration of thermal velocities, the final relative *mean values* v_n and v_p are *non-zero* for electron and hole carriers velocities, respectively. These resulted velocities are called *drift velocities*. For low fields, the electric field mobility can be expressed by

$$\mu_{n,p} = \mp \frac{v_{n,p}}{E}. \tag{1.3}$$

The importance of these mobilities is related with the electron current density (j_n) and hole current density (j_p) as function of an electric field, expressed as:

$$j_n = -q \cdot n \cdot v_n = q \cdot \mu_n \cdot n \cdot E \tag{1.4}$$

$$j_p = q \cdot p \cdot v_p = q \cdot \mu_p \cdot p \cdot E. \tag{1.5}$$

Composition of both current densities results in the total current density $j = j_n + j_p$, also expressed as:

$$j = q \cdot (\mu_n \cdot n + \mu_p \cdot p) \cdot E = \sigma \cdot E = \frac{E}{\rho}. \tag{1.6}$$

It is worth noting that carriers mobility of a semiconductor material determines the ohmic voltage drop $V = \rho j \Delta x$ for a given current density and hence the power loss density ($j \cdot V$) and heating generation. Hence, mobility determines the maximum allowed current density in devices [11]. A collection of carrier mobilities values, obtained by measurements and/or simulations from different works are reported in Table 1.1 for Si and SiC.

As presented in Table 1.1, mobilities values for electron and holes in Si are higher than those for SiC. However, mobility is not the unique to be taken into account to select a material for the power devices construction. Further properties, such as bandgap energy, thermal conductivity, critical electric field among others, must be necessarily considered for the high performance of semiconductor materials inside power devices as shown in Figure 1.2 [8].

1.1.2 Impact Ionization

In power applications, semiconductor devices clamp hundreds of volts in their off-states with minimal leakage currents up to the safe operating voltage limits. Those voltage limits are dictated by the device breakdown, which is mainly determined by the impact ionization and its avalanche multiplication effect [4]. Theoretically, this effect settles the breakdown voltage property being always present a leakage current that is

Table 1.1: Collection of mobilities reported in literature.

Work	μ_n [cm^2/V.s]	μ_p [cm^2/V.s]	Technology
Lutz et al. [11]	1420	470	Si
Linewih et al. [13]	1417	—	Si
Freda Albanese [16]	1500	480	Si
Thomas [17]	1330	495	Si
Lutz et al. [11]	1000	115	4H-SiC
Linewih et al. [13]	950	—	4H-SiC
Freda Albanese [16]	720	120	4H-SiC
Perez-Tomas et al. [15]	950	—	4H-SiC

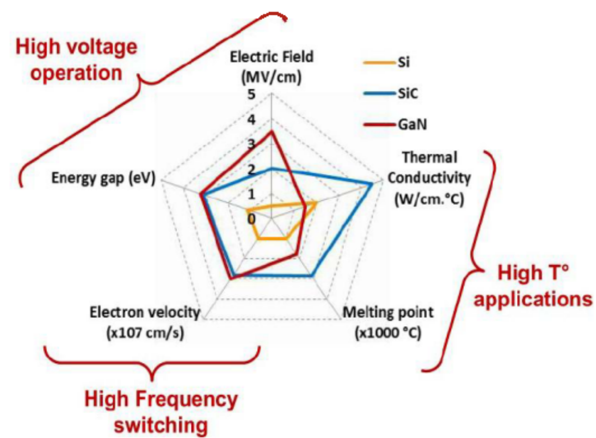


Figure 1.2: Application fields of WBG materials (SiC and GaN) vs Si [8].

Table 1.2: Coefficients for impact ionization rate calculation reported in literature.

Work	a_n $(x10^6 cm^{-1})$	b_n $(x10^7 V.cm^{-1})$	a_p $(x10^6 cm^{-1})$	b_p $(x10^7 V.cm^{-1})$	Technology
Lee et al. [19]	3.80	0.177	9.90	0.298	Si
Ogawa [20]	0.75	0.139	4.65	0.23	Si
Van Overstraeten et al. [21]	0.703	0.1231	1.582	0.2036	Si
Lutz et al. [11]	1.10	0.146	2.10	0.220	Si
Baliga [1]	0.7	0.123	1.6	0.2	Si
Akturk et al. Model 2 [4]	1.98	0.946	4.38	1.14	4H-SiC
Akturk et al. Model 3 [4]	2.5	1.84	3.25	1.71	4H-SiC
Raghunathan et al. [22]	—	—	3.25	1.71	4H-SiC
Baliga [1]	—	—	6.46	1.75	4H-SiC
Ayalew et al. [14]	3.44	2.58	3.5	1.7	4H-SiC

dominated by quantum mechanical tunneling of carriers. Impact ionization rates for electron or hole (α_n and α_p, respectively) are defined as the number of electron–hole pairs created by an electron or a hole traversing 1 cm through the depletion layer along the direction of the electric field [1]. Such electron and hole ionization rates are related to the semiconductor material, and they are dictated by Chynoweth's Law [18]:

$$\alpha = a \cdot exp(-\frac{b}{E}), \tag{1.7}$$

where, a and b are the impact ionization coefficients extracted from the exponential fitting with experimental data.

So, the corresponding avalanche generation rate can be expressed as

$$G_{ava} = \frac{1}{q}(\alpha_n j_n + \alpha_p j_p). \tag{1.8}$$

Due to impact ionization coefficients a and b are different for electrons and holes, and they depend on the semiconductor material, the results of some experimental measurements oriented to determine such coefficients have been summarized in Table 1.2 for Si and 4H-SiC.

In Figure 1.3, results of numerical simulation of impact ionization rates for Si and 4H-SiC are presented. Such simulations were performed using the coefficients reported by Lutz et al. [11] and Akturk et al. Model 3 [4], respectively. Impact ionization rate for electron and holes were calculated using the form of equation 1.7 as:

$$\alpha_n = a_n \cdot exp(-\frac{b_n}{E}) \tag{1.9}$$

$$\alpha_p = a_p \cdot exp(-\frac{b_p}{E}). \tag{1.10}$$

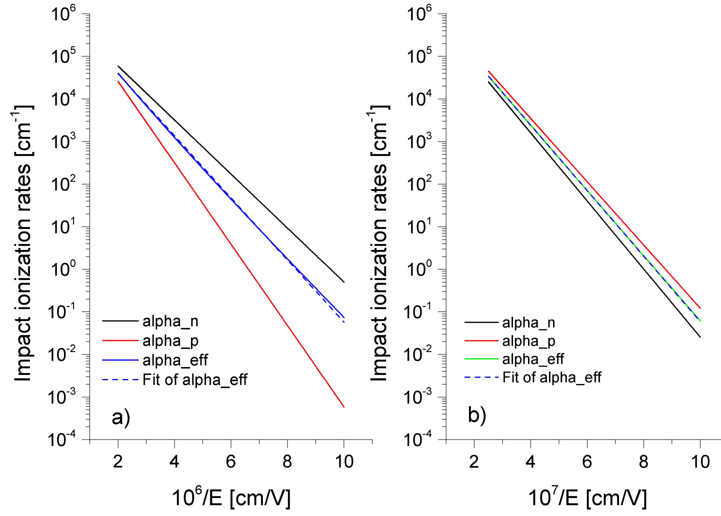


Figure 1.3: Numerical simulation of impact ionization rates for electron (black lines) and holes (red lines) in a) Si and b) 4H-SiC. Effective ionization rates (blue lines) are also presented. Electric Field is ranging in 0.1-0.5 $MV.cm^{-1}$ and 1-4 $MV.cm^{-1}$ for Si and 4H-SiC, respectively.

Table 1.3: Effective coefficients for breakdown calculation of Si and 4H-SiC, extracted by fitting from effective impact ionization rate numerical simulation.

Technology	a_{eff} $(x10^6 cm^{-1})$	b_{eff} $(x10^6 V.cm^{-1})$	E $[MV.cm^{-1}]$ for $\alpha_{eff} \approx 100cm^{-1}$
Si	1.13478	1.68	0.18
4H-SiC	2.8412	17.68	1.72

Furthermore, effective ionization rate (α_{eff}) determines directly the breakdown voltage of a pn-junction. According to [20], α_{eff} can be obtained from the following relation:

$$\alpha_{eff} = \frac{\alpha_n - \alpha_p}{ln(\frac{\alpha_n}{\alpha_p})} \tag{1.11}$$

which is also shown in Figure 1.3 for Si and 4H-SiC. It is worth noting that effective coefficients a_{eff} and b_{eff}, necessary for breakdown calculation, can be extracted by exponential fitting obtaining the results summarized in Table 1.3. Such results will be used in the following sections.

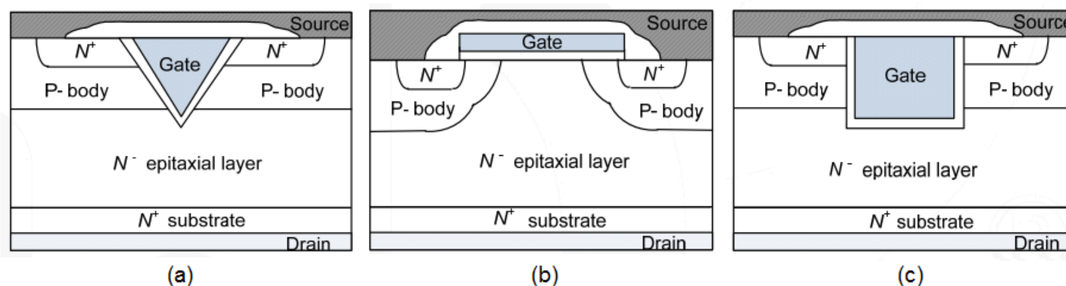


Figure 1.4: Types of vertical structures for modern enhanced power MOSFET [23].

1.2 Structure of a Power MOSFET

A MOSFET can be seen as a two-terminal switch, which are named "Drain" and "Source", where the electric current that flows between such terminals is controlled by an electric field, which is generated by the voltage applied to a third terminal called "Gate." This last terminal is separated from the semiconductor substrate by an oxide layer acting as the insulator.

First power MOSFET devices were designed in lateral structures, with the drain, source and gate terminals placed on the semiconductor surface. These lateral designs facilitate the integration of devices, but the power rating was limited because the drain-source distance must be large for higher blocking voltage capabilities [23].

However, modern vertical structures enabled for enhanced power MOSFETs with higher blocking voltage capabilities (initially ranging in $10^2 - 10^3$ V) by growing the epitaxial layer (drift region), placing the drain and source terminals on the opposite faces of the semiconductor substrate. In this way, more surface for drain and source terminals also enabled higher current densities. The first vertical structures, presented in Figure 1.4, are summarized in [23] as:

a) VMOSFET designed with a V-groove at the gate region. VMOSFET presented stability problems in manufacturing and a high electric field at the tip of the gate.

b) DMOSFET design has a double-diffusion structure with a P-base region and a N+ source region, forming the n-Channel. This structure is wider used successfully for power MOSFET since the 1970s. Some variations of this structure have improved even more the ratings of power MOSFETs [11], [24].

c) UMOSFET design has a U-groove at the gate region. Higher channel density reduces the on-resistance as compared to the VMOSFETs and the DMOSFETs. However, it presents problems with the high electric field again at the corners of the U-groove.

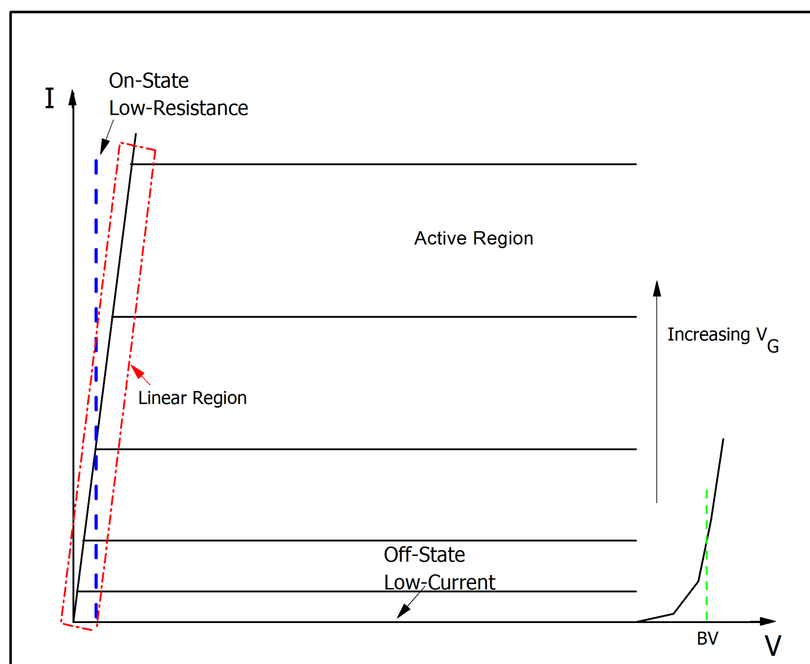


Figure 1.5: Analytical trans-characteristic curves of a typical enhanced n-channel MOSFET transistor.

1.3 Electric Characteristics of Power MOSFET

Theoretically, an ideal MOSFET is characterized by blocking infinity reverse voltage in off-state condition (when the gate voltage is lower that threshold voltage, $V_{GS} < V_{th}$) without presence of leakage currents, and it conducts infinity current flow under on-state condition (when $V_{GS} > V_{th}$) without power losses due to internal zero on-resistance. However, as shown in Figure 1.5, a physically enhanced n-Channel MOSFET presents different properties, which carry it to work in Ohmic Region, Cutt-Off or Blocking Region, and Saturation or Active Region depending on the bias conditions.

As mentioned before, when $V_{GS} < V_{th}$, the MOSFET is in blocking mode. Hence, a reverse V_{DS} can be held while a I_{DSS} is forced due to the effect of the thermal energy on the Fermi-Dirac distribution of electron energies and bias level applied. In fact, the leakage current is temperature dependent, as it will be treated below, and it arises as temperature increments too. This operation mode is held while the reverse voltage applied does not arise over certain value called BV_{DSS}. After such voltage, the leakage current increments in an uncontrolled way, which causes a positive feedback by self-heating effect and the subsequent failure of the device.

On the other hand, when $V_{GS} > V_{th}$, inversion of states is performed, and the current flow can also be modulated depending on the drain-source potential. In fact,

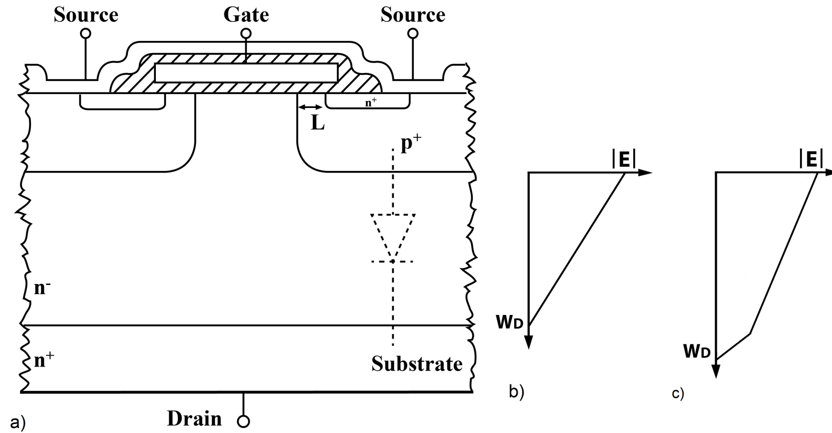


Figure 1.6: a) DMOSFET cell structure of a Power n-MOSFET (PiN diode is purposely highlighted). b) Triangular shape distribution of Electric Field (E) named Non-Punch-Through (NPT). c) Trapezoidal shape distribution of of the space charge named Punch-Through (PT).

the operation mode under this condition depends on the V_{DS} polarization. In this way, when $V_{DS} < (V_{GS} - V_{th})$, the device is working in the ohmic region and the drain current (I_D) rises linearly with V_{DS}. When $V_{DS} > (V_{GS} - V_{th})$, the MOSFET entries in the active or saturation region and the current slightly increases with V_{DS} but essentially it is limited by the on-resistance parameter.

It is worth mentioning that figures of merit of power MOSFETs are: off-state blocking voltage, off-state leakage currents, on-state resistance and threshold voltage. These constitute the main electrical parameters of power MOSFETs, which are discussed in the following sections considering the DMOSFET structure, which is again reported in Figure 1.6a.

Moreover, results of numerical simulations, performed on the electrical characteristic parameters above mentioned, are also presented. The methodology for such calculations consisted of using script writing on MATLAB of the equations defined in the next sections together to specific coefficients and constants collected from literature. Sweep of different variables was used such as doping concentrations, thickness substrates, electric fields, voltages among others.

1.3.1 Breakdown Voltage Parameter

One parameter that is associated with the capability of blocking voltage for MOSFET devices is the Breakdown Voltage (BV). It is the maximum reverse voltage (in off-state condition) that can be applied to the power MOSFET, without over-biasing the device dangerously. The BV is related to the critical Electric Field (E_C) generated at the p-n junction that could lead to impact ionization and avalanche multiplication.

In the DMOSFET structure, the blocking voltage is improved by the slightly doped

n^- (drift region) diffused material, which supports the Electric Field (E) generated by the potential V_{DS} applied. In fact, E is distributed along the width of the drift-region (w_D) forming a space charge. If w_D is large enough to avoid that the space charge reaches the n^+ region (close to drain terminal) forming a triangular shape (see Figure 1.6b), it is called *non-punch-through* (NPT) dimensioning. Otherwise, if the space charge reaches the n^+ region forming a trapezoidal shape distribution (see Figure 1.6c), it is called *punch-trough* (PT) dimensioning [11], [25]. At the same time, a p^+ diffused region avoids that carriers flow from the n^+ diffused region close to the source terminal toward the drift region (drain) under off-state condition. When this design and bias conditions are guaranteed, intrinsic PiN-diode into de DMOSFET structure is reverse biased. As aforementioned, the blocking voltage property is limited by the maximum E_C at breakdown avalanche that drift region can hold, which can be determined as

$$E_C = (\frac{n+1}{B \cdot w_D})^{\frac{1}{n}} = (\frac{q \cdot (n+1) \cdot N_D}{B \cdot \varepsilon})^{\frac{1}{n+1}} \tag{1.12}$$

where, w_D is the drift region length, N_D is the donor doping density, q is electron charge and ε is the dielectric constant of material [11]. Following [26], n and B are defined by 1.13 and 1.14, respectively, where E_0 is the initial electric field in the drift region, which is assumed to be around $2.4 \times 10^5\ V/cm$ and $2.4 \times 10^6\ V/cm$ for Si and SiC, respectively. The b_{eff} and a_{eff} coefficients related to the effective ionization rates are extracted from Table 1.3.

$$n = \frac{b_{eff}}{E_0} \tag{1.13}$$

$$B = \frac{a_{eff}}{{E_0}^n \cdot exp(n)} \tag{1.14}$$

Following [27], most literature about Si defines values for E_0 in the range of 0.2-0.3 MV/cm at 300K. On the other hand, SiC usually describes one order of magnitude more, in most of the electric parameters, than those for Si. In fact, the E_0 value for SiC usually ranges between 2-3 MV/cm [28].

Having in mind Figure 1.6b, the integration of electric field distributed along drift region (w_D) gives the breakdown voltage as

$$BV = \int_0^{w_D} E dx = \frac{1}{2} w E_C. \tag{1.15}$$

Substituting 1.12 into 1.15, breakdown voltage could be expressed in function of the drift-region width or the doping density by equations 1.16 and 1.17, respectively.

$$BV = \frac{1}{2}(\frac{n+1}{B} \cdot w^{n-1})^{\frac{1}{n}} \tag{1.16}$$

$$BV = \frac{1}{2}(\frac{n+1}{B})^{\frac{2}{n+1}} \cdot (\frac{\varepsilon}{q \cdot N_D})^{\frac{n-1}{n+1}} \tag{1.17}$$

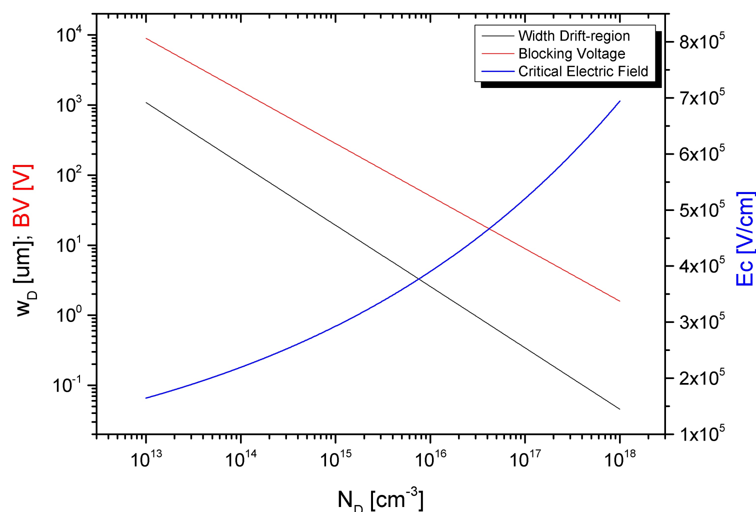


Figure 1.7: Critical electric field strength (E_C), breakdown voltage (BV) and depletion width (w_D) at breakdown as function of doping density N_D for p$^+$n-junction in Si at 300K.

According to [11], the width of the drift-region, w_D as function of N_D for a given breakdown voltage is expressed as:

$$w_D = (\frac{n+1}{B})^{\frac{1}{n+1}} \cdot (\frac{\varepsilon}{q \cdot N_D})^{\frac{n}{n+1}}. \tag{1.18}$$

Thus, unique independent variable to define critical electric field E_C, breakdown voltage BV and width drift-region w_D, is the donor doping density N_D defined in equations 1.12, 1.17 and 1.18, respectively. Results of numerical calculation of these parameters are displayed in Figures 1.7 and 1.8 for Si and SiC, respectively.

At a first glance in the Figures 1.7 and 1.8, the drift-region width w_D is reduced for higher doping concentration as well as the breakdown voltage and viceversa. At the same time, due to the w_D is reduced, the critical electric field E_C is high due to the reduction of the space charge (see eq. 1.12). This means that to clamp higher BV, it is necessary designing devices with higher w_D which is reached through lower N_D, and by consequences lower $E - C$ can be guaranteed. However, as it will be see in the next sections, higher values of w_D is not favourable for the on-resistance parameter.

With the aim of making up a comparison between Si and SiC technologies, a case of study is presented according to Figure 1.7 and 1.8. To reach BV=1 kV in a Si device with w_D=85 μm, it is necessary a doping concentration in the drift region N_D=1.83 $\times 10^{14}$ cm$^-$3. While, to reach the same BV in a SiC device, it is necessary a higher doping concentration of N_D=2.65 $\times 10^{16}$ cm^{-3} but resulting in a thinner w_D= 6.37 μm, and consequently the SiC device will have a less on-resistance than Si for the same breakdown voltage. It is also worth noting that critical electric field E_C for SiC is more

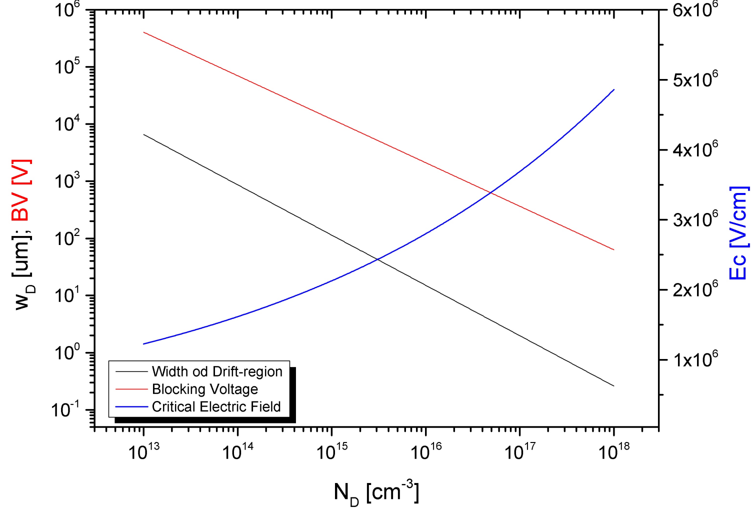


Figure 1.8: Critical electric field strength (E_C), breakdown voltage (BV) and depletion width (w_D) at breakdown as function of doping density N_D for p$^+$n-junction in SiC at 300K.

Table 1.4: Typical E_C values for some semiconductors materials [11].

Material	E_C (V/cm)
Si	2×10^5
GaAs	4×10^5
4H-SiC	$> 2 \times 10^6$
GaN	$> 3 \times 10^6$
C	$> 1 \times 10^7$

than one order of magnitude than that for Si device, which is advantageous to hold high voltages with thinner drift-regions.

Conceptualizations reviewed in this section could also be applied to other semiconductor materials, in particular for those with wider bandgap energy than Si. In fact, due to the higher energy involved in passing an electron from valence to conduction band, higher critical electric fields E_C are registered in Table 1.4.

Numerical analysis performed above was well applied at room temperature (300K) but in real applications these estimations are not guaranteed, and normal operation of power devices could be compromised. In fact, temperature dependence of both “n” and “B” parameters are defined in [11] as

$$n(T) = \frac{b_{eff} + 1100 * (T - 300)}{E_0}, \tag{1.19}$$

$$B(T) = \frac{a_{eff}}{E_0^{n(T)} \cdot exp(n(T))}. \tag{1.20}$$

Substituting 1.19 and 1.20 in equation 1.17, with predefined E_0 and N_D values, breakdown voltage results purely temperature dependent. Therefore, minimum and maximum operation temperature should be considered for application of power devices, having in mind that lower temperatures decrease the breakdown voltage and vice-versa.

1.3.2 Drain Leakage Current Parameter

The main contribution for the Drain Leakage Current (I_{DSS}), in the vertical power MOSFET cell structure of the Figure 1.6a, is related to the p^+n-junction (source-drain terminals) polarized under reverse bias (blocking current mode). It is well known that when a reverse voltage is applied on a pn-junction, it generates a space charge at the junction and the related increase of the depletion zone. Under this condition, factors like voltage level and temperature are well related to the generation of carriers that enhance the proliferation of reverse current density (j_r), which, at its time, is the result of the diffusion current density (j_s) and space charge current density (j_{sc}) expressed as:

$$j_r = j_s + j_{sc} = q(\frac{n_i^2}{N_D} \cdot \frac{L_p}{\tau_p} + \frac{n_i}{\tau_g} \cdot w_{sc}) \tag{1.21}$$

with

$$w_{sc} = \sqrt{\frac{2\varepsilon}{q} \cdot (\frac{N_A + N_D}{N_A.N_D}) \cdot (V_{bi} + V_r)} \tag{1.22}$$

$$V_{bi} = \frac{kT}{q} \cdot ln(\frac{N_A.N_D}{n_i^2}) \tag{1.23}$$

where, n_i is the intrinsic concentration ($n_i = \sqrt{n.p}$), N_D and N_A are the donors and acceptors carriers density of the n and p^+ regions, respectively; $L_p = \sqrt{D_p.\tau_p}$ is the hole diffusion length with D_p ascribed as the diffusion constant of holes, τ_p and τ_g are the hole carrier lifetime and the carrier generation lifetime, respectively. On the other hand, w_{sc} is the space charge width in function of acceptors and donors carriers densities, built-in voltage V_{bi}, which is related to the device design [1], and the reverse voltage V_r applied to the junction. It is worth noting in equation 1.21, j_s increases faster than j_{sc} in terms of n_i, even when j_r is voltage dependent via the w_{sc} expression introduced. Also, the τ_g is important to determine which current will dominate the total reverse current flow. For example, for cases where $\tau_g \approx \tau_p$ and $L_p \approx w_{sc}$, the space charge current j_{sc} dominates the reverse current. Furthermore, τ_p and τ_g can be obtained from the Shockley-Read-Hall model [29], [30], written as:

$$\tau_g = n_i \cdot (\frac{\tau_{n0}}{n_r} + \frac{\tau_{p0}}{p_r}) \tag{1.24}$$

$$\tau_p = \tau_{p0} + \frac{\tau_{p0}.n_r + \tau_{n0}.p_r}{N_D} \tag{1.25}$$

where, τ_{n0} and τ_{p0} are the minority carrier lifetime for electrons and holes, respectively; n_r and p_r are the carrier concentration assuming the Fermi level E_F equal to the recombination level E_r [2]. If E_r is equal to the intrinsic energy E_i, it results in $n_r = p_r = n_i$ and equation 1.24 is reduced to $\tau_g = \tau_{n0} + \tau_{p0}$ which leads to the minimum value for the generation lifetime. In fact, from [2] an approximation based on [29]–[31] establishes that τ_{n0} and τ_{p0} are determined by

$$\tau_{n0} = \frac{1}{N_r c_n} \quad (1.26)$$

$$\tau_{p0} = \frac{1}{N_r c_p} \quad (1.27)$$

resulting in ranges between 0.5 and 100 μs for a total concentration centers N_r of only 10^{13} cm^{-3} with capture coefficients $c_{n,p}$ in the range of 1×10^{-9} to 2×10^{-7} $\text{cm}^{-3}s^{-1}$ at 300K. In this way, typical value for τ_g is 100 μs assuming mean values for τ_{n0} and τ_{p0} in the case where $n_r = p_r = n_i$.

In Figure 1.9, the results from a numerical simulation of the leakage current in reverse polarization are presented for Si and SiC n-MOSFETs, which are drawn with solid-lines and dash-lines, respectively. The breakdown voltage of such devices was simulated before. Simulations were performed at 300K (black lines) and common operating temperature of 400K (red lines). It is worth noting that j_r depends strongly on the temperature, and the losses related to this effect can be very high for standards Si devices (for the simulation case, it will be $\sim$ 0.18 W.cm^{-2} at 125°C). On the other hand, the leakage current of SiC devices is relatively lower at low temperatures; and even when it increases for high temperatures, the j_r remains always lower than that for Si at normal operation temperatures.

Furthermore, when the reverse voltage applied to the drain-source terminals of a MOSFET is close enough to the Breakdown Voltage BV, a process of impact ionization starts due to the high electric field applied. In fact, every electron generated is accelerated inside of the crystal structure of the pn-junction, by the effect of the strong electric field imposed, and causes the generation of another electron-hole pair that is known as impact ionization. Such electron and hole generated are again attracted and accelerated by the electric field repeating this cycle, described in the band diagram of the Figure 1.10. Such a process is known as Avalanche Multiplication and enhances the reverse leakage current.

Indeed, this avalanche multiplication is very complex, and several models exist according to the technology and application of interest, which define an avalanche multiplication factor (M) [32], [33]. In our case, different considerations must be performed for avalanche multiplication factors due to the electron, holes and space charge currents ($M_{n,p,sc}$). However, good approximations can be performed using the relation expressed by [34] as:

$$M = \frac{1}{1 - (\frac{V_r}{BV})^m} \quad (1.28)$$

where, the fitting exponent m ranges between 4 and 6. We have considered $m = 5$ for Si and SiC simulation using $j_r = M(j_s + j_{sc})$. The enhanced j_r currents obtained for Si and

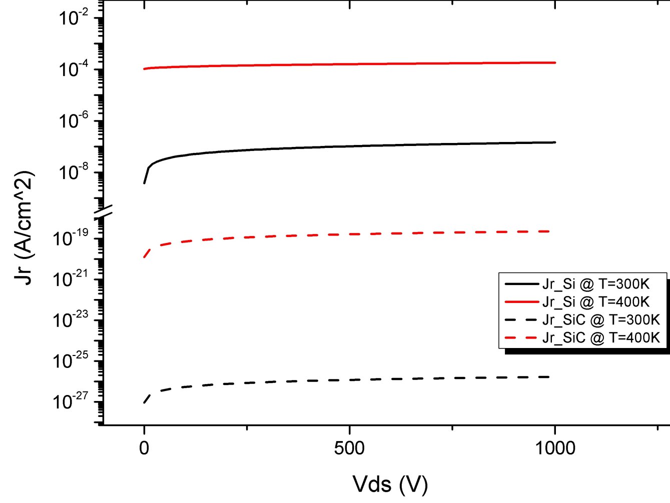


Figure 1.9: Simulation results of j_r in function of V_{DS} for a Si (solid-lines) and SiC (dash-lines) of an n-MOSFET designed for BV=1 kV. Simulations performed at 300K (black-lines) and 400K (red-lines). Avalanche multiplication effect during the breakdown was not considered.

SiC n-MOSFETs are drawn in Figure 1.11a and 1.11b, respectively. It is worth noting that j_r currents grow rapidly during the low regime reverse voltage than those presented in Figure 1.9. Then, the j_r currents rise slightly while the reverse voltage becomes high. Finally, they increase suddenly again with the high reverse voltage regimes closely to the breakdown voltage. However, the leakage current in SiC device keeps on lower values than those for Si device, even when the temperature grows to 125°C.

1.3.3 On-Resistance Parameter

Another main aspect to care in power semiconductor devices is the drain to source on-resistance (R_{DSon}) value during the conductive regime. While for low current and voltage applications, transistors present considerable high on-resistances; for high current densities applications, low values of on-resistance are required to avoid self-heating and losses due to power dissipation. In the Figure 1.12, the resistance contribution of every section inside a vertical power MOSFET structure forming the total resistance path, is represented. Such resistance contribution can be expressed as:

$$R_{DSon} = R_{sp} + R_{n^+} + R_{ch} + R_a + R_{epi} + R_{sub} \tag{1.29}$$

where, R_{sp} is the resistance in between source contact and package terminal, R_{n^+} is the source region resistance, R_{ch} is the channel resistance, R_a is the resistance related to the accumulation region, R_{epi} is the epitaxial resistance and R_{sub} is the substrate resistance close to the drain terminal.

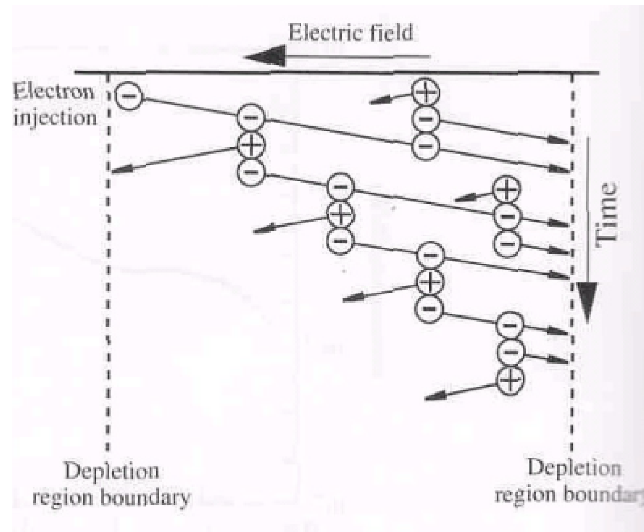


Figure 1.10: Band diagram's example of the interaction of electron-hole generation by impact ionization in the depletion zone during avalanche multiplication under the effect of a strong electric field.

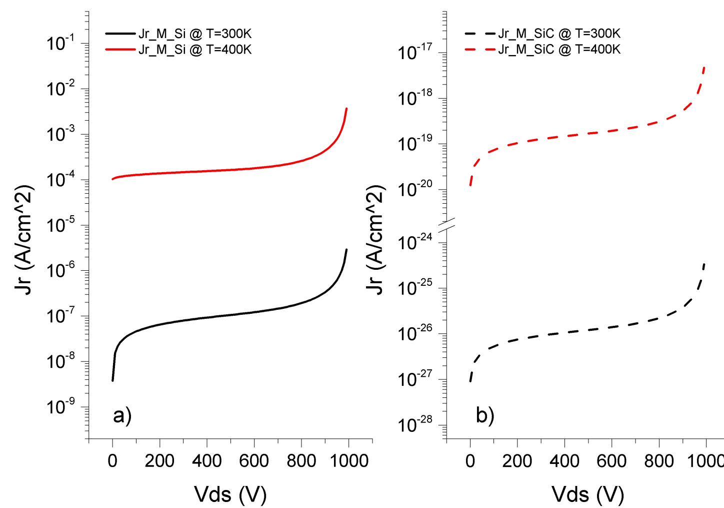


Figure 1.11: Simulation results for j_r in function of V_{DS} for a) Si and b) SiC n-MOSFETs designed for BV=1 kV. Simulation performed at 300K (black-lines) and 400K (red-lines). Avalanche multiplication effect during the breakdown was considered.

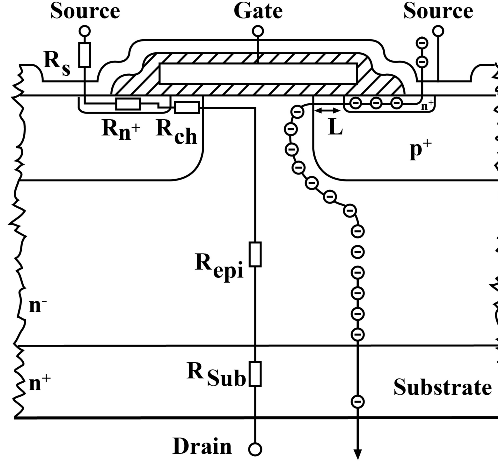


Figure 1.12: Representation of current path and resistance contribution of different sections in a standard vertical MOSFET.

Table 1.5: Resistance contribution for R_{DSon} standard vertical MOSFET for high blocking voltage. Values extracted from [35]

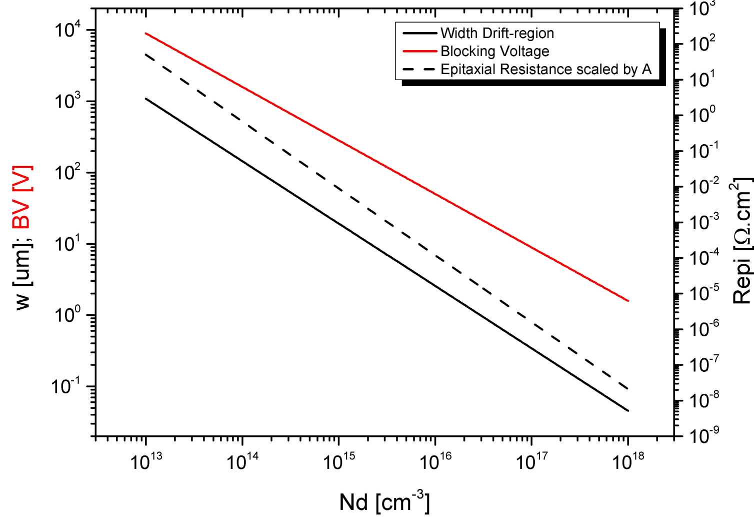
Abbr.	Section inside Power MOSFET	For $BV = 600$ V (%)
R_{sp}	Package	0.5
R_{n+}	Source region	0.5
R_{ch}	Channel	1.5
R_{a}	Accumulation region	0.5
R_{epi}	Epitaxial (drift) region	96.5
R_{sub}	Substrate close to drain terminal	0.5

However, in vertical power MOSFETs, the epitaxial resistance R_{epi} related to the low doped drift region has a big contribution in the total resistance between drain-source terminals, as summarized in Table 1.5, because the surface resistances contribution decreases with the increase of the cell density, which is given by [11]:

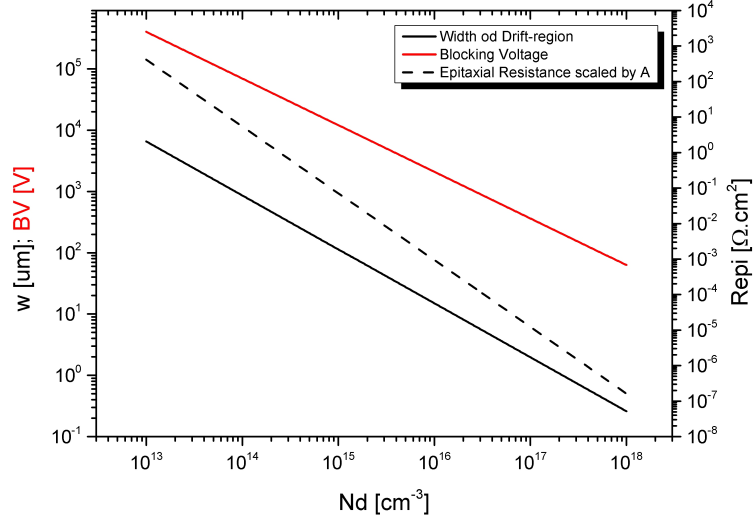
$$R_{epi} = \frac{w_D}{q\mu_n N_D A} \tag{1.30}$$

where, μ_n is the electron mobility and A is the active area of the device in cm^2.

Through a first glance at 1.30, it can be concluded that to reach lower resistances contribution of the epitaxial (drift) region, the N_D should be as high as possible due to R_{epi} is inversely proportional to the doping density. But, R_{epi} is also proportional to the w_D and this is in strongly dependence of the semiconductor material electronic properties and the doping density of the drift region as shown in 1.18. Moreover, the BV



(a) Results for Si n-MOSFET.



(b) Results for a 4H-SiC n-MOSFET.

Figure 1.13: Numerical calculation of Epitaxial Resistance (R_{epi}) scaled by the active area (A) of a power MOSFET in function of N_D. For comparison purpose, the results simulation for w_D and BV are also plotted. Simulations performed at 300K.

is directly proportional to the w_D through 1.16. This means that for a given high N_D, a decrement of the w_D is necessary to reach lower R_{epi} contribution. However, using 1.16, the decrement of the w_D (or a higher N_D using 1.17) sets a lower BV capability. These affirmations are demonstrated by the simulation results presented in Figures 1.13a and 1.13b for Si and 4H-SiC MOSFET devices, respectively.

It is worth noting that there are big differences between these two simulation cases

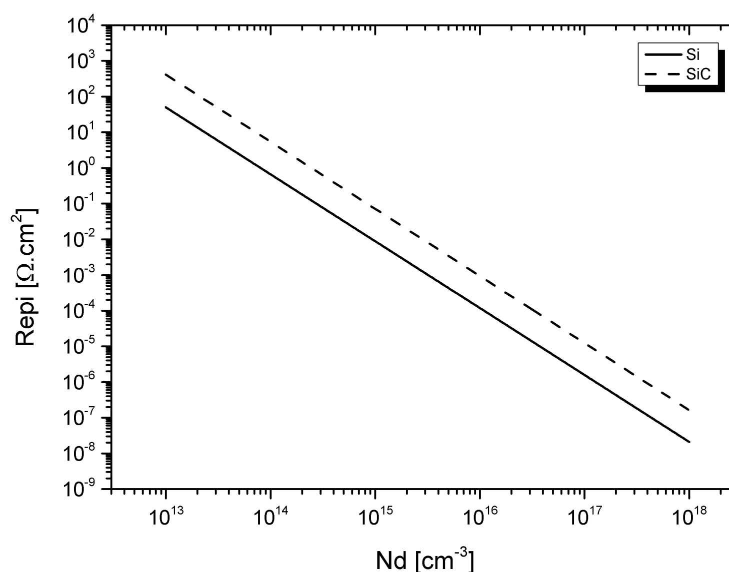


Figure 1.14: Comparison of R_{epi}, scaled by the active area A, obtained from numerical simulation for a Si and 4H-SiC vertical power MOSFET in function of N_D.

as demonstrated in the last sections. For instances, the BV values obtained though simulation as a function of the N_D for a 4H-SiC n-MOSFET, and its respective w_D, at a given N_D were shown in Figure 1.13b. These values are one order higher than those for a Si n-MOSFET shown in Figure 1.13a including the R_{epi} resistance. A direct comparison between the SI and 4H-SiC R_{epi} simulation results obtained is presented in Figure 1.14. It is worth noting that resistance data are scaled by the active area A of the devices. As mentioned, it seems that R_{epi} of the 4H-SiC device has higher values than that of Si ones for the same doping density N_D. However, this higher R_{epi} is contrasted with the higher BV reached for 4H-SiC MOSFET device.

For instance, observing the Figure 1.13a, a Si device designed for a BV=1 kV needs a N_D=1.83 $\times 10^{14}$ cm^{-3}, which results in w_D=85 μm and $R_{epi_{Si}}$ = 210 mΩ.cm^2. On the other hand, , observing the Figure 1.13b, to reach the same BV for a 4H-SiC device is necessary a higher doping concentration N_D=2.65 $\times 10^{16}$ cm^{-3}, which results in a thinner w_D=6.37 μm and $R_{epi_{SiC}}$ = 150 $\mu\Omega$.cm^2. In this way, 4H-SiC devices demonstrate to have smaller R_{epi} than Si devices at a same BV without taking in consideration the impact of the active area (A) factor for each device technology.

1.3.4 Gate Leakage Current

As shown in Figure 1.4, the gate contact terminal in the vertical power MOSFET structures is electrically isolated from the substrate and channel by a dielectric layer. In this way, a potential applied to the gate terminal generates an electric field, which creates a depletion region on the channel. Since many decades, the SiO_2 has been preferred in Si technology because it can be easily obtained via thermal oxidation technique. Even if this

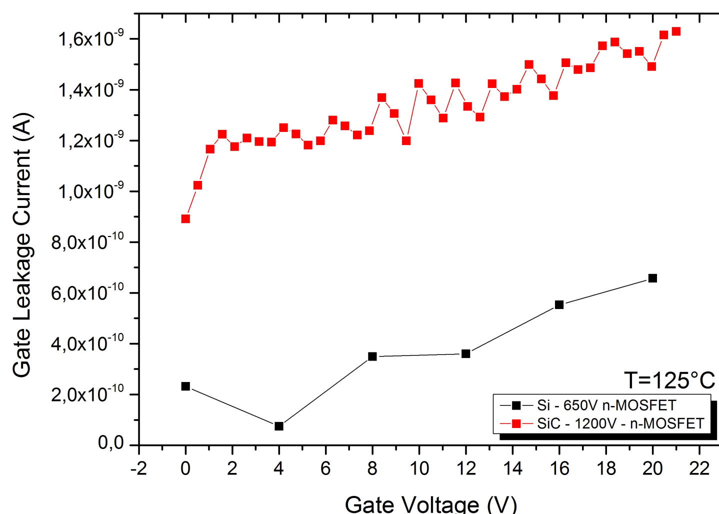


Figure 1.15: Comparison of gate leakage current measured on a 650V Si and a 1200V SiC n-MOSFET devices at 125°C.

approach is maintained for SiC, improvements of oxidation techniques and new dielectric materials are also in the course of reducing the considerable presence of interface states [36], [37].

The importance of the gate oxide is related to two tasks: a) Provide a high input impedance for the control gate terminal and b) Facilitate the control of current flow through the channel. Leakage current from gate oxides in power MOSFET devices can reveal defects and drawbacks, which can limit the performance of power MOSFETs. Main limitations of gate oxides performances are related to oxide breakdown, charge tunneling, trapping and interface defects among others. Such limitations are reflected on the gate leakage current as shown in Figure 1.15. In this case, the gate leakage current (I_{GSS}) was measured for comparison purpose in two power MOSFETs. The first device was a Commercial On The Shelf (COTS) 650V n-MOSFET in Si and the second device was a R&D 1200V n-MOSFET in SiC. It is evident that improvements are needed in the SiC device manufacturing to decrease its gate leakage current.

Contrary to the nanoscale implementation of MOSFETs, which are integrated into digital and logic integrated circuits, the problematic of gate oxides in power devices are reduced due to the oxide thickness, which must endure high drive voltages (5-20 V) compared with that of nanoscale devices, but maintaining oxide capacitances as low as possible. More details about gate leakage current, models, and tunneling problematics can be found in [38]–[42]

1.3.5 Threshold Voltage Parameter

The threshold voltage parameter is one of the main important parameter to characterize the metal-insulator-semiconductor stack in a MOSFET device. As mentioned

before, the application of a voltage on the gate terminal of a n-MOSFET induces a charge depletion region on the channel (interface p-base/oxide in Figure 1.6). If the gate voltage continues to increase, the channel experiences an inversion of charges concentration, which is sufficient to start a low current flow between drain and source terminals. This weak-inversion starts when the gate voltage is high enough to equal the surface potential (ψ_S) to the bulk potential (ψ_B) in the channel [1]. When this condition is reached, the gate voltage V_G is distributed along the thickness oxide and the channel substrate as:

$$V_G = V_{ox} + \psi_S \tag{1.31}$$

where the oxide voltage V_{ox} can be related to the total charge in the semiconductor channel Q_S by

$$V_{ox} = E_{ox} t_{ox} = \frac{Q_S}{\varepsilon_{ox}} t_{ox} = \frac{Q_S}{C_{ox}} \tag{1.32}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$, and it is the specific oxide capacitance.

Only when the device enters in strong-inversion operation, the carrier density becomes sufficient to allow conduction of current between drain and source terminals through the channel. Hence, the Threshold Voltage (V_{th}) can be defined as the gate voltage at which the MOSFET enters in the strong-inversion operation. Normally, this condition is reached when surface potential (ψ_S) is equal to twice the bulk potential (ψ_B) [1], [43]. Then, using (1.31) and (1.32), the V_{th} can be expressed as

$$V_{th} = \frac{Q_S}{C_{ox}} + 2\psi_B, \tag{1.33}$$

with

$$\psi_B = \frac{kT}{q} ln(\frac{N_A}{n_i}). \tag{1.34}$$

Due to the Q_S depends on the surface potential ψ_S and acceptor doping density N_A of the p-base region in a n-channel MOSFET, the total charges in strong-inversion operation are determined in [43] as:

$$Q_S = \sqrt{4\varepsilon_S q N_A \psi_B}, \tag{1.35}$$

where, ε_S is the electric permittivity of the semiconductor surface. Therefore, a more defined expression for V_{th} can be found replacing (1.35), and $C_{ox} = \varepsilon_{ox}/t_{ox}$, in equation (1.33), as:

$$V_{th} = \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{4\varepsilon_S q N_A \psi_B} + 2\psi_B. \tag{1.36}$$

Nevertheless, the expression (1.36) describes an idealized threshold voltage and it does not consider the flat-band voltage (V_{fb}) of the MOS structure. The V_{fb} depends on the charge trapping and impurities ions in the oxide [44], [45], and its study is outside of this work.

However, equation 1.36 shown that threshold voltage V_{th} directly dependences on the acceptor doping concentration N_A in the channel region and the thickness of the dielectric

Table 1.6: Calculation parameters for the reported V_{th} simulations.

Symbol	Description	Units	Figure 1.16 Si	Figure 1.16 SiC	Figure 1.17 Si	Figure 1.17 SiC
N_A	Acceptor doping density	cm^{-3}	1e16 - 1e18	1e16 - 1e18	1e17	1e16
ε_S	Permittivity of Substrate		11.7	9.72	11.7	9.72
ε_{ox}	Permittivity of oxide		3.9	3.9	3.9	3.9
N_C	States conduction band density	cm^{-3}	3.10e19	4.20e20	3.10e19	4.20e20
N_V	States valence band density	cm^{-3}	2.86e19	3.80e19	2.86e19	3.8e19
t_{ox}	Oxide thickness	nm	1 - 100	1 - 100	50	50
T	Temperature	K	300	300	200 - 500	200 - 500
E_g	Bandgap Energy	eV	1.17	3.263	1.17	3.263

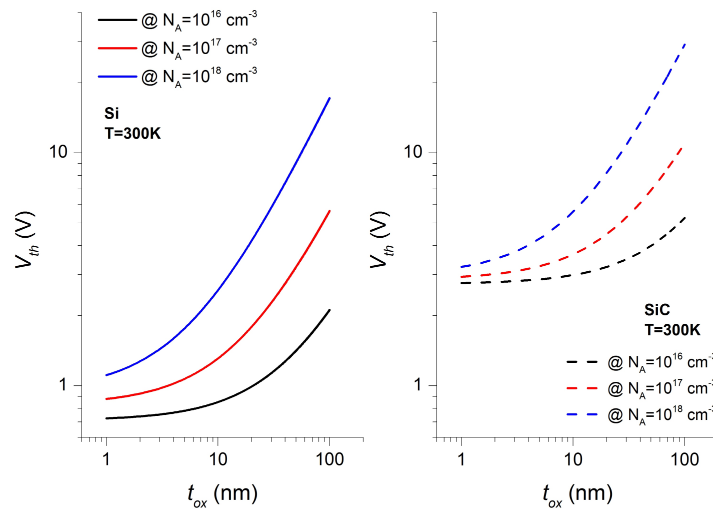


Figure 1.16: Threshold voltage simulation as function of oxide thickness t_{ox} for different acceptor doping densities N_A for Si and SiC n-channel MOSFETs.

gate insulator t_{ox}. It is worth noting that the bulk potential ψ_B is directly affected by temperature T, but it is also inversely proportional to the intrinsic concentration carriers n_i (see equation 1.34). Due to the n_i depends strongly on temperature, the V_{th} decreases at high temperature device operation as demonstrated through a numerical simulation performed using calculation parameters summarized in Table 1.6.

In this way, simulations of V_{th} at 300K, as a function of t_{ox} and at different doping concentration of the p-base region (N_A), are presented in Figure 1.16 for a Si and a 4H-SiC n-MOSFET devices. In these simulations, the impact of Si and 4H-SiC electric properties in the threshold voltage was compared using identical oxide thickness and doping acceptor densities. It is evident that higher V_{th} are required in the 4H-SiC device to force its channel in the strong-inversion operation ($\psi_S \geq 2\psi_B$ condition). This is mainly because of the higher bandgap energy (E_g) and the lower intrinsic carrier density

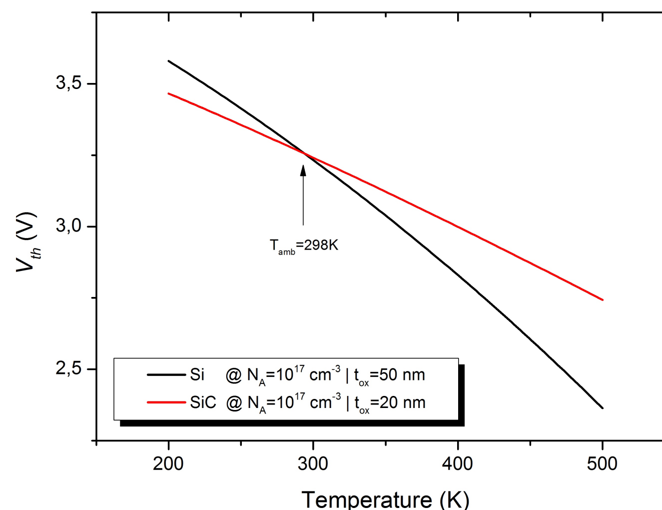


Figure 1.17: Threshold voltage simulation as function of temperature for Si and SiC n-channel MOSFETs. Parameters calculation of both devices were selected to have a similar V_{th} at room temperature.

(n_i) of SiC (see Table 1.6).

Moreover, as was mentioned before, the V_{th} depends also on the temperature operation through ψ_B, which is function of thermal velocity ($v_{th} = kT/q$) and n_i (see equation 1.36). In the Figure 1.17, simulation results of V_{th} as function of the temperature are presented for Si and SiC n-channel MOSFETs. Parameters calculation of both devices were selected to have a similar V_{th} at room temperature (see Table 1.6). As shown in Figure 1.17, the V_{th} decreases when the temperature increases for both devices. However, the threshold voltage of the Si MOSFET is lower at high temperatures than SiC device. This last is not favorable for applications working in the high-temperature regime, where SiC technology can demonstrate improvements in this aspect. More details about these concepts and physic models can be found in [1], [43].

1.4 Noise in Semiconductor Devices

Noise is a random process that is present in every circuit or device. Noise can be generated by external or internal sources. This section will be referred to internal noise in semiconductor devices. In particular, noise in semiconductor devices is a physical phenomenon, which occurs at microscopic level involving interactions of charge carriers with defects. Thus, the noise affects the output performance being a direct evidence of the presence of defects in the structure of the device. In fact, low-frequency noise measurements have been considered as a tool for the experimental investigation of microscopic defectiveness inside electronic devices [9], [10].

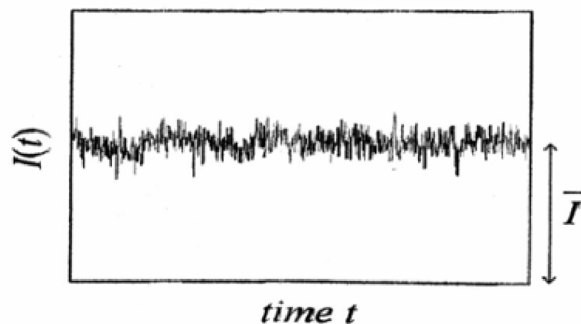


Figure 1.18: Typical electronic signal noisy [47].

The output current affected by noise (see Figure 1.18) can be defined as

$$i(t) = \overline{I} + i_n(t) \tag{1.37}$$

where, $\overline{I}$ is the average current and $i_n(t)$ is a random fluctuating current with average value equal to zero. However, the specific current value at a certain time can not be determined, even if the past of the current is known, but typical statistical properties of noise can be predicted such as amplitude distribution or average power [46]. Therefore, in order to quantify the noise and incorporate it as an electronic characteristic for electronic devices diagnosis, statistical models are needed. Moreover, more information about the noise generation is obtained when it moves from the time domain to the frequency domain through Fourier transform. In this case, it is possible to characterize the noise by means of Power Spectral Density (PSD) [46].

1.4.1 Power spectral density

Predicting the power of a random signal is necessary to measure the signal over a long time. Thus, the average power delivered by a voltage noise $v(t)$ to a load resistance is given by

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_0^T \frac{v^2(t)}{R} dt. \tag{1.38}$$

Usually, the average power of a signal is referred to 1Ω load and is expressed, therefore, in V^2 or A^2 rather than W. However, the concept of average power can be better expressed when it is defined in frequency domain. This concept is introduced as Power Spectral Density (PSD). Thus, the PSD unit of a voltage or current noise is V^2/Hz or A^2/Hz, respectively. The PSD of a random variable (noise) is defined by means of Wiener-Khintchine theorem [47] as

$$S(f) = 4 \int_0^\infty \overline{X(t).X(t+s)} cos(2\pi fs) ds, \tag{1.39}$$

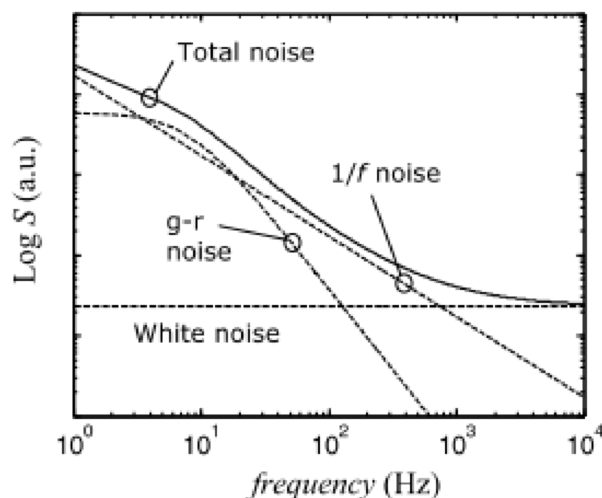


Figure 1.19: PSD (S) of low-frequency noise and white noise plotted vs. frequency [47].

where, $S(f)$ is the Fourier Transform of $\overline{X(t).X(t+s)}$, which is

$$\overline{X(t).X(t+s)} = \lim_{T\to\infty} \frac{1}{T}\int_0^T X(t).X(t+s)dt. \tag{1.40}$$

Thus, with $s = 0$ in eq. 1.40, the power of the noise variable is obtained as

$$\overline{X^2(t)} = \int_0^\infty S(f)df. \tag{1.41}$$

then, the power of a signal P obtained form its PSD is determined by

$$P = \int_{f_1}^{f_2} S(f)df. \tag{1.42}$$

As can be noted in Figure 1.19, a noise signal with constant $S(f)$ for all frequencies is called "white noise", and it is usually observed at high-frequencies. While, at low-frequencies the noise is typical dependent on frequency. The corner transition from low-frequency to white noise depends on type, size, bias point among others, of the device under test. Typical white noise can be predicted and avoided through circuital solutions, however, low-frequency noise can be related to several sources and are still an open discussion in literature. Such low-frequency noise sources will be reviewed below.

1.4.2 High Frequency Noise

Thermal Noise

The random motion of electrons in a conductor material, which is induced by the electron scattering activated by thermal energy, leads to thermal noise, even if the average over time is always zero. Such a thermal noise depends on the material resistance

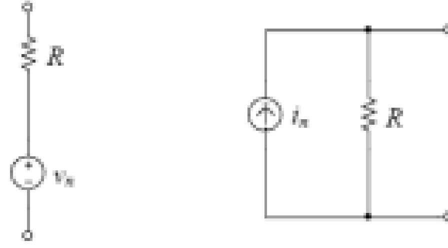


Figure 1.20: Circuital models of the thermal voltage and current noise.

R, with a PSD for the noise current described by

$$S_I = \frac{4kT}{R} \tag{1.43}$$

where k is the Boltazmann's constant and the temperature T is given in Kelvin. The PSD of the thermal voltage noise is

$$S_V = 4kTR. \tag{1.44}$$

It is worth noting that the PSD of the thermal noise is not frequency dependent being considered white noise. However, thermal noise is not white over all the frequencies otherwise the noise power would extend to infinity which is unphysical. In fact, the extended expression of the thermal current noise in eq. 1.43, which includes a correction factor, is

$$S_I = \frac{4}{R}\frac{hf}{exp(hf/kT) - 1}, \tag{1.45}$$

where, h is the Planck's constant. For the $f << kT/h$ condition, the eq. 1.45 is simplified in eq. 1.43, while for higher frequencies S_I drops.

In the Figure 1.20, the circuital modeling of thermal voltage and current noise are shown. In both cases a noiseless resistance is used in serie with a noise voltage source and in parallel with a noise current source, respectively.

Shot Noise

This kind of noise is associated to a potential barrier and to the discrete nature of charges (electrons) to cross it in random and independently manner [47]. Potential barrier in electronic devices is usually formed by pn-junctions such as in diodes, MOSFETs, Bipolar Transistors among others. No barrier is present in a simple conductor, therefore no shot noise is present. The PSD of the shot noise that describes the fluctuation of the current I that crosses the barrier is described as

$$S_I = 2qI. \tag{1.46}$$

A current is necessary to induce shot noise, however, in a pn-junction both forward and backward current noise contribution must be considered separately. In fact, considering the below expression of the current in a diode

$$I = I_0(e^{(qV_d/kT)} - 1), \tag{1.47}$$

where, I_0 is the saturation current and V_d is the diode voltage applied, the total shot noise is the sum of both contributions as

$$S_I = 2qI_0e^{(qV_d/kT)} + 2qI_0 = 4qI_0|_{V_d=0V}. \tag{1.48}$$

Moreover, the instantaneous (dynamic) resistance of the diode (r_d) can be approximated from eq. 1.47 as

$$r_d = \left(\frac{dI}{dV_d}\right)^{-1} = \frac{kT}{qI_0e^{(qV_d/kT)}}. \tag{1.49}$$

Then, the evaluation of this expression for V_d=0V results in $r_d = kT/qI_0$. Finally, considering eq. 1.48 for V_d=0V, it results in $S_I = 4kT/r_d$ that is exactly the same as the thermal current noise expression. In fact, there is a close relation between shot and thermal noise, however, if $I \gg I_0$ the expression is reduced to half of the PSD ($S_I = 2kT/r_d$).

Apparently, the shot noise is not frequency dependence but this is true only for frequencies lower that $1/\tau$, being τ the time which the charge carriers take to cross the potential barrier (depletion region). Other limitation is the correlation between current pulses which results in a different expression for shot noise [48].

1.4.3 Low Frequency Noise

The random capture and generation of carriers, originated by traps in surface energy states and the density of surface states of the material, is called generation-recombination (g-r) noise. The latter is characterized by the fluctuations of the number of carrieres available for current transport [47]. The traps are usually related to particular interfaces defects or impurities that produce electronic states which are activated under specific energies. Thus, g-r noise is generated by the charges jumping between these electronic states, each one characterized by a certain time constant (τ) for the transitions. The PSD of a single g-r noise process is characterized by a Lorentzian spectrum as shown in Figure 1.19.

Moreover, a considerable density distribution of electronic states can lead to a particular noise generation called Random-Telegraph-Signal (RTS) [47]. The PSD of RTS noise is again characterized by Lorentzian spectrum as that of g-r noise. RTS and g-r noise generation describe constant high power noise at frequencies lower than that determined by the trapping/detrapping process. For frequencies higher than the latter, the noise decrease with a power relation $\sim 1/f^2$. Interesting information about the trap

energy level, capture and emission kinetics and spatial location of the traps can be obtained from RTS and g-r noise characterization using temperature or bias dependencies [49], [50].

Furthermore, *flicker noise* was first observed in vacuum tubes evidenced by flickering observed in the plate current. The PSD of this kind of noise follows $S_I \sim 1/f^\gamma$ characteristic, where f is the frequency and the slope coefficient γ often is close to 1, but it has been observed to take on values from 0.8 to 1.3 in various semiconductor devices [10], [47], [51]–[55]. Moreover, 1/f noise has been measured in emergent 2D technologies like Graphene and similar [56]–[60].

Generally, the PSD of the $1/f$ current noise is described through the expression:

$$S_I = \frac{K \cdot I^\beta}{f^\gamma} \quad [A^2/Hz] \tag{1.50}$$

where, β is the bias current exponent (usually set as 2) and K is a proportionality constant that is mainly related to the structure device and/or material properties. Since the current bias I is not the noise source but a current scaling factor, this facilitates the detection of the $1/f$ noise through measurement techniques. Moreover, $1/f$ has been extendedly studied from different point of views. Mainly, two models have been proposed for $1/f$ noise modelling [61]. Hooge noise model ($\Delta\mu - model$) associates the $1/f$ to the fluctuations of the carrier mobilities in conductive channels [62], while the second one is the McWorther model ($\Delta n - model$) describes the $1/f$ noise as the fluctuation of the number of carriers [63]. The latter has been widespread recognized as the principal explanation of flicker noise mainly because the first model is based in a empirical formulae and experimental observations. However, both models have been used to describe $1/f$ noise in semiconductor devices, where one can explains the phenomenon and the other cannot [10], [55], [64], [65]. Furthermore, other mixed or unified noise models have been also proposed as that presented in [66].

However, the $1/f$ noise can be approximated by the superposition of multiple g-r noise mechanisms as shown in Figure 1.21 [47]. Due to the flicker noise follows a inverse power law dependence on frequency, the noise is higher at the low-frequency part of the spectrum (10^{-5} to 10^7) as was shown in Figure 1.19 [47]. While 1/f noise is not a problem for high frequency communications, it is a clear evidence of defects into the charge conductive structures of devices. In fact, recent studies using 2D-materials have demonstrated that 1/f noise is merely a surface effect when the thickness of the conductive film (or channel formation in the case of MOSFETs) is $< \sim$2.45 nm, otherwise can be attributed to a volume effect [56], [57], [60], [67].

Improved surface treatment in manufacturing has decreased 1/f noise, but even the interface between semiconductor surfaces and grown oxide passivation are centers of noise generation. Therefore, flicker noise is quite common. Thus, this is not only observed in transistors, diodes, and resistors, but it is also present in thermistors, carbon microphones, thin films, and light sources. Furthermore, no electronic amplifier has been found to be free of flicker noise.

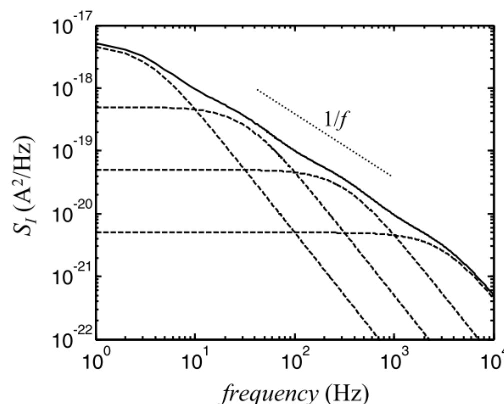


Figure 1.21: Superposition of 4 Lorentzians giving a total spectrum that approximately exhibits a 1/f dependence over several decades of frequency. Extracted from [47].

Chapter Conclusions

In this chapter, some fundamental electronic properties of Silicon (Si) and Silicon Carbide (SiC) semiconductor materials have been reviewed as a first conceptualization.

Then, widely used vertical structures for power MOSFETs were presented. The case of study in this chapter was the DMOSFET structure, which was used for the study of the electric characteristics of power MOSFETs such as the I-V transfer curves characteristic.

In this way, electrical parameter properties of power MOSFETs were reviewed through models and simulations. The parameters reviewed were: Drain Breakdown Voltage, Drain Leakage Current, On-Resistance, Gate Leakage Current and Threshold Voltage. Evaluation of these parameters constitutes a valuable tool for characterization process in the semiconductor manufacturing. Hence, even a superficial knowledge of the physics of these characteristic parameters is well appreciated for reliability purposes.

Furthermore, main concepts of low-frequency noise were presented. Internal noise sources in electronic devices (including power MOSFETs) were briefly reviewed. The major cause of 1/f noise in semiconductor devices is traceable to the properties of the surface or volume of the material and structure of the device. Though low-frequency noise does not represent a serious problem in power MOSFETs, its measurement and characterization can constitute an important tool for diagnostic of defectiveness inside devices during reliability tests [9]. In the next chapters, measurement procedures and standards will be reviewed to evaluate the parameters properties here studied.

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Chapter 2

Reliability Testing on Power Devices

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Reliable semiconductor technologies are continuously demanded in the nowadays competitive technological applications market. Different high reliable applications involve Military and Satellite, Automotive, Renewable Energy, Avionics and others critical fields [68], [69]. However, also other less critical fields demand high reliability on products otherwise considerable economic losses can be registered [70].

Since the first silicon devices appeared, continuous improvements have contributed to the maturity of this technology over decades [69]. Specific power applications demanded for reliable power transistors able to work with high rated voltages/currents for many years. Hence, competitors manufacturing semiconductor devices started to develop set and procedures for testing devices, according to the emerging and customer needs. In this way, accelerating tests and reliability tests began to be applied in semiconductor

devices to investigate deterioration and degradation of materials during device operation as well as the defects introduced during design and production process. Rapidly, reliability concepts and standards were appearing together with rigorous testing for products qualification in semiconductor devices.

Traditionally, the reliability of a device has had two components. The first one is a methodology for accelerated life testing of products and the second one is probabilistic models for failure prediction. One example of this approach is the MIL-HDBK-217 [71]. Other traditional standard methodologies for reliability are discussed in [72]. However, last advances in engineering and science fields have enabled for adopting a complete reliability analysis researching for failures modes and mechanisms that dominate the power semiconductor field [73]. Furthermore, the reliability testing has carried the Si technology out to the actual maturity during the last decades. However, new challenges in reliability tests have born with the Wide Band Gap (WBG) technologies for semiconductor devices [28], [74], [75].

In this chapter, a revision of reliability concepts and methodologies will be presented, focusing in the case of non-reparable items for reliability purposes [76]. A survey study of the most accelerated life test practiced in the industry, together with electrical measurements on power MOSFETs, will be also covered.

2.1 Why Reliability on Power Semiconductor Devices?

As mentioned before, power semiconductor devices are well diffused in any nowadays electronic application. Most of such power applications are fundamental and critical for modern systems and technological fields. In this way, the need for high reliability of power electronics devices has been increased in the last 15 years [77]. Some reasons for this increased requirement are:

- Last applications handle continuously more power densities, expressed as controlled power by unit volume, which can be performed only through the increment of current densities keeping the die semiconductors and package as small as possible. This demand has led to the increment of power loss through heating dissipation with the consequence of higher operating temperatures, which also affect the packaging.

- Emerging applications, such as automotive and train electric traction, demand electronic semiconductor devices to work in adverse thermal conditions with temperatures around 125 °C. These application fields require power devices to guarantee higher quoted junction temperatures around 175-200 °C.

- New power devices based on WBG technologies possess better electric and thermal characteristics than Si. For instance, SiC (Silicon Carbide) and GaN (Gallium Nitride) power devices are rated to operate with junction temperatures above 200 °C and higher blocking voltages (1.2 to 3.3 kV).

- Nowadays electronic applications have a high density of power devices. Furthermore, the trend to lithography shrink is also continuing for Smart Power technologies enabling for new products with more spread of functionalities in a single chip. Most of them work in cascade decreasing the reliability of the application because of the effect that a failure can cause to its integrity. Reaching high reliability of every element increases the total reliability of the application.

It is worth mentioning that, once the semiconductor technology is in a maturity state, most of the reliability of power devices depends on the materials and process for packaging. Since the package faces directly harsh environments during normal operation of devices, this must reach as high reliability as that for the semiconductor die. In this context, materials, structures and functionalities (characteristics) of a single electronic device or product, must be tested to guarantee a certain "Lifetime" working at a determined "Mission Profile."

2.2 Reliability Concepts

Many authors agree on defining the reliability of a product $R(t)$ as the probability of such a unit can work during a determined time, always under specific conditions, without experiences a failure [12], [76], [78]. On the other hand, the unreliability of a product $F(t)$ can be defined as the probability that such a unit experiences a failure before a determined time, always working at determined conditions [76]. Thus, the following probability relationship for whichever product can be stated as

$$R(t) = 1 - F(t). \tag{2.1}$$

In the base of these definitions, many concepts are considered, such as the necessity of statistical calculation of sample population to be tested and the distribution function to be considered to describe the trend of failed devices, together with acceleration models, to establish the reliability of the product. Furthermore, since failures are a function of the time operation, it is important to consider the application area in which the tested item is involved. For instance, the expected lifetime of electronic parts in the automotive field is a decade but for parts involved in a guided missile only minutes are considered. Other kinds of considerations must be performed on the specific conditions under which the product will be tested [78].

Nevertheless, the definition of failure, which determines when a device fails, must also be detailed. A failure could be considered as whichever condition of the Device Under Test (DUT) that impedes to reach the target profile. In particular, failure in a device can be the shifting of its electrical parameters beyond the established limit or the package explosion, which could also complicate the post-failure analysis stage.

2.2.1 Failure Terms

There are some expressions related to specific measurements of reliability. The failure rate $\lambda(t)$ can be defined as the ratio between the number of failed units (n) and total

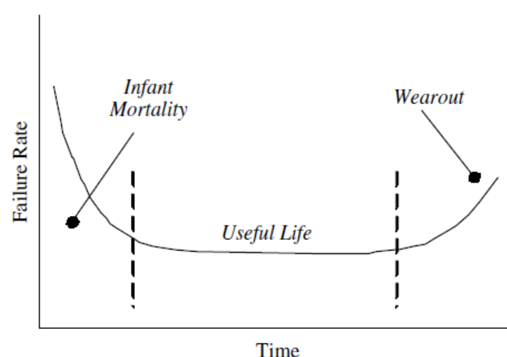

Figure 2.1: Typical bathtub curve of the failure rate in function of time.

work time performed by the units before failures.

$$\lambda(t) = \frac{n}{t_1 + t_2 + \ldots + t_n} \tag{2.2}$$

It is a calculated value that provides a measure of reliability of a product. This value is usually expressed as failures per million hours (fpmh or 10^6 hours), but can also be expressed as failures per billion hours (Failures In Time (FIT) or 10^9 hours).

The Mean Time To Failure (MTTF) is also a fundamental measurement of reliability that describes the mean time elapsed until the first unit failure. If the failure rate, λ is constant; then, it is inversely proportional to the MTTF.

$$MTTF = \frac{1}{\lambda(t)} = \frac{t_1 + t_2 + \ldots + t_n}{n} \tag{2.3}$$

Nevertheless, the Mean Time Between Failure (MTBF) represents statistically the time elapsed between two consecutive failures, assuming a constant failure rate, λ.

$$MTBF = \frac{(t_2 - t_1) + (t_3 - t_2) + \ldots + (t_n - t_{n-1})}{n} \tag{2.4}$$

Another consideration into reliability field is the variation of the failure rate in time. In this context, the bathtub curve of the Figure 2.1 presents three stages that describe the variation of λ with time. The initial part of the curve is characterized by a decreasing failure rate, which describes the transition from a high failure occurrences at an early stage to a constant failure rate (second part of the curve). Failures ocurred in this first part are correlated with specific weakness/defects in units. This reliability stage of a product is known as infant mortality. As soon as failure rate becomes constant, the useful life part of the bathtub curve is manifested (see Figure 2.1). Failures with a constant rate are random and are related to specific mechanisms that can result via the stress parameters and workload profile of an accelerated test. Finally, a increased failure rate (third part in the bathtub curve) is again presented in the end, and it is related to the normal wearing out and aging processes on the units.

2.2.2 Acceleration Factor and Accelerated Test

There are several definitions for the term Acceleration Factor (A_F) [12], [76], [78]–[80]. A practical definition of A_F is the ratio between the stress load of an accelerated test and the load experienced by the units in normal operating conditions. Such A_F is most related to the Arrhenius Model [81] in terms of two different absolute temperatures T_o and T_t (operating and test temperature, respectively):

$$A_F = e^{\frac{E_a}{k}(\frac{1}{T_0} - \frac{1}{T_t})} \tag{2.5}$$

where, E_a is the activation energy necessary to reproduce a specific failure mechanism and k is the Boltzmann's constant. It is worth mentioning that E_a can only be determined from experimental data, but this topic is not covered in this thesis work. However, an excellent explanation about the extraction of E_a for failure mechanisms can be found in [79], [82]. Furthermore, reported E_a values, used for reliability prediction on SiC devices, can be found in [83], [84].

On the other hand, as mentioned before, accelerated tests are used to apply stress loads in power semiconductor devices because of the large lifetime quoted for such units. In particular, DUTs subjected to higher-than-usual levels of one or more accelerating variables, while measurement of electrical and electronic characteristics of DUTs is performed, wearing out the DUTs to observe failures in a reasonable amount of time. The acceleration of such failures depends on the test conditions factors, i. e. temperature, voltage/current, humidity, cycling operation, radiation among others. The aim is to produce accelerated failures in controlled environments in a short time, which can be equivalent to failures produced in normal conditions applications in a long time due to wearing out of DUTs [12].

Therefore, accelerated testing field is very useful to verify the reliability of semiconductor devices in short-time instead of normal lifetime operation. Thus, analyzing degradation and failure mechanisms of devices working in normal conditions is impractical due to their long expected life. Moreover, the results of non-accelerated tests are only useful for the operating environment similar to those of the test conditions [80].

2.3 Reliability Methodologies Testing

Reliability of electronic devices using accelerated tests is applied through Accelerated Life Tests (ALTs) methodologies and is assessed through prediction models [85]. ALTs methodologies are applied during the assessment of products in the phase of R&D and qualification to render roughness the devices and technologies. In this section, different ALT reliability methodologies are reviewed.

2.3.1 Accelerated Life and Degradation Testing

Accelerated Life Testing (ALT) methodology was initially developed to assess whether the products meet the expected long-term reliability requirements. Usually, ALT tests can be conducted in three different modes [80]:

- Accelerating the use cycles of a product under normal operating conditions. This approach was oriented to test products that are used only short periods of time per day.
- Over-stressing the product samples with higher work conditions than normal to accelerate the manifestation of failures.
- Alternatively, continue with the accelerated stress over the before degraded products to evaluate the final development of the degradation process. This mode is also referred as Accelerated Degradation Testing (ADT).

2.3.2 Highly Accelerated Life Testing

Highly Accelerated Life Testing (HALT) is oriented to improve designs and production process of products addressing to the determination of the operational limits of the products. In this way, extreme stress conditions are applied to determine all potential failures modes of the devices. Usually, during the R&D of semiconductor devices, several HALT are performed at increased step of stress to assure adequate design margin within application environments and maximum stress conditions. In typical HALT tests of power electronic devices, temperature, humidity and/or voltage are used to over-stress the DUTs, however, acceleration stress factors are seldom dimensioned. [80], [86]–[88].

2.3.3 Highly Accelerated Stress Screening

Once the design has been strengthened, and the production has started, Highly Accelerated Stress Screening (HASS) is carried out on samples of the production lots to verify the proper operation of the final product. HASS is frequently used for qualification of a production process assuring the manufacturing of useful devices. Several environments for stressing (i. e. temperature, humidity, voltage, etc.) can be employed in HASS if devices have been tested during the design phase with HALT methodology. However, the stress level is derating because the purpose of HASS is only to verify the normal operation (and degradation) of a well-settled device designed [80], [87], [88].

2.3.4 Reliability Demonstration and Acceptance Tests

Reliability Demonstration Test (RDT) and Reliability Acceptance Test (RAT) are similar tests oriented to highlight whether produced devices reaches the reliability metrics imposed for the qualification. Typically, these methodologies state conditions such as a minimum number of devices that does not fail the tests before a specified number of work cycles or hour test. RDT and RAT do not use extremely accelerated conditions; however, results of a test performed with these methodologies support the decision for accepting or unaccepting the produced lot [80].

2.3.5 Burn-In Test

This methodology is a widely used methodology in the industry to screen the less reliable devices from a production lot. Usually, the stress conditions are accelerated during the tests and the time duration is around 24-48h. Burn-In Test methodology is applied to packaged devices. This methodology uses temperature and voltage stress to evaluate failure mechanisms that depend on these factors in short-time, and that could cause infant mortality of devices (see Figure 2.1) [80].

2.4 Accelerated Life Testing for Power Semiconductor Devices

As mentioned before, semiconductor electronic devices are expected to work for decades, and it is impractical to test devices for all this time. Hence, manufacturing industry has always been practicing accelerated tests for reliability purpose. These "empirical tests" have supported the elaboration of several methodologies and guidelines for a wide number of reliability tests. Each reliability test is oriented to evaluate specific failure mechanisms of electronic devices when these are working in adverse conditions. Furthermore, much of these tests are also used for qualification of products and production process in the semiconductor field. Table 2.1 presents the more frequent reliability tests applied to the power semiconductor devices, such as MOSFETs and IGBTs. Nowadays, these tests have become international standards overseen by associations and state departments, i.e. Automotive Electronics Council (AEC), Joint Electron Device Engineering Council (JEDEC), Military Department of Defense of United States (MIL-DoD), International Electrotechnical Commission (IEC), etc. However, these represent only a reference or guideline because in most of such standards, contradictions, and unclear situations are also present.

However, every manufacturer of power semiconductors has developed its internal test procedures, enabling for the internal quality level of its products, but at the same time, this tendency makes difficult the comparison of qualification test results from different suppliers.

Even if the reliability tests from the Table 2.1 are not categorized, these are oriented to test the electrical characteristics and package properties of power semiconductor MOSFETs and IGBTs (and power modules). More details about these listed tests can be found in [77], [80], [89]. Nonetheless, the entire tests are necessary for reliability purposes, the “High Temperature Reverse Bias” (HTRB) will receive a depth attention in the next chapter.

2.5 Electrical Characterization of Power Devices

Nowadays, power devices are well covered by MOSFET devices, which exhibit a set of electrical parameters features reviewed in the first chapter. Furthermore, specific procedures for measuring such parameters have been elaborated and collected in

Table 2.1: Summary of Reliability Tests for Electric and Package Characteristics of MOSFET according to their respective standards.

Acronym	Name	Typical Conditions	Standard
HTRB	High Temperature Reverse Bias	t:1000 h V: 80% BV T : 150 – 175 °C	JESD22-A108D IEC60747-8:2010 MIL-STD-750
HTGB	High Temperature Gate Bias	t:1000 h V: max. BV_{gate} T: 150 °C	JESD22-A108D IEC60747-8:2010 MIL-STD-750
H3TRB (THB)	High Humidity High Temperature Reverse Bias	t:1000 h T: 85 °C H: 85% RH V: 80% BV	JESD22-A101D:2010 IEC60749:2002 MIL-STD-750
TST	Thermal Shock Test	$T_{stg_{min}} - T_{stg_{max}}$: -40 °C to 125 °C $t_{storage}$:1 h t_{change}:30 s	JESD22-A106B:2004 IEC60749:2002 MIL-STD-750
LTS	Low Temperature Storage	$T : T_{stg_{min}}$ t: 1000 h	JESD22-A119:2004 IEC60068-2-1 MIL-STD-750
HTS	High Temperature Storage	$T : T_{stg_{max}}$ t: 1000 h	JESD22-A103D:2010 IEC60068-2-2 MIL-STD-750
TC	Temperature Cycling	ΔT_C: 80 K t_{cycle}: 2 - 6 min. Cycles: 2000 - 5000	JESD22-A104E:2014 JESD22-A105c:2011 IEC60747-8:2010 IEC 60747-2/7:2000 MIL-STD-750
PC	Power Cycling	Heating by Power Dissip. Cooling externally t_{cycle}: 0.5 - 10 s Cycles: 20000 - 100000 $T_{j_{max}}$: 125 °C	JESD22-A122:2007 JESD22-A105c:2011 IEC60747-8:2010 IEC 60749-34:2010 MIL-STD-750
V	Vibration	Sin. sweeps: 5g, 2 h per axis	JESD22-B103B:2006 IEC60068-2-6:2007 MIL-STD-750
MS	Mechanical Shock	t: 30g, three times per axis	JESD22-B104C:2004 IEC60068-2-27:2008 MIL-STD-750

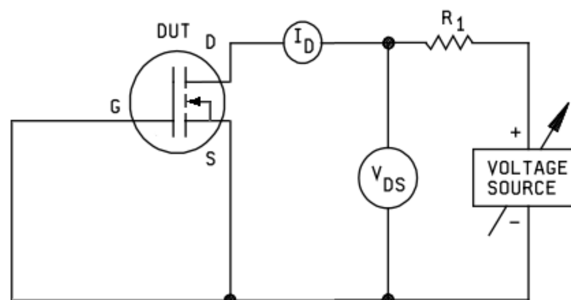

Figure 2.2: Test circuit for drain to source leakage current (I_{DSS}) measurement in Power n-MOSFETs.

standards. By way of example, MIL-STD-750 series standard [90], titled Test Methods for Semiconductor Devices, provides the electrical connections and the required information for measurement of device electrical characteristics. In this section, electrical characterization methods for power MOSFETs will be deeply reviewed.

2.5.1 Drain to Source Leakage Current Measurement

The purpose of this test is to measure the I_{DSS} when the terminals Drain and Source are reversed polarized under specific conditions (see Figure 2.2). This test can be regulated by the method 3413.1 of the MIL-STD-750:3 [90]. As far as power enhanced MOSFETs are concerned, this measurement is performed with the Gate-Source terminals short-circuited to ground (V_{GS}=0 V) (see Figure 2.2).

2.5.2 Drain to Source Breakdown Voltage Measurement

This measurement method uses the same electric schematic from Figure 2.2 for power enhanced MOSFETs, and it constitutes an extension of the I_{DSS} measurement method. In this way, the specified turn-off gate voltage condition must be applied, while the drain to source bias is adjusted to make a certain drain current (I_D) flow. Once, the desired I_D is reached, the drain to source voltage is measured, which is called Breakdown Voltage Drain to Source (BV_{DSS}). Usually, the measured BV_{DSS} will be larger than the designed one. Reference to this measurement can be found in [90](method 3407.1).

2.5.3 Gate Leakage Current Measurement

This test is supported by MIL-STD-750:3 [90] (method 3411.1). In the ambit of the power MOSFETs, the purpose of this test is to measure the gate leakage current (I_{GSS}) when specific voltage bias condition of the drain to source is applied. Usually, a short-circuit between drain and source terminals is used as shown in Figure 2.3. The normal procedure to measure I_{GSS} is to set voltage bias and temperature conditions.

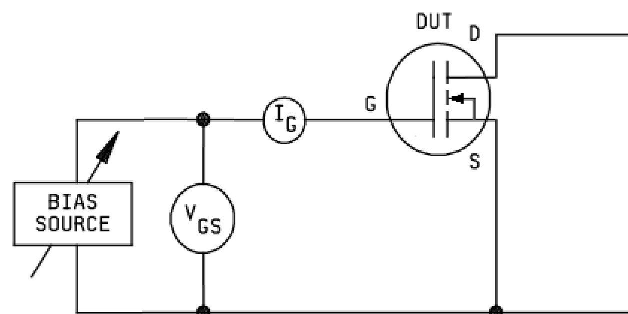

Figure 2.3: Test circuit for gate to source leakage current (I_{GSS}) measurement in Power n-MOSFETs.

After the V_{GS} voltage is configured, the current I_{GSS} can be measured. Frequently, this measurement is performed using positive and negative polarization.

In order to correctly perform the test, it is important to take into account the gate capacitance of power MOSFET. This capacitance determines a charge (or discharge) current during a transient condition. In order to assure that the gate leakage current is measured in steady state condition, a minimal charge (or discharge) time delay is required. Most of the actual instrumentation performs this delay time, automatically, under parametrization.

2.5.4 Threshold Voltage Measurement

Simple and historical definition considers the threshold voltage (V_{th}), in a traditional power MOSFET, as the gate to source voltage (V_{GS}) at which the drain current is comparable to the leakage current [90]. However, for modern MOSFET devices with complex cell structures and materials, this V_{th} definition has been revised considering a functional mode of the threshold voltage, which is the V_{GS} level needed by the MOSFET to move from weak to strong drain-to-source conduction state [91].

Due to threshold voltage constitutes a fundamental parameter for reliability assessment, several works about methods for the extraction of the V_{th} have been published in a decade, considering functional applicability in both crystalline and non-crystalline MOSFETs [91]–[99].

Many factors, as drain voltage, parasitic series resistance, electron mobility degradation and noise, can affect the determination of the threshold voltage. In fact, more advanced and complex methods for V_{th} extraction are focused on discarding mathematically this disturbs. Some of the more practiced and reported V_{th} extraction methods have been reviewed in [91], which are:

- Constant-Current (CC) method
- Match-Point (MP) method

- Linear-Extrapolation (LE) method
- Second-Derivative (SD) method
- Third-Derivative (TD) method
- Current-to-square-root-of-the-Transconductance Ratio (CsrTR) method
- Transition method
- Normalized Mutual Integral Difference (NMID) method
- Normalized Reciprocal H function (NRH) method
- Transconductance-to-Current-Ratio (TCR) method
- Reciprocal-H function (RH) method.

Continuously, in the methods above listed, the region of work in which the MOSFET is biased (linear or saturation) is considered for the V_{th} extraction. Some of the reported methods are widely used in industry because their simplicity of implementation. For instance, the CC method evaluates the V_{th} as the value of the V_{GS} corresponding to a predetermined, constant drain current I_D, while the V_{DS} is biased in linear or saturation region [12], [90], [98], [99]. Other widely used methods are Match-Point (MP) and Linear-Extrapolation (LE), being suitable to extract the V_{th} in the linear region. A common schematic circuit used to measure the V_{th} through the methods before listed is presented in Figure 2.4 for Power n-Channel MOSFETs. It is worth noting that two regulated power supplies are needed to reach the electric requirements of the measurement test. Thus, after bias conditions are applied to the device (a sweep voltage in gate-to-source terminals and a fixed voltage in drain-to-source terminals), measurement and storage of the electric current and voltages is performed. Once the measurement data has been collected, one of the extraction methods mentioned above can be applied.

Nevertheless, a variation of the CC method that uses a simple and practical circuit (see Figure 2.5) to perform on-the-fly measurements of the V_{th}, while the MOSFET is polarized in the saturation region, is also presented. This alternative method states the criteria I_D=3 $\cdot I_S$ (with I_S as the saturation current) at which the $V_{GS} = V_{th}$ [99]. The advantages of this alternative method are the usefulness of only a single adjustable power supply and the quick measurement process. In fact, direct measurement approach can be either a) punctual current bias (i. e. I_D=250 μA) and reading of the corresponding V_{th}, or b) voltage sweep until I_D reaches a certain value at which the V_{th} is caught. Even if the simplicity of this method, it gives a good approximation of the V_{th} which can be used as a first evaluation parameter during reliability tests.

2.5.5 On-Resistance Measurement

The test method to measure the static drain-to-source on-state resistance (R_{DSon}) is fully described in MIL-STD-750 (method 3421.1) [90]. This test is addressed to measure

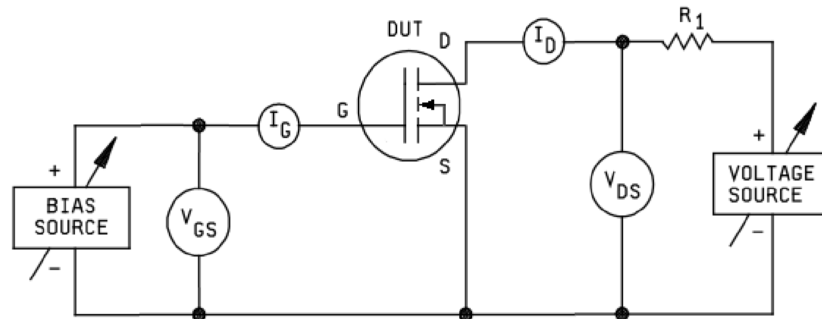

Figure 2.4: Test circuit for threshold voltage (V_{th}) measurement of Power n-Channel MOSFET.

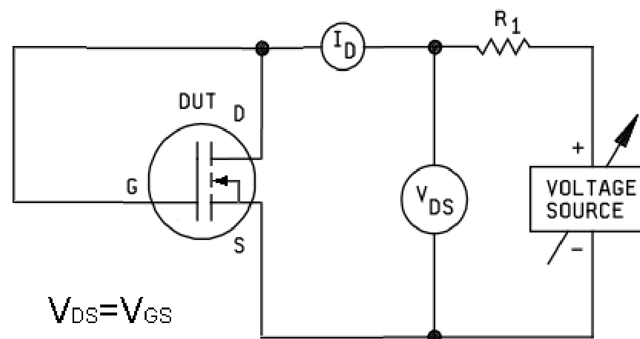

Figure 2.5: Test circuit for threshold voltage (V_{th}) test of Power n-Channel MOSFET using a single adjustable power supply.

the resistive path between drain and source terminals at specific bias and temperature conditions. Usually, a desired pulsed drain current I_D is set together with a particular constant V_{GS}. Once, the I_D has been reached, the V_{DS} is measured. Finally, the R_{DSon} is calculated as V_{DS}/I_D. The circuit schematic of the Figure 2.6 is suggested.

Regularly, this test is configured to make fast measurements (by punctual and/or pulsed biasing) to avoid self-heating on the DUT by the high current density involved when power MOSFET is tested.

Chapter Conclusions

Reliability is the property of a product to work continuously under the same conditions without experiencing a failure before of a specific time. In this chapter, concepts and definitions about the reliability of semiconductor devices have been reviewed. Due to the reliability of products can be evaluated through accelerated tests, several accel-

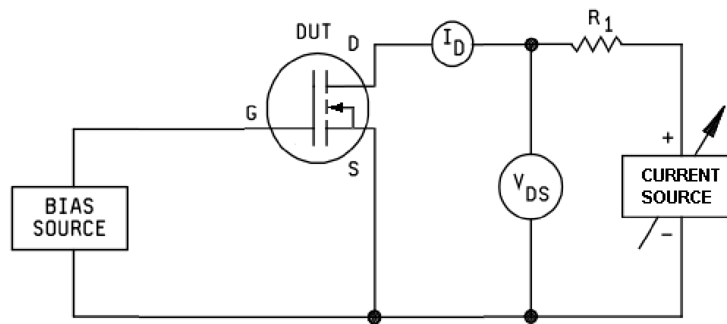

Figure 2.6: Test circuit for drain-to-source on-resistance (R_{DSon}) test of Power n-Channel MOSFET.

eration factors can be used to stress the semiconductor devices. The most widely used is temperature acceleration factor. In this way, accelerated tests are used to study the reliability and failure mechanisms in semiconductor devices, including power MOSFETs.

Semiconductor devices describe a life cycle characterized by a decreasing failure rate (λ) during the first hours of operation due to specific defects in the production processes. This early failures stage is followed by a constant λ, which is associated with random failures resulting from the stress test and specific failure mechanisms. Finally, last life stage of semiconductor devices is characterized the an increasing λ associated with the normal aging at the end of the lifetime of the DUTs.

Reliability methodologies and standards have been settled to guide the application of accelerated tests and reliability assessment in the semiconductor industry. Some reliability methodologies have been reviewed in this chapter, together to the widely accelerated tests used on power MOSFETs. Finally, methods and techniques for measurement of electrical characteristics of power MOSFETs, such as I_{DSS}, BV_{DSS}, I_{GSS}, R_{DSon} and V_{th} (which were treated in the first chapter), have been also reviewed using the standard MIL-STD-750 [90].

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Chapter 3

High Temperature Reverse Bias: Instrumentation Development

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ChapterHTRB

Since many decades, manufacturing of semiconductor devices has had to appeal at accelerated tests to determine the better design and processes for obtaining reliable devices and for qualifying products. As seen in the previous chapter, accelerated tests are intended to stress the DUTs making them work under worse than normal conditions, including higher temperatures, voltages/currents and humidity (some tests also consider radiation as a stress factor), to induce degradation and failures on DUTs in shorter time which otherwise would occur in several years of normal operation [100]. One of such accelerated tests is the High Temperature Reverse Bias (HTRB), which is oriented to stress the DUTs under high temperature and high reverse polarization to accelerate failures related to trapping mechanisms or materials integrity degradation [101]. DUTs involved in this test can vary from a single pn-junction diode until the more complex power devices [102]–[104].

In this chapter, a depth overview of HTRB test standard is provided, highlighting the main drawbacks arising from its traditional application in industry. An advanced HTRB methodology is proposed, which has been tested during the doctoral studies. In order to apply such a methodology, an experimental HTRB instrumentation has been developed. The latter was used to run the advanced HTRB test of power MOSFETs, whose results will be presented in the next chapter. Besides, its potentialities, handling thermal runaway problematic, violent failures events, individual temperature control among others, are also described. As reviewed in the last chapter, Electric Characterization Tests (ECTs) are important to determine the integrity of electronic devices. These ECTs consist on V_{th}, I_{DSS}, I_{GSS} and BV_{DSS} measurements. Therefore, the handling of the electrical interconnections for the ECTs of power MOSFETs is also presented.

3.1 HTRB standard technique

There are different standards to regulate the procedure application of the HTRB test. Main standards are MIL-STD-750D [90] and JESD22A-108D [105]. The former is oriented to qualify semiconductor devices for military applications while the second is used as a reference for commercial industry manufacturing. As early mentioned, HTRB test applies both electrical and thermal stress on DUTs, accelerating failure mechanisms such as those due to the presence of contaminants, mask misalignment, wrong diffusion, passivation problems and others [101]. In this way, using industrial instrumentation and thermal chambers, the temperature test is set into the range of 150-175°C, according to desired Acceleration Factor (A_F), which was described in the last chapter. However, higher test temperatures are required for emergent power MOSFETs technologies as $4\,H{-}SiC$.

For the voltage stress, MIL-STD-750D suggests that reverse bias shall be set at 80% of the BV_{DSS} of the DUTs; which must be polarized with gate terminal in off-state condition (see Figure 3.1) [90]. On the other hand, JESD22a-108 is not clear about the level of stress voltage [105], but it is an industrial testing convention to apply the same polarization level aforementioned. Moreover, in the electric schematic of the Figure 3.1, the resistor in series with the DUT avoids seeing all the DUTs as a unique system in case of failures. This rough solution has been well practiced during decades to avoid canceling the test by the failure of a single DUT, even when qualification standards do not accept failures [105].

Furthermore, in order to determine the HTRB test duration time, two ways can be followed. The first consists in determining the minimum test time (t_t) in function of the A_F and the expected operation lifetime of the devices in normal conditions work (t_u), by

$$t_t = \frac{t_u}{A_F}. \tag{3.1}$$

The second option is to apply suggestions from [90] and [105], which determine a maximum time of 1000 hours together with pre- and post-ECT of parameters devices.

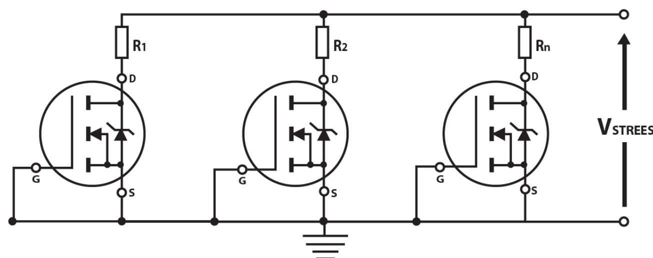

Figure 3.1: Electric schematic for the High Temperature Reverse Bias (HTRB) test on power MOSFETs.

However, inside the industrial manufacturing, the HTRB test time is divided into relative large time periods, applying interim ECTs at fixed test time, e.g. 168h, 500h and 1000h. In fact, most of the qualification standards describe specific details about this kind of test, such as the number of DUTs, maximum number of accepted failed DUTs, failure criteria, and others [106], [107].

3.2 Drawbacks of HTRB Instrumentation and Standards

Many reported works have made observations to main drawbacks of HTRB and the standards that regulate this test [101], [108], [109]. In effect, Green et al. [108] makes the observation that the application of existing reliability test standards, based on Silicon (Si) technology, to emergent technologies as Silicon Carbide (SiC) power MOSFETs qualification can in some cases result in ambiguous test results. However, some drawbacks, which are treated in this section, are related to manual operation and inconsistencies between the standards mentioned above.

Electric parameters of DUTs are measured at room temperature, before and after the stress test, to discard failed device. Besides, interim measurements are performed on the test, but these are not so frequently due to manual operation and long-time for cooling-down steps [80]. In fact, only JESD22A-108 standard [105] makes reference to a window time of maximum 96 hours to complete the interim measurements, but this specification does not consider the natural recovery process of degradation devices, which are particularly pronounced after long elapsed relax time of the DUTs. However, more complex industrial instrumentation has been developed for automation of reliability tests in the last years. Some of these instrumentations are smart power supplies, remote controlled switching matrix among others. This kind of instrumentation is useful to accelerate the ECTs measurement procedures, but this equipment has difficult accessibility because of their high prices, without mentioning that their designs lead to work with high DUTs densities, which for R&D laboratories is not beneficial.

Other drawbacks are the inconsistencies between standards related to the ECTs measurement procedures. For instance, JESD22A-108D [105] allows for electrical characterization tests at high temperature, but only after that the post stress room temperature

measurements have been performed. AEC-Q101 [106] does not describe this procedure at high temperature but requires that pre- and post-stress electrical measurements occur at room temperature. In this way, each manufacturer can determine the better reliability plan test for products qualification but these are not always the better for the reliability of devices under normal operation conditions. Hence, comparison of reliability data from different manufacturers is difficult.

On the other side, the determination of device failure criteria is another inconsistent problem between standards. For instance, the AEC standard explicitly establishes that device parameters remain within electrical test limits of the specification and within ± 20% of their pre-stress values to pass the test; but leakage currents cannot exceed five times their initial value. In this ambit, JEDEC and MIL-DoD standards do not have specifications about this. Even more, as mentioned before, the stress time duration and interim measurements time are not clearly determined in all the three standards.

More specifically, during a HTRB test, DUTs are placed on special boards that are entered into a thermal chamber. By thermal convention process, the only ambient temperature is controlled instead of the single device one. In fact, industrial thermal chambers are used to control the ambient temperature test, but the single device temperature is not controlled. Even more, the problematic of thermal runaway, which is related to the positive feedback between temperature device and leakage currents increment is not controlled nor detected during the HTRB test. Such kind of problem causes more accelerated failures because the temperature of the single DUT increases even higher than temperature test via its thermal runaway event, becoming greater than the others DUTs, leading to an inevitable early failure of such a device. Due to the presence of series protection resistors (see Figure 3.1), failed DUTs are not detected until the next interim ECT measurement, because of the serie resistor is burnt by the high current density during the failure, which is adding uncertainties to the real failure time within the test. However, in some cases the protection resistor continues to work, even when the devices have failed interfering with the remaining DUTs in test or leading the failed DUT into package explosion, which makes difficult the post-failure analysis.

Nevertheless, the power consumption of bulky instrumentation involved in HTRB testing is very high (around 6-10 KW only for thermal chamber operation). This high cost in power has its reason if the reliability of power semiconductor devices is ensuring. However, it is evident that innovative instrumentation that can do the same task but with less power consumption is challenging. Reaching this challenge is essential because usually High-Temperature Tests are performed during R&D phases in the manufacturing industries and the number of devices to be tested at this stage is limited, being always important the failure and stress information collected during the tests. In fact, there is a demand for smart instrumentation and systems for reliability testing capable of collecting relevant information during accelerated tests at lower power consumption as possible.

Finally, some specific drawbacks above commented are summarized as:

- Manual operation.

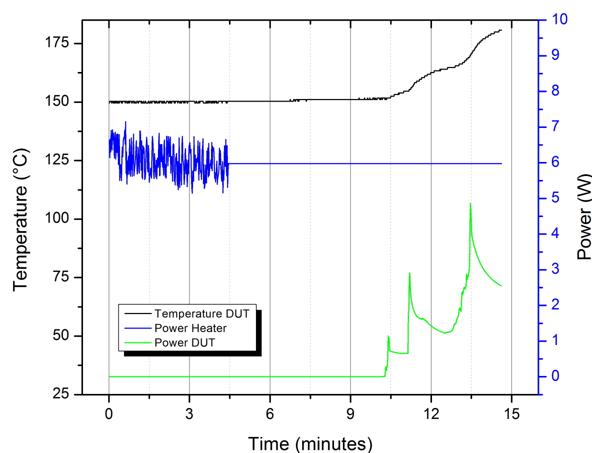

Figure 3.2: Thermal runaway triggered by the power loss dissipation (green line) increases the temperature of device (black line).

- Uncertainties related to real failure time.
- Ambient temperature control instead of the individual temperature device.
- Leakage currents and temperature of DUTs controlled in real time to avoid early failures due to a thermal runaway process.
- Wear compatibility of Si reliability standards with wide bandgap technology as SiC.
- High power consumption by bulky instrumentation.

3.2.1 Thermal Runaway

Electric parameters of semiconductor devices are well related with temperature operation as studied in the first chapter. Specifically, in power MOSFETs, the I_{DSS} is governed by the body leakage current, which proportionally changes with the junction temperature. As mentioned above, DUTs are reverse biased under off-state condition during a HTRB test while high temperature is applied. Such high temperature leads to an increment of the I_{DSS}, which will further increase in regions of high temperature, which are termed hotspots. These regions inside the power MOSFET die will get hotter, which again leads to more increased leakage current closing a positive feedback (See Figure 3.2).

If the high power loss density is not extracted by cooling or stopping the heating of the device during a HTRB, this could carry the DUT out to fail under thermal runaway mechanism. In this way, failure will not happen because of low reliability of the device in any power application but due to bad heating extraction systems. In fact, if the P_{gen} is the generated power density and P_{out} is the power density that can be maximally

extracted via the package and heat sinker, a condition for the thermal runaway can be expressed as [110]:

$$\frac{\partial P_{gen}}{\partial T} > \frac{\partial P_{out}}{\partial T}. \tag{3.2}$$

If this condition is fulfilled for a steady-state operation, a fast temperature increment in the device will occur as shown in the Figure 3.2. Usually, in standard instrumentation and procedure for HTRB, these kinds of failures cannot be detected nor avoided. Finally, the destruction of the device will be due to high temperature.

3.2.2 Uncertainties of Lifetime Estimation

When lifetime estimation is performed by mean of accelerated tests, the time elapsed before failure devices is an essential collection of data to determine the failure rate (λ) and others as MTTF and MTBF. After many hours of stress, the power MOSFETs can experience thermal runaway problems that lead to a higher activation energies induced by the uncontrolled increment of temperature device during the test.

Moreover, high thermal interfaces and non-independent temperature control per DUT can lead to temperature test of devices are well different than the required one. For instance, the test temperature in devices can be less than the setpoint and as consequences the acceleration factor (A_F) is less than that calculated for a certain temperature setpoint. The latter is not considered when reliability models for lifetime estimation are applied.

Furthermore, the long time elapsed between interim measurements avoid detecting failures in “real-time”. In fact, JESD22A-108D [105] suggests an exponential distribution in time of four interim measurements over the DUTs (including the pre- and post-stress characterization) as shown in the Figure 3.3. In this way, failure times registered for failed DUTs are not according with the exact moment when the DUTs failed.

All the last mentioned drawbacks are the main causes for uncertainties in the estimation of lifetime in power devices during reliability testing. A solution for the last drawback can be the customization of the time between interim measurements. Therefore, more frequent interim measurements could be performed based from a linear till customized distribution oriented to an accurate individuation of early and wearing failures. Obviously, it is evident that to reach this solution, automated instrumentation must be implemented because of the impractical case where operators must always be present during the total completion of the test due to manual operations for the interim measurements.

3.3 HTRB Innovative Methodology

As mentioned in the last section, thermal chambers used in standard HTRB tests do not implement individual temperature control over DUTs, which is a drawback to detect thermal runaway. Also, significant time elapsed for electrical characterization of DUTs after a stress period introduces uncertain on results, especially in new semiconductor

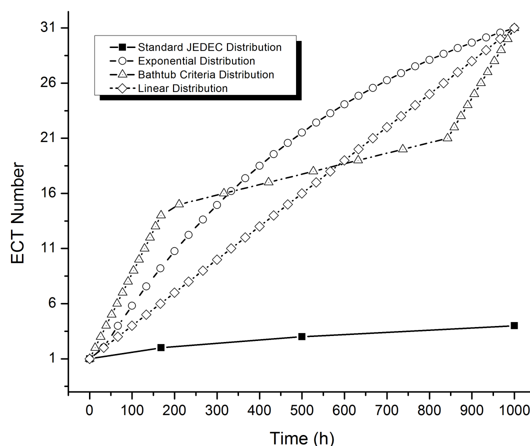

Figure 3.3: Examples of different interim electric measurements distribution into 1000h of HTRB test.

technologies, as mentioned in [108]. Also, even when failure data are collected during the seldom interim measurements steps because of traditional HTRB methodologies, it remains crucial regarding reliability analysis. The number of such measurements during a HTRB could be increased (Figure 3.3) with the support of automated instrumentation as that here reported. In this way, more measurement points give greater information about DUT degradation in time and about final failures.

Thanks to the instrumentation implemented during the thesis work, which will be detailed in the next sections, an alternative HTRB procedure has been experimented (see Figure 3.4). This proposed method divides the complex time of standard HTRB into several short time duration stress cycles. Furthermore, based on the capabilities of the implemented instrumentation, the proposed alternative HTRB methodology introduces a step called Electric Verification Test (EVT). This last is the same interim ECT but at a different temperature than room one, as also shown in Figure 3.4. In this way, interim measurement data can be gathered at operation temperature comparable to that one of general power electronic applications (e.g. 85-125°C), given better information about degradation processes that are evidenced at operating temperatures and not at room one. This suggestion can be favorable also to avoid significant waiting time for cooling DUTs to room temperature for the interim measurements due to the high thermal capacities of normal ovens used.

Also, a P_{Hth} parameter is defined in the instrument control environment. This parameter is used during the stress cycles to monitor each Temperature Control Module (TCM), detecting when the heating power drops below the P_{Hth} limit indicating the presence of significant self-heating in the respective DUT. In that case, an Emergency Electric Characterization Test (EECT) will be triggered, at the same temperature that EVT, automatically on the self-overheating DUT. On the other side, a I_{DSmax} is another parameter that could trigger an EECT overall DUTs. This event takes place when

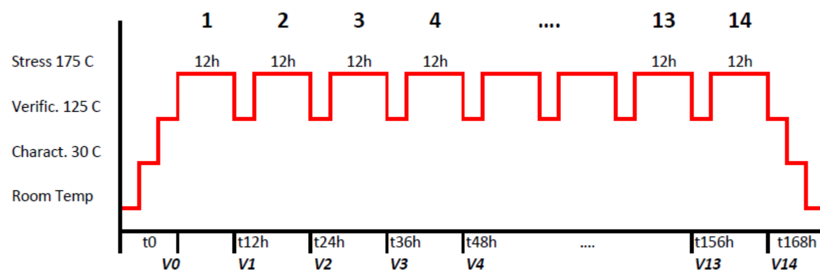

Figure 3.4: Proposed time scheduling for a 168h long HTRB test applying the reported alternative methodology.

anomalous leakage current increment appears in the total current monitored by the Source and Measuring Unit (SMU) during a stress cycle. In both cases, the system can identify the failed DUT (or strongly degraded DUT) and the thermal and electrical stress is stopped over the failed device, ensuring the test prosecution for the remaining DUTs and ensuring the possibility to practice well failure analyzes.

3.4 Innovative HTRB Instrumentation

As above mentioned, this section presents the implementation of an automated system capable of carrying out both thermal and electrical stress tests for HTRB of power transistors like MOSFETs. The proposed apparatus is resumed in the block diagram presented in the Figure 3.5. The overall system is controlled by a desktop computer, through an application developed by mean of $LabWindows^{TM}$-CVI from National Instruments (NI). The electrical connections between the DUTs and the SMU (Model 2410-C from Keithley Instruments Inc.) are realized by a Switch Matrix Module (SMM). TCMs locally control the temperature of each DUT individually. The computer application remotely controls the SMU with an IEEE-488 communication interface, while TCMs and SMMs communicate with a Master Communication Module (MCM) on an Inter-Integrated Circuit (I^2C) bus. Currently, a small prototype with six DUTs has been implemented for tests; however this modular architecture allows controlling up to 127 slaves because of the 7-bits addressing implemented by the I^2C communication protocol. The MCM communicates with the computer application by an Universal Serial Bus (USB) interface.

In this way, the system developed to carry out innovative HTRB methodology is composed of two parts:

- Hardware
  - Source and Measuring Unit (SMU)
  - Switch Matrix Module (SMM)
  - Temperature Control Module (TCM)

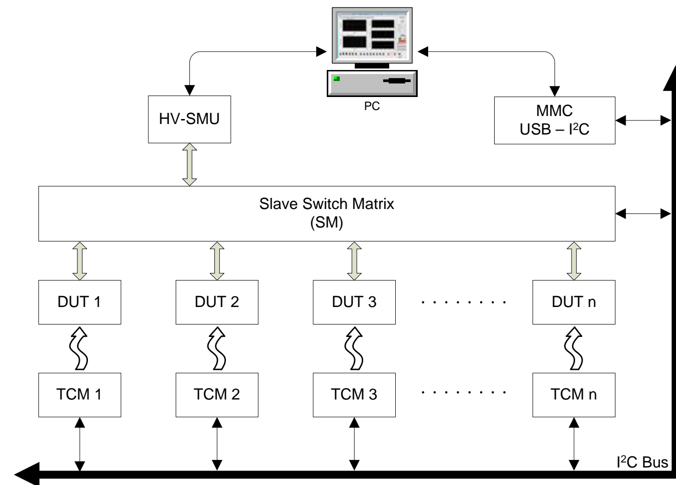

Figure 3.5: Block diagram of the proposed instrumentation for innovative HTRB tests.

  - Master Communication Module (MCM)

- Software

  - Instrumentation System Application for PC

3.4.1 Source Measurement Unit

A SMU is an instrument capable of biasing a programmable voltage/current level while it measures the respective voltage/current response. Modern SMU can be remotely programmed using communication interfaces such as Ethernet, USB, IEEE-485, COM among others. In the ambit of this work, the Keithley's 2410-C SMU instrument has been used. This instrument is designed specifically for test applications that demand tightly coupled sourcing and measurement oriented to characterization and production test applications. More detailed information can be found in [111]. However, key features of the Keithley's 2410-C SMU are listed below:

- Five instruments in one (IV Source, IVR Measure).
- Source and sink (4-quadrant) operation.
- Bias Voltage in the range from ±5uV to 1100V.
- Measurement voltage in the range ±1uV to 1100V.
- Current sourcing in the range of 10pA until 1A.
- Maximum Power Output: 20W.

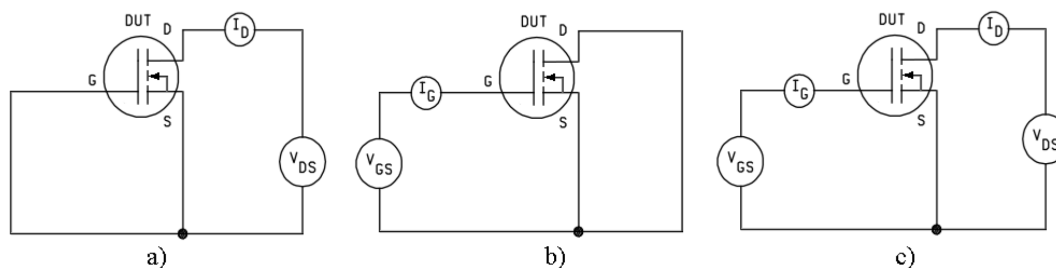

Figure 3.6: Circuital schematics used for measuring: a) Drain Leakage Current (I_{DSS}) & Breakdown Voltage (BV_{DSS}), b) Gate Leakage Current (I_{GSS}) and c) Threshold Voltage (V_{th}). Such measurements are performed during the Electric Characterization Tests (ECTs), Electric Verification Test (EVTs) and Emergency Characterization Test (EECTs) operations.

- 0.012% basic measure accuracy with 5½-digit resolution.
- 1700 readings/second at 4½ digits via General Purpose Interface Bus (GPIB).
- 2 and 4-wire remote V-source and V-measure sensing, 6-wire ohms mode.
- Standard Commands for Programmable Instrumentation (SCPI) via GPIB, RS-232, and Keithley Trigger Link interfaces.

3.4.2 Switch Matrix Module

During electric characterization of DUTs, the electrical connections must be reconfigured according to the measurement to be applied. In our case, measurements of I_{DSS}, BV_{DSS}, I_{GSS} and V_{th} are performed during the ECTs, EVTs and EECTs using the circuits whose schematics are shown in Figure 3.6 [90].

Due to several devices are tested during a HTRB, it is impractical to perform all the measurements by manual operation. Hence, automation of electrical interconnections is performed by exploiting switching matrix and control software. In this way, a SMM has been implemented according to the circuital schematic in Figure 3.7, where measurements of I_{DSS}, BV_{DSS}, I_{GSS} and V_{th} can be performed using only two relays. Furthermore, by applying the correct control sequence, the SMM can polarize the devices also for HTRB test according to the circuital schematic presented in Figure 3.8 and for eventual High Temperature Gate Bias (HTGB) tests. Firmware programmed in the SMM is simplified in the flow chart displayed in the Figure A.2 (Appendix A).

On the other hand, the Figure 3.9 presents a real view of the SMM implementation. The relay board *(a)* is controlled via a flat cable *(b)* by an 8-bit microcontroller (ATmega16) working as slave *(c)* using the I^{2}C protocol communication. Furthermore, this slave module also controls the “Security Lock”, which turns off the test in case the box cover is accidentally opened, preserving the integrity of the workers. Other extra tasks of this slave module are:

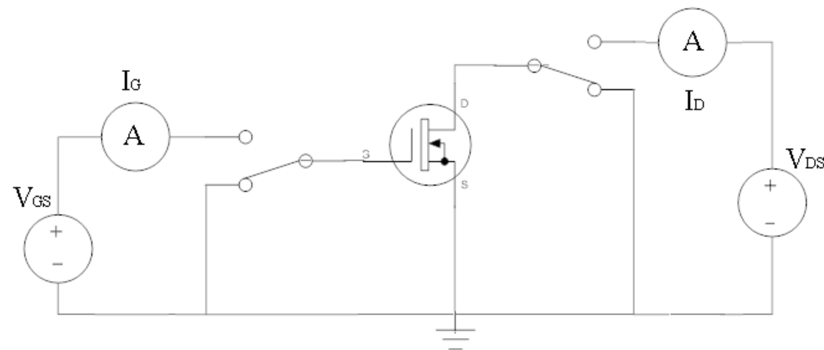

Figure 3.7: Circuital schematic of the system exploited for switching electrical interconnections during the ECTs, EVTs, EECTs, HTRB and HTGB tests: two-relays per every Device Under Test (DUT) have been used.

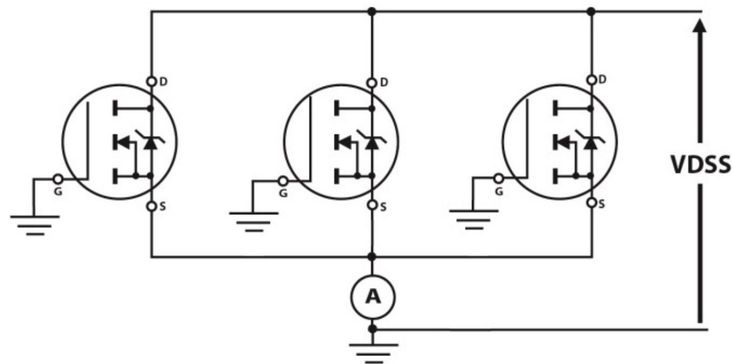

Figure 3.8: Alternative circuit schematic for the HTRB with the proposed instrumentation.

- Visual notification of high voltage presences.
- Main relay security for high voltage.
- Control of Fan for air-circulation during the cooling process.

3.4.3 Thermal Control Module

The TCM is a complex sub-system, which is described in the block diagram of the Figure 3.10. The TCM provides several functionalities, first of all, a Proportional Integrative Derivative (PID) controller, realized with an 8-bit microcontroller (Atmel AVR Atmega16). The PID controller acquires the case temperature of the DUT (with an integrated 10-bit Analog to Digital Converter (ADC) and generates 2 Pulse Width Modulation (PWM) control signals. After of filtering these signals, the first one is used

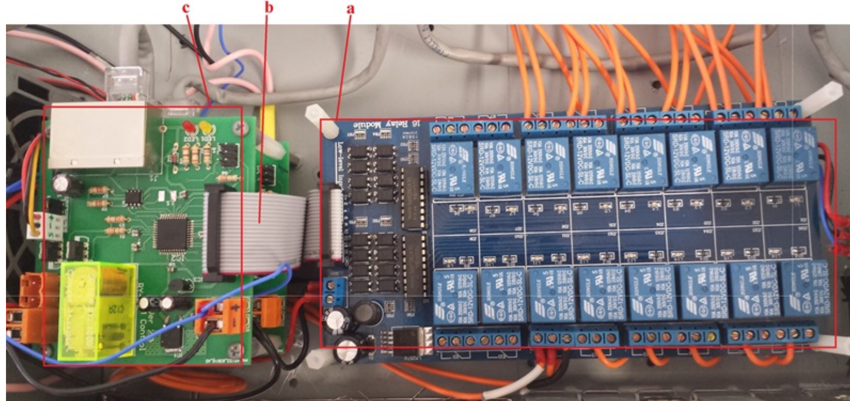

Figure 3.9: View of the SMM slave module: a) Commercial Relay Board, b) Flat-Cable connection and c) Prototype Board of the SMM.

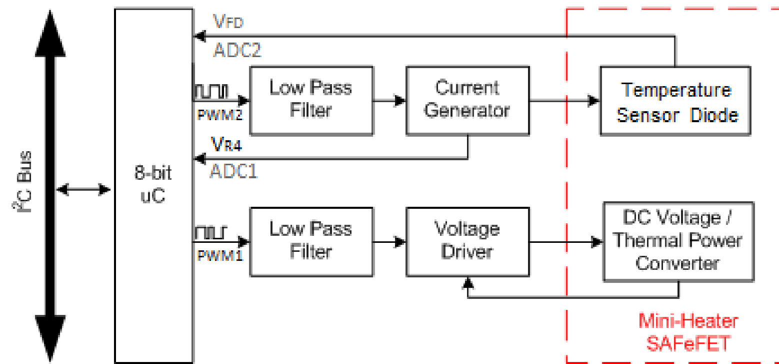

Figure 3.10: Block diagram of a single Thermal Control Module (TCM) developed for individually controlling the temperature of each DUT.

to bias the temperature sensor with a constant current while the second one sets the work point of the thermal actuator (heater). In Figure 3.11a, the view of the first Printed Circuit Board (PCB) prototype containing three TCMs is shown. As observed from the TCM block diagram (see Figure 3.10), the temperature sensor and thermal actuator parts are embedded into a single power device called the Surface Added Feature Field Effect Transistor (SAFeFET). However, in a second prototype of the TCM, a SiC power n-MOSFET was used as heater element together to an external temperature sensor. More details about these implementations are given below. To provide a good thermal conduction transfer from the power heater element to the DUT, a brass-sinker has been implemented (see Figure 3.11b), where both devices can be placed systematically on the top and bottom of the sinker (see Figure 3.11c). A detailed description of TCM implementation and work will be provided following.

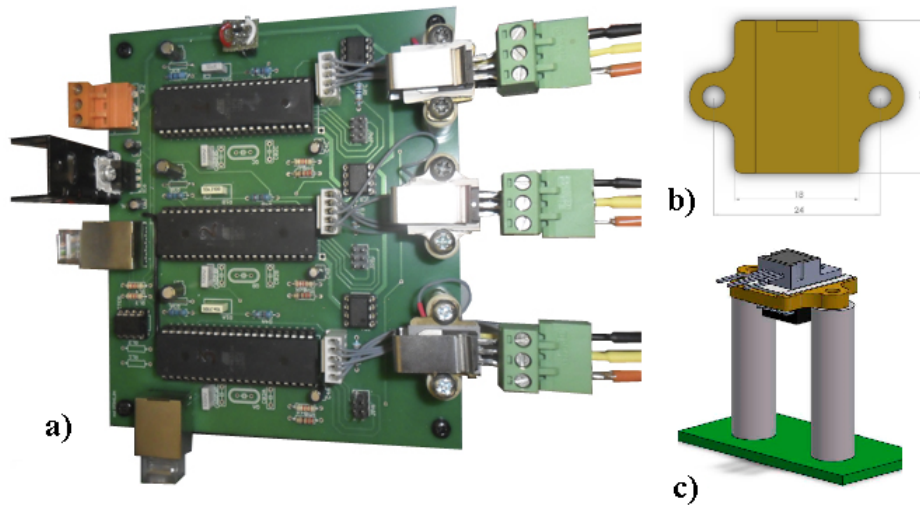

Figure 3.11: Thermal Control Module (TCM) physical implementation. a) First PCB prototype with 3 TCMs. b) Bottom view of the Brass-Sinker designed for the SAFeFET (Surface Added Featured Metal Oxide Semiconductor)-DUT placing. c) 3D view of the SAFeFET and DUT disposal.

Power Devices for Mini-Heater Implementation

Since power consumption (or losses) of any semiconductor device leads to heat dissipation, a power MOSFET can be set to work at different saturation levels controlling the V_{GS} applied to adjust the Q point operation (see Figure 3.12). Hence, sensing the temperature of the power device, a specific setpoint can be set adjusting the power dissipation of the device. The higher is the power dissipated, higher is the junction device device temperature, which can be sensed using a temperature sensor (i. e. a internal poly-Silicon diode array in the MOSFET die or an external passive temperature sensor).

As mentioned before, for the mini-heater implementation (see Figure 3.10), in a first stage, the SAFeFET has been used. In particular, the COTS STZ150NF55T has been used, which is available into a single P^2PAK package, and it is produced by STMicroelectronics [112]. An advantageous feature of SAFeFET is the integration of one array of poly-Silicon diodes that are electrically isolated from the power n-MOSFET, which is also contained into the same die as noted in Figure 3.13. Main electrical characteristics of SAFeFET are summarized in Table 3.1 [113], which were considered for the TCM implementation.

Furthermore, in a second prototype of the TCM module, a power SiC n-MOSFET of ST Microelectronics was used. In particular, the COTS SCT30N120 packaged in HIP247 from STMicroelectronics was used. This is a high power rated SiC MOSFET able to work at 200 °C of junction temperature and 1200 V of rated drain-to-source breakdown. The maximum power handling of this device is around 270 W. Regarding

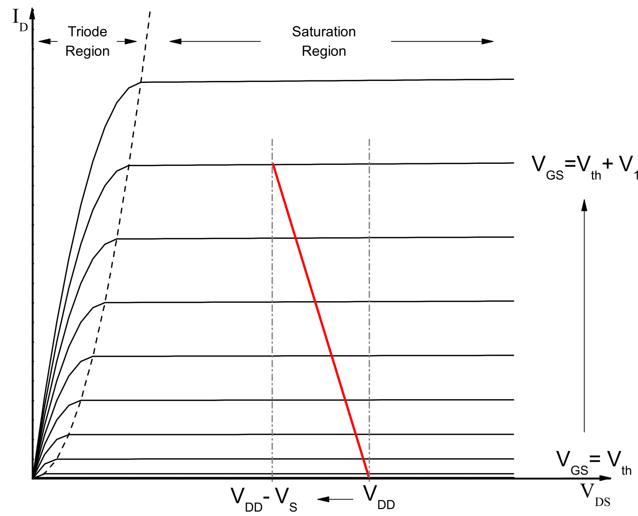

Figure 3.12: Symbolic I-V characteristic of the SAFeFET working for heating generation into the TCM (red line).

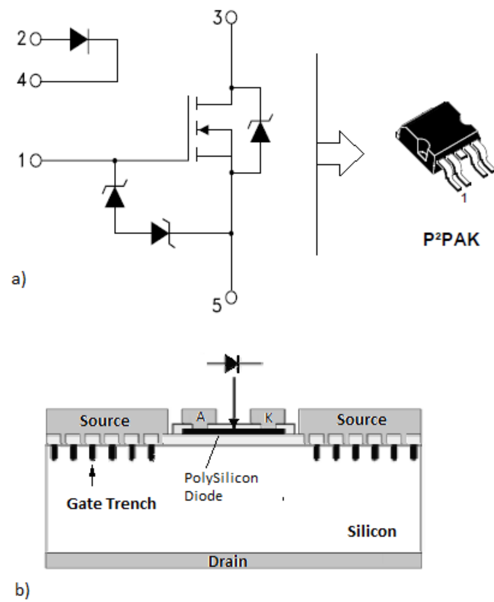

Figure 3.13: a) Electrical schematic of SAFeFET and the P^2PAK package. b) Cross-section view of the SAFeFET cell structure.

Table 3.1: Maximum Electrical Operation Conditions for STZ150NF55T (extracted from [113]).

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0)	55	V
V_{GS}	Gate-Source Voltage	±18	V
I_D	Drain Current (continuous)	40	A
P_{TOT}	Total Power Dissipation (T_C=25°C)	250	W
T_j	Operating Junction Temperature	-55 to 175	°C
V_F	Sense diode forward voltage (T_C=25°C & I_F=250uA)	3.5	V
dV_F/dT	Variability of forward voltage respect to temperature (I_F=250uA)	-6	mV/°C

Table 3.2: Maximum Electrical Operation Conditions for SCT30N120 (extracted from [114]).

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0)	1200	V
V_{GS}	Gate-Source Voltage	-10/+25	V
I_D	Drain Current (continuous)	45	A
P_{TOT}	Total Power Dissipation (T_C=25°C)	270	W
T_j	Operating Junction Temperature	-55 to 200	°C

the temperature sensing of the device, an external passive sensor must be used because the SiC power MOSFET does not implement any surface added feature or similar. Main electrical parameters of SCT30N120 are listed in Table 3.2. More details can be found in [114].

Therefore, mainly advantages of the SAFeFET and the SiC power MOSFET, when are used as mini-heater, are:

- For SAFeFET:
  - Smaller size, which avoids higher thermal capacitances.
  - Active temperature sensor included in the die.
- For SiC power MOSFET:
  - Higher temperatures operation.
  - Easier terminals connection.
  - Higher power dissipation.

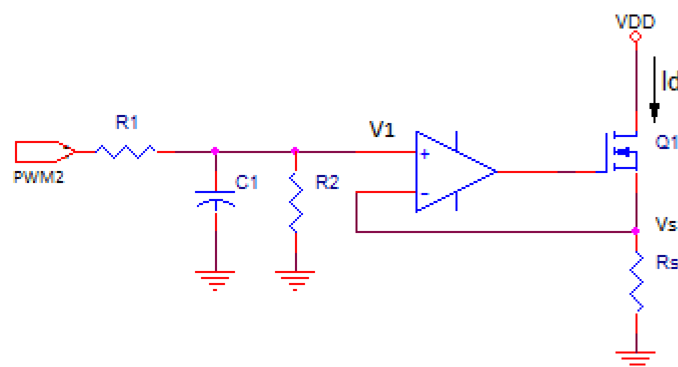

Figure 3.14: Electronic circuit schematic for heating generation using SAFeFET.

On-board Heating System

The electric functionality required for heating generation through the SAFeFET was presented in Figure 3.12. The red line represents the translations of Q-point operation MOSFET between different levels of I_D, which is controlled by small changes in the gate voltage bias given by $V_{GS} = V_{th} + V_1$. In Figure 3.14, the circuital schematic of the heater control system is shown: specifically, the PWM2 signal generated by the 8-bits microcontroller is reported. Combining information from Figures 3.12 and 3.14, it is noteworthy that V_{DS} is not a fixed value because, due to the feedback control circuit (see Figure 3.14), the bias changes according to $V_{DS} = V_{DD} - V_S$ where $V_S \approx V_1$.

Also, it is important to note that PWM2 signal is low pass filtered at $Fc \approx 7Hz$ (R1=2.2 KΩ and C1=10 uF) and attenuated by 20.8dB (due to the voltage divider between R1 and R2=220 Ω). These steps permit to extract an approximated DC level component (V_1), which represents the voltage setpoint for the Voltage/Current converter, formed by the Operational Amplifier (OpAmp) and power MOSFET. This voltage setpoint controls the flow of drain current (I_D) thanks to the feedback formed with the sensing resistance Rs=1 Ω. Due to the voltage divider formed by R1 and R2, the maximum setpoint voltage is limited to V_{1max} which leads to the maximum heating power (P_{Hmax}) dissipation on SAFeFET described as

$$P_{Hmax} = V_{DSmin} \cdot \frac{V_{1max}}{Rs} \tag{3.3}$$

where $V_{DSmin} = V_{DD} - V_{Smax}$ with $V_{Smax} \approx V_{1max}$, because of the feedback highlighted in Figure 3.14, resulting into

$$P_{Hmax} = \frac{(V_{DD} * V_{1max}) - {V_{1max}}^2}{Rs}. \tag{3.4}$$

After applying the above equations, two prototypes were implemented during the doctoral studies. The first one considered $V_{DD} = 24$ V and $V_{1max} = 0.45$ V, which led

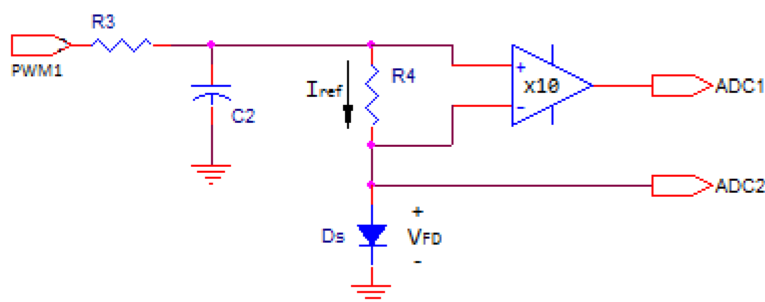

Figure 3.15: Electronic circuit schematic for temperature sensing using the internal SAFeFET Sensing Diode (D_s).

to a power consumption for heating P_{Hmax} = 10.6 W, reaching maximum temperatures of 175 °C easily using the SAFeFET. However, such operation temperature is critical for Silicon Technologies if these must work continuously for long time.

Therefore, as mentioned before, a second prototype was developed using a COTS SiC power MOSFET (SCT30N120 packaged in HIP247) provided again by STMicroelectronics. This prototype keeps V_{DD} = 24 V but increases V_{1max} = 0.65 V, which led to a higher power heating consumption of P_{Hmax} = 15.2 W and consequently a higher temperature of about 200°C. This prototype is even in functionality tests verification, but it is revealing itself as a robust and reliable system at higher temperature accelerated test.

Temperature Sensing Circuit

As mentioned before, two different prototypes of the TCM were performed. For the TCM with the SAFeFET device, the temperature sensing circuit is reported in Figure 3.15. A similar circuit is implemented for the TCM with the SiC power MOSFET, but the sensing diode (D_s) part is replaced by a Platinum variable resistor of 1000 Ω at 0ºC (PT1000 sensor), whose resistance value presents a positive and linear relation with temperature as detailed in [115]. In both cases, the PWM1 signal is used to bias these temperature sensors with a fixed reference current (I_{ref}), which is generated by the 8-bits microcontroller. In fact, changes in the temperature allow for proportional variation of the voltage drop of the sensors, which can be monitored to measure the temperature [116].

In this way, according to Figure 3.15, the PWM1 signal is low pass filtered at F_c≈1.25 Hz (with R3=2.7 kΩ and C2=47 μF) obtaining only a closely DC component. The duty cycle of PWM1 is continually adapted by the PID1 algorithm in the microcontroller to assure in R4=800 Ω a fixed drop voltage nearly to the setpoint for PID1. Such a setpoint value is stated in V_{R4}=200 mV for the TCM with the SAFeFET, while for the TCM with the SiC power MOSFET the V_{R4}=400 mV: as a consequence, the I_{ref} is fixed at 250 μA and 500 μA, respectively. In order to sense the voltage V_{R4}, which is

used for the PWM1 signal adjustments, differential A/D conversion (ADC1) is used in the microcontroller with the internal gain set to ×10. On the other hand, single A/D conversion (ADC2) is used to sense the V_{FD} (see Figure 3.15). Both ADC1 and ADC2 are performed at 10-bits of resolution, as is detailed in [117]. Since D_s is integrated with the power MOSFET in the same die, the junction temperature of the SAFeFET can be determined as

$$T_j = (\frac{V_{FD} - V_F}{\frac{\partial V_F}{\partial T}}) \tag{3.5}$$

where, V_{FD} is determined by real-time measurements as explained before, while V_F is the forward voltage of D_s at 25 °C and $\partial V_F / \partial T$ is the variability of the forward voltage with respect to the temperature determined at I_F=250 μA (see Table 3.1).

On the other side, the temperature measured by the PT1000 sensor can be extracted from the common expression that describes the Platinum resistance in function of the temperature R_T (for the range [0-850 °C]) as

$$R_T = R_0(1 + AT + BT^2), \tag{3.6}$$

with

$$A = 3.9080{\times}10^{-3}\ °C^{-1}$$
$$B = -5.775{\times}10^{-7}\ °C^{-2}$$

where R_0 is the resistance at *zero °C* of the Platinium sensor. In this way, monitoring the forward drop voltage in the PT1000 sensor (again signalled as V_{FD}) at a fixed $I_{ref} = 500\ \mu$A, the TCM can solve for $R_t = V_{FD}/I_{ref}$.

Discrete PID Controller

As will be seen in the next topic, a Proportional Integrative Derivative (PID) controller was programmed into the control firmware of the TCM microcontroller. A PID controller allows for the stabilization of a system without depth knowledge of the mathematic model that represents such system. In this way, the PID controller is based on an experimental tuning method, through the configuration of some constants, to give an output contribution for the process. Such contribution can be integrative, derivative or proportional. By definition, these three contributions are obtained separately, and then, algebraically added as shown in the block diagram of an analog PID controller of the Figure 3.16.

The transfer function of the PID controller presented in Figure 3.16 is

$$u(t) = K_p.e(t) + K_i \int_0^t e(t)dt + K_d \frac{de(t)}{dt}, \tag{3.7}$$

where:

- $u(t)$: It is the input to the process or the output of the controller.

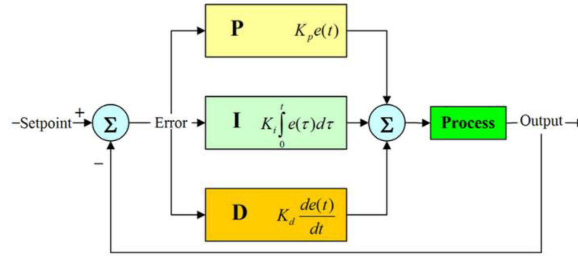

Figure 3.16: Block schematic of a Proportional Integrative Derivative (PID) controller for analogue signals.

- $e(t)$: It is the error signal.
- $K_p.e(t)$: It is the proportional contribution from the error signal.
- $K_i \int_0^t e(t)dt$: It is the integrative contribution, which recovers information from the past of the error signal until time t.
- $K_d \frac{de(t)}{dt}$: It is the derivative contribution, which is capable to anticipate the future of the error signal.

In the analog implementation of the PID controller, resistors R and capacitors C are used to design the proportional, integrative and derivative contributions; afterward, these are added by the analog electronic circuit. However, in the case of microcontrollers, which are capable of processing only discrete values, a discretization of the PID controller must be performed which can be implemented in software and simulations. In this way, for the discretization of the PID controller, again the three contributions will be treated separately and added at the end [118].

First, the error signal is considered as the difference between the reference signal $r(t)$ and the output of the process $s(t)$:

$$e(t) = r(t) - s(t). \tag{3.8}$$

The discretization of the error signal expression is given by

$$E(n) = R(n) - S(n). \tag{3.9}$$

Then, the discretization of the transfer function of the PID controller expressed in equation (3.7), considering that $t = nT$, becomes as

$$K_p.e(t) \approx K_p.E(n), \tag{3.10}$$

$$K_i \int_0^t e(t)dt \approx K_i \cdot T \sum_{k=0}^{n} E(k), \tag{3.11}$$

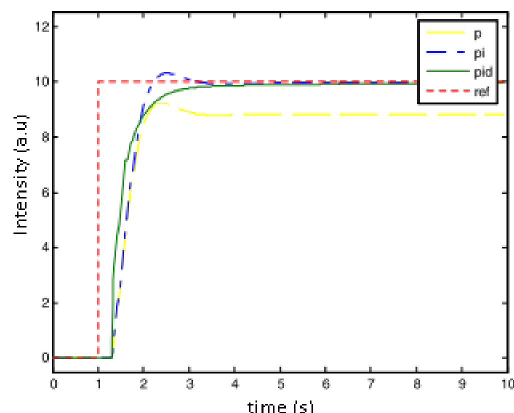

Figure 3.17: Typical PID regulator responses for step change in reference input from [23].

$$K_d \frac{de(t)}{dt} \approx K_d \frac{E(n) - E(n-1)}{T}, \tag{3.12}$$

where, n is the discrete step update at every time period T. Once the individual contributions have been discretized, the final discrete PID controller is given by

$$U(n) = K_p.E(n) + K_i \cdot T \sum_{k=0}^{n} E(k) + K_d \frac{E(n) - E(n-1)}{T}. \tag{3.13}$$

However, avoiding that changes in the desired process output make any unwanted fast changes in the control input due to the feedback, the discrete PID controller is improved when the derivative term is only based on the process output value [118]:

$$U(n) = K_p.E(n) + K_i \cdot T \sum_{k=0}^{n} E(k) + K_d \frac{S(n) - S(n-1)}{T}. \tag{3.14}$$

Results simulation from [118] are reported in Figure 3.17, where the typical PID regulator response to step change in the reference input is compared with the responses from only proportional and proportional-integrative controls.

Heating Temperature Control

Even though both heating and sensing electronic circuits were defined in the last sections, a third element is required to relate heating and sensing temperature. As was reported in block diagram of a single TCM developed, shown in the Figure 3.10, the mentioned third component is composed by a control algorithm, which is simplified in the flow chart of the Figure A.1 (Appendix A). Such a control firmware was developed and optimized for running on the 8bits-microcontroller AVR Atmega16 [117].

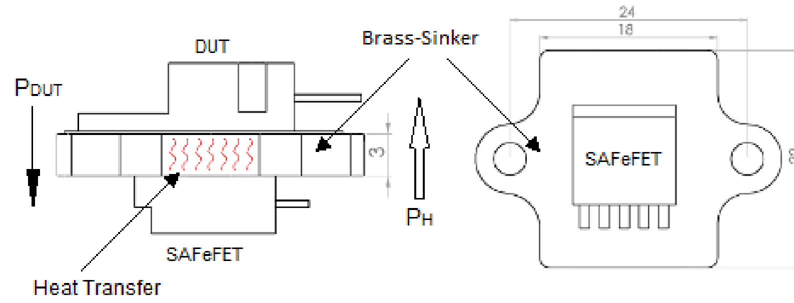

Figure 3.18: Schematic of the physical disposal of the SAFeFET (heater) and DUT on a Brass-Sinker sample holder.

The first task of the control firmware is the generation of a reference current I_{ref}, which is assured by the PID1 algorithm execution. In this way, PWM1 signal is continuously updated by PID1 to assure a particular drop voltage in R4 (see Figure 3.15), considering the setpoint SP_V_{R4} and voltage V_{R4}. This last is calculated as

$$V_{R4} = \frac{ADC1 * V_{ref}}{2^n * Gain}, \tag{3.15}$$

where, ADC1 is the A/D conversion data acquired, V_{ref} and n are the reference voltage and the number of bits for the A/D converter, respectively. The factor Gain=10 is used due to the temperature sensing circuit of the last section. Then, the I_{ref} is obtained by the Ohm's Law: $I_{ref} = V_{R4}/R4$.

Once the I_{ref} has been set by PID1, the diode forward voltage V_{FD} can be determined as

$$V_{FD} = \frac{ADC2 * V_{ref}}{2^n}, \tag{3.16}$$

where, ADC2 is the A/D conversion result from V_{FD} acquisition. Then, the T_j can be determined using equation (3.5).

On the other hand, heating power dissipated by SAFeFET can be determined by

$$P_H = P_{Hmax} * DC_R, \tag{3.17}$$

where, P_{Hmax} was defined by equation (3.4), and DC_R is the ratio between the duty cycle configured by the PID2 for the generation of the PWM2 signal and its maximum value (e.g. 500/1100). In this way, PWM2 signal is continuously updated by the PID2 algorithm to adjust the heating power (P_h) to keep constant the T_{DUT}. It is worth mentioning that the DUT is physically placed as shown in the schematic of the Figure 3.18. T_{DUT} is extrapolated from the T_j of the SAFeFET, using the linear fitting equations extracted from a thermal calibration process, which will be explained in the experimental section.

Table 3.3: Tuning Parameters used for PID1 and PID2 Controllers.

Symbol	Parameter	Value's PID1 I_{ref} Process	Value's PID2 T Process
K_p	Proportional factor	180	100
K_i	Integrative factor	0.1	0.4
K_d	Derivative factor	0.005	0.005
T	Period time for PID update	100ms	100ms
S_{max}	Maximum output PID value	1100	1100
S_{min}	Minimum output PID value	0	0
SP_1	Reference Setpoint for TCM's SAFeFET	0.2V	[25-175]°C
SP_2	Reference Setpoint for TCM's with PT1000 and SiC power MOSFET.	0.4V	[25-200]°C

Due to both PWM signal generation and A/D conversions are discrete processes, discrete PID controllers, reviewed in the last topic, were implemented in C language into the microcontroller firmware. Also, a windup control has been applied to limit the output value from the controller into a constrained range of the process work. In the Table 3.3, the tuning parameters for both PID1 and PID2 controller in the TCM are reported.

3.4.4 Master Module Communications

The MCM manages the communication between the computer application and the different slaves modules such as TCMs and SMMs. This communication module is necessary because of the slave modules recognizes only I^2C protocol, while the computer allows only for USB peripherals. In fact, into the MCM module, the protocols conversion sequence USB⇌UART⇌I^2C is performed for any in/out communication. The USB part is attended by the FTR232L chip, while the UART and I^2C are attended by the 8bits-microcontroller ATmega16 [117]. Also, several bus repeater chips (P82B96)are used to assure the signal quality of the I^2C into the system. In the Figure 3.19, a view of the MCM prototype board implementation is presented.

3.4.5 Instrumentation Management Computer Application

As initially mentioned, the instrumentation system developed in this work is managed by a computer application programmed in $LabWindows^{TM}$-CVI from NI. Such a user application allows the user for configuring tasks like electrical characterization, thermal control, electrical stress, data acquisition, data storage, failure criteria, real-time monitoring between others. A screen capture of the Graphical User Interface (GUI) programmed for the system application is presented in Figure 3.20. Since it is impractical

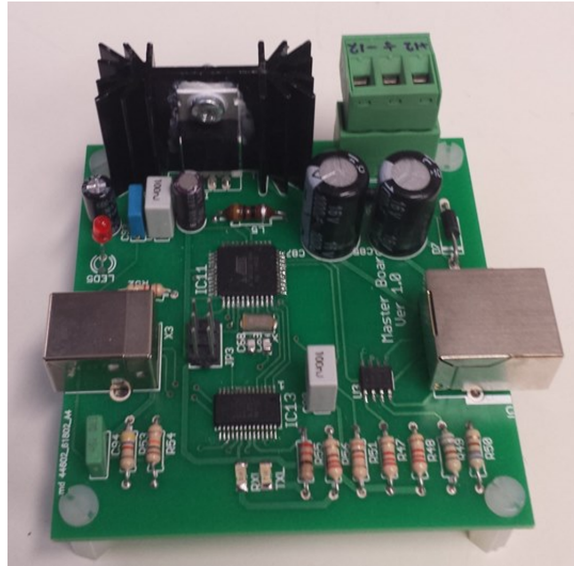

Figure 3.19: View of the Master Communication Module (MCM) prototype board implementation.

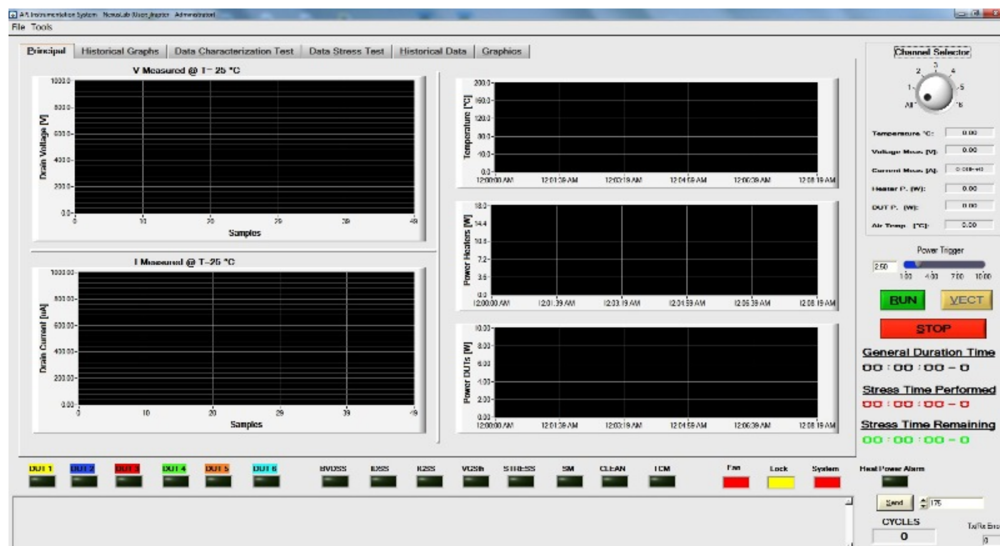

Figure 3.20: Screen capture of the control application Graphical User Interface (GUI).

presenting the complete code of the application, the Figure 3.21 presents a block diagram that summarize the main code elements, structures, and interactions that were programmed. It is worth noting that Multi-Threading programming was used in this work because of at least three priority process were running in parallel and interchanging critical state information about the DUTs, instrumentation, peripherals, and application.

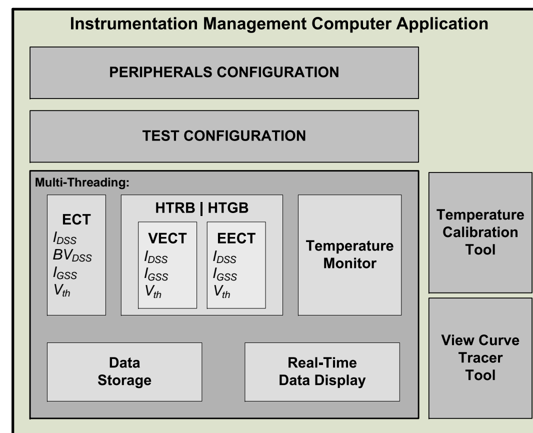

Figure 3.21: Block diagram of the software application for the HTRB instrumentation.

Chapter Conclusions

In this chapter, a depth analysis of the High Temperature Reverse Bias (HTRB) test was presented together with the international standards that give a guideline about this reliability test. Some annotations about main drawbacks of the manual operation and general thermal control performed on this test were reported. Some of such drawbacks are: long duration of interim measurements due to the extended time operation of cooling-down and heating-up the Devices Under Test (DUTs), thermal runaway, package explosion of failed devices, uncertainties on the true failure time of devices in a typical HTRB and demand of more quantitative and qualitative reliability data during the stress tests.

In contrast to such drawbacks, an advanced methodology and automated instrumentation for HTRB testing on power transistors was reported in this chapter. The individual DUT case temperature was controlled by a dedicated Thermal Control Module (TCM). Such TCM is based on the functionality of a Surface Added Feature Field Effect Transistor (SAFeFET) fabricated in Silicon (Si), which contains one power transistor and one diode for temperature junction sensing application. Thermal runaway (and then, catastrophic failures or package explosions) was prevented due to the individual regulation of the heating power for each DUT by the TCM operation. Furthermore, obtaining lower thermal capacitances in contrast with the traditional equipment, the instrumentation can change the DUT temperatures from 30-175 °C (and vice versa) in few minutes. All the DUTs are heated simultaneously (i.e. the heating and cooling phases have the same duration for six or more samples). All these features allow to propose a new methodology for the HTRB testing, based on the cyclic iteration of a stress and an electrical characterization phase. As a result, the data collected can reconstruct the progressive deterioration of the DUTs over the time.

Currently, the first prototype can test six samples per run. However, the modular architecture of the system allows for easy expansion to more test units, with little effort.

Electrical characterization and electrical stress are performed using a Source Measurement Unit (SMUs) Model 2410-C from Keithley Instruments Inc. This procedure is possible through the implementation of an internal Switch Matrix Modules (SMM), which permits changing electric interconnections between the power supply and the DUTs. A computer application, which was also developed during the doctoral studies, manages the instrumentation.

It is worth mentioning that the power SAFeFETs, employed in the TCMs, have been provided by STMicroelectronics, who has demonstrated a particular interest in the instrumentation and methodology developed. In fact, the last contribution from STMicroelectronics consisted in Silicon Carbide (SiC) power n-MOSFETs, which has allowed a significant upgrade of the instrumentation to reach stress temperatures until 200 °C with the help of Platinum resistors (PT1000) for temperature sensing. This upgrade is crucial for reliability study on devices based on new technologies, such as SiC, Gallium Nitride (GaN), Graphene among others.

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Chapter 4

High Temperature Reverse Bias: Experimentation

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The first prototype of the advanced HTRB instrumentation is shown is Figure 4.1. It was enabled to test simultaneously six DUTs using the power SAFeFET as the heating element for the TCMs. As mentioned in the last chapter, the SAFeFET has an internal diode, which is used as temperature sensor. On the other hand, the second prototype of the advanced HTRB instrumentation is presented in Figure 4.2. It is worth mentioning that this prototype uses power MOSFETs in SiC from STMicroelectronics (SCT30N120 packaged in HIP247) as heater element (inset of Figure 4.2). In this case, a Platinium resistor (PT1000) was used as temperature sensor. Also, in this last upgrade of the developed instrumentation, thermal isolation based in PTFE[1] sheets was implemented to avoid thermal power losses (see Figure 4.2).

Once the prototypes were assembled, a verification of the functionalities and temperature calibration were performed. These first stages of the experimentation are included

[1] Polytetrafluoroethylene (Teflon)

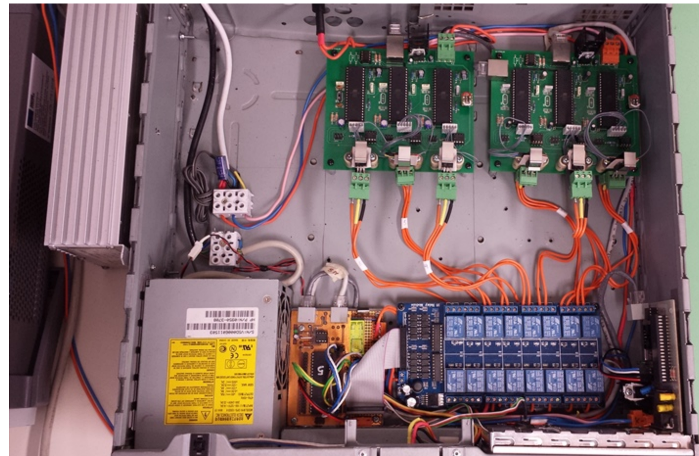


Figure 4.1: First prototype of the innovative HTRB instrumentation implemented with SAFeFETs to test 6 DUTs. Maximum temperature of test 175 °C.

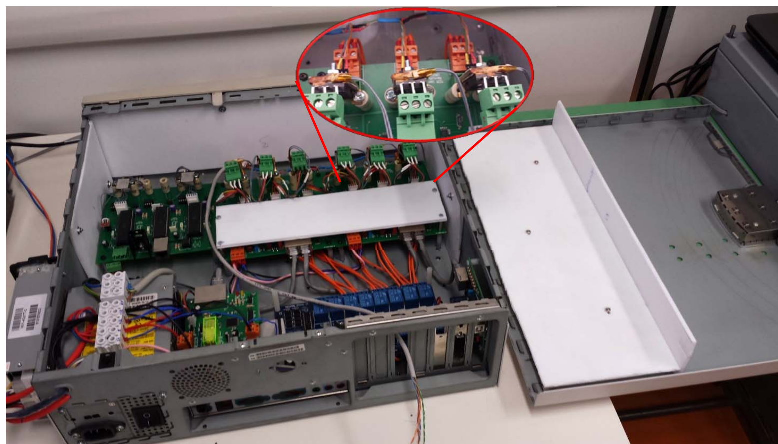


Figure 4.2: Second prototype of the innovative HTRB instrumentation implemented with SiC power MOSFETs to test 6 DUTs. Maximum temperature of test 200 °C.

in this chapter, and a practical demonstration of the control of thermal runaway of DUTs during HTRB test as well. The full instrumentation, during a test operation, is presented in Figure 4.3.

Afterward, several HTRB tests of different time duration have been carried out on COTS power MOSFETs in Si and SiC, which were provided by STMicroelectronics. In fact, the instrumentation here reported was also tested in the facility of ST Catania (IT), specifically in the Power Transistor Division (PTD) Group. Main results of such experiments and measurements are explained in the next sections.

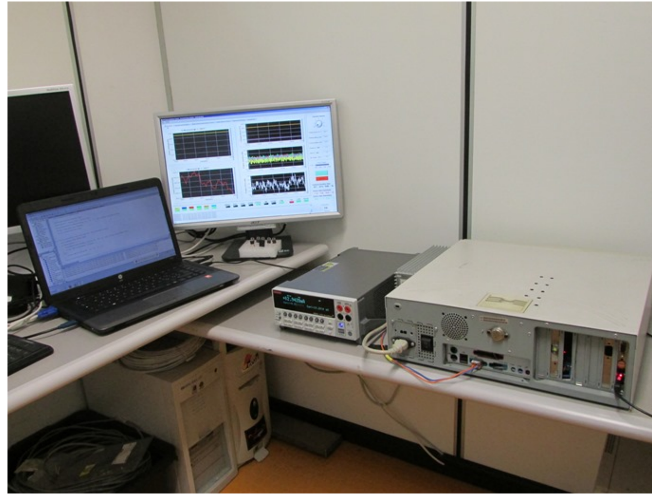


Figure 4.3: Innovative HTRB instrumentation setup.

4.1 Thermal Stabilization Time

The TCM is mainly aimed to heat an individual DUT at a temperature setpoint for accelerated tests or simply electrical characterization in temperature. As heat is transferred to DUT by thermal conduction flow, a settling time is necessary to stabilize the temperature on DUT to the desired setpoint. It is worth noting that the higher the setpoint the higher the settling time. TO determine the effective temperature applied to the DUT, a temperature sensor (LM35DT) with package TO220 was used to simulate a normal DUT during the validation of the thermal control process. In this way, the right DUT temperature was measured using the external sensor while a heating process is commanded using the worst case. The temperature of both the internal diode and LM35DT sensor were registered. In this way, TCMs were commanded to heat the DUTs (in this case the LM35DT) at 170°C. Then, temperatures registered were compared, as shown in Figure 4.4, to found the minimal settling time required to reach temperature stabilization in a closely value to the setpoint.

In Figure 4.4, the label "Error PID $<$ 1%" indicates the minimum level required to consider temperature stabilization. This condition (point T1) is reached by the heater after 90 seconds from the beginning of the heating process, but at the same time, LM35DT temperature is still growing due to the thermal capacitances between the heater and the DUT. However, the point T2 was considered to assume as stable the both trends, which means that a minimum time of 180 seconds is necessary to reach stabilization of temperature. However, also from Figure 4.4, it is evident that an adjustment is necessary to guaranty that DUT temperature (in this case LM35DT) is set in the desired setpoint, although this means that SAFeFET will work at a higher temperature. This temperature adjustment procedure is presented following.

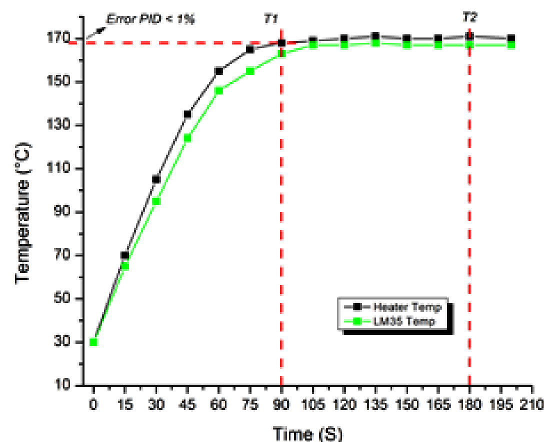


Figure 4.4: Comparison between temperatures measured from SAFeFET sensing diode Ds (Heater Temperature) and external sensor (LM35DT Temperature).

4.2 Temperature Extrapolation in TCMs

As above mentioned, it is necessary to adjust the temperature setpoint of the heater system in order to obtain the desired temperature of the DUT. Therefore, a relation between the actual DUT temperature and the set heater temperature is required for properly warming the DUT up during thermally accelerated tests, where the temperature of the sample must be kept as nearly as possible to setpoint during the complete test. To this purpose, results of linear fitting performed on measured temperature data, at different SAFeFET junction temperature setpoints, after 180 seconds of thermal stabilization time are presented in Figure 4.5. In fact, according to the results obtained by the linear fitting, only offset and slope values should be applied to extrapolate the DUT temperature (T_{DUT}) from SAFeFET junction temperature (T_j)(i.e. $T_{DUT} = 4.48661 + 0.92793 * T_j$).

In order to verify the result of such a calibration procedure, the temperature trend of both heaters was registered over time. For instance, LM35DT temperature sensors (enclosed in package TO-220) were used as DUTs in two TCMs with vertical and horizontal heater disposal. The registered temperature trends of the heater 2 and 3, before and after temperature calibration was applied, are shown in Figure 4.6. At the first glance, it seems that the temperature calibration adjusts the heat generation to the desired setpoint (e.g. 175 °C) of both heaters. Moreover, an approximated settling time can be collected from the temperature trends vs. time shown in Figure 4.6. A conservative settling time of 5 min. is suggested before starting whichever electrical or stress test at high temperature.

It is worth highlighting that the temperature calibration is performed each time a long-time accelerated test is performed, or the heater elements are replaced. A Thermal Adjustment Tool (TAT) was developed to automatize this procedure (see Figure 4.7), which automatically sends the fitting data parameters to every TCM. In fact, the fitting

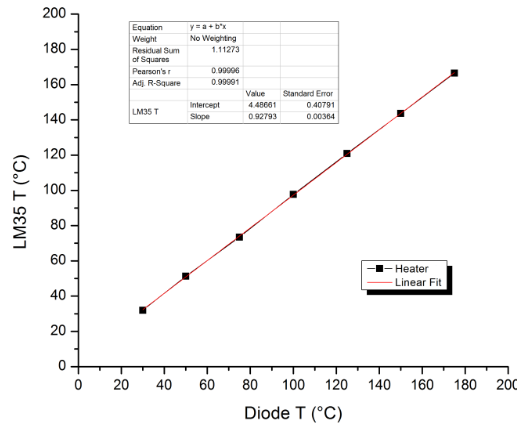


Figure 4.5: Linear Fitting of temperature measured on SAFeFET sensing diode (values in X-axis) and external sensor (LM35DT for Y-axis).

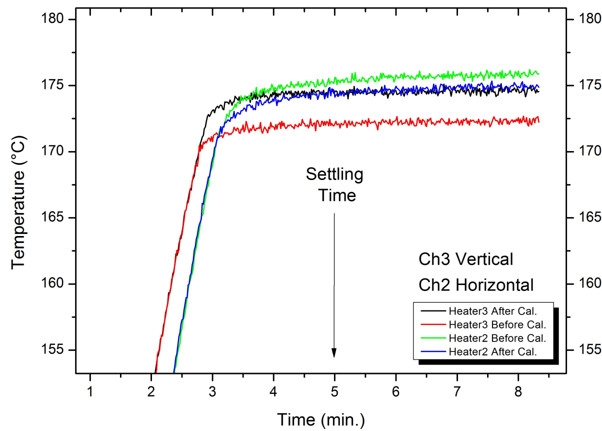


Figure 4.6: Measured temperature trends vs. time, of two different heater disposal, before and after the temperature calibration.

data are used by the TCMs each time the temperature control algorithm (treated in the last chapter) is executed achieving that T_{DUT} can reach its setpoint. This process was replicated for the prototype with power SiC MOSFETs as heater elements.

4.3 Experiment 1: Thermal Runaway Control

As mentioned in the last chapter, TCM was designed to heat samples during an accelerated test and, at the same time, to detect and control thermal runaway events. This functionality is possible adapting automatically the heating power dissipation of the SAFeFET (or power SiC MOSFET in the case of the second prototype) according

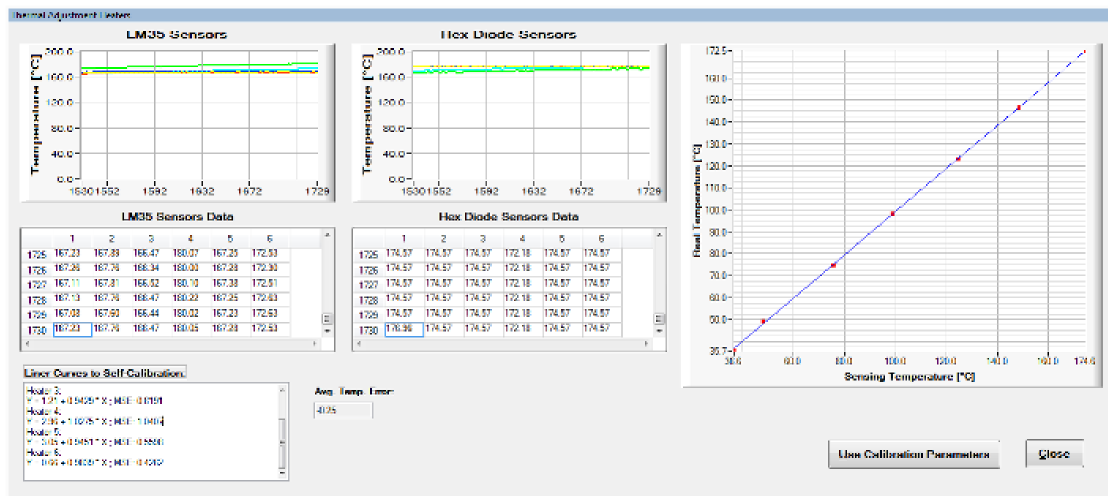


Figure 4.7: GUI of the Thermal Adjustment Tool (TAT) developed to automatize the T_{dut} calibration procedure.

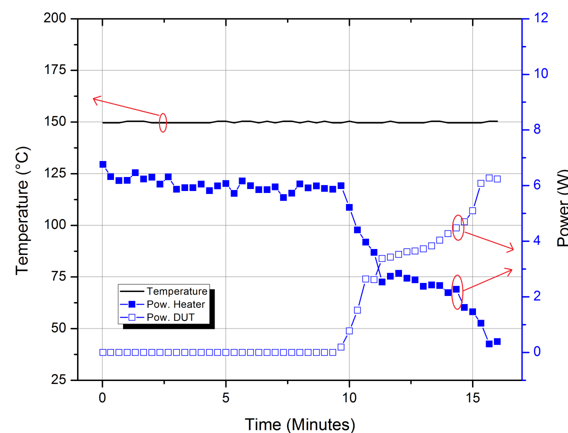


Figure 4.8: Detection and control of thermal runaway effect, over a DUT power transistor, performed by the TCM.

to the self-heating temperature generated from the loss power dissipation in a degraded DUT. Experimental results of an overstressing voltage accelerated test, practiced on a COTS power MOSFET using the TCM for temperature stress, are reported in Figure 4.8. It demonstrates that the TCM can effectively adapt its heating power (line with blue filled square symbols) to conserve the DUT temperature (black line) closely to the test temperature setpoint, which is affected by self-heating caused by the severe increment of the DUT power dissipation (line with blue square symbols).

Moreover, even if the power dissipation of the DUT increases because of the leakage current degradation, the temperature of the test for every DUT is controlled and settled

Table 4.1: Electrical parameters of devices involved during the first HTRB experimental test.

Parameter	Condition	Typical Value
BV_{DSS}	$V_{GS} = 0V$	>650V
I_{DSS}	$V_{GS} = 0V$ & $V_{DS} = 650V$ & $T_c = 25°C$	< 1uA
I_{DSS}	$V_{GS} = 0V$ & $V_{DS} = 650V$ & $T_c = 125°C$	<100uA
T_{jmax}		150°C

within an error $< 1\%$. Obviously, it must point out that the DUT is in degradation of its electrical parameters, and it is going into inevitable failure, but a localized higher temperature will not accelerate the failure event because of the control of thermal runaway. As a result, certain time failures are collected, and effects of not over-accelerated stress test can be analyzed in the post-failure phase.

4.4 Experiment 2:HTRB on 650V $MDmesh^{TM}$-V Power Si n-MOSFETs

This section exposes the results reported in [109]. Experimental measurements were divided into two parts. The first one was performed to prove that the new HTRB methodology and instrumentation is capable of wearing out power devices, and for this aim, stress parameters were oversized in a controlled manner. Devices involved in the test were COTS $MDmesh^{TM}$-V 650V Power n-MOSFETs, encapsulated in a TO220 plastic package manufactured by STMicroelectronics. Main electrical characteristics extracted from the datasheet are resumed in Table 4.1.

Using ECTs at T=40 °C, experimental BV_{DSS} of the DUTs was determined. In the Table 4.2, the result measurements from initial and final ECTs for I_{DSS} (at different V_{DS} bias level) and BV_{DSS} are summarized. Afterwards, the stress voltage ($V_{DS(stress)}$) was set according to the following relation:

$$V_{DS(stress)} = \frac{BV_{DSS(Th)} + \overline{BV_{DSS(Ex)}}}{2}$$

where, $BV_{DSS(Th)}$ is the datasheet value for the breakdown voltage given in Table 4.1 and $\overline{BV_{DSS(Ex)}}$ is the average of experimental breakdown voltage values measured in the initial characterization of DUTs (at $I_{DS} = 1mA$). Specifically, the set $V_{DS(stress)}$ was higher than the $BV_{DSS(Th)}$ in order to make a greater degradation of DUTs into a shorter time than the standard HTRB test, but sufficiently lower than $\overline{BV_{DSS(Ex)}}$ avoiding an uncontrolled overstress situation.

Once that $V_{DS(stress)}$=691 V was set, a temperature of 175 °C was programmed for the thermal stress task. The total stress duration was 210 hours, divided into 1-hour cycles. ECTs were performed between cycles at 125 °C according to the methodology

Table 4.2: ECT results (before and after stress test) for power n-MOSFET involved in the second experiment.

Parameter	DUT 1		DUT 2		DUT 3	
	Initial	Final	Initial	Final	Initial	Final
$I_{DSS}{}^{*}$ @ $50\%^{\dagger}$ $[nA]$	11.21	18.28	13.66	19.33	9.66	12.30
$I_{DSS}{}^{*}$ @ $80\%^{\dagger}$ $[nA]$	11.37	31.34	12.41	41.45	11.76	13.93
$I_{DSS}{}^{*}$ @ $100\%^{\dagger}$ $[nA]$	15.29	148.89	15.29	173.31	13.39	15.33
$BV_{DSS(Ex)}{}^{*}$ @ $I_{DS} = 1mA$ $[nA]$	718.89	718.89	745.41	741.72	724.54	731.16

$*$ @ $V_{GS} = 0V; T_{DUT} = 40°C.$

$\dagger$ *Percentage of* $BV_{DSS(Th)}$.

Table 4.3: Normalized percentage variations of I_{DSS} and BV_{DSS} for DUTs stressed.

Parameter	DUT 1	DUT 2	DUT 3
ΔI_{DSS} @ 50% $BV_{DSS(Th)}$	0.63	0.42	0.27
ΔI_{DSS} @ 80% $BV_{DSS(Th)}$	1.76	2.34	0.18
ΔI_{DSS} @ 100% $BV_{DSS(Th)}$	8.74	10.33	0.14
ΔBV_{DSS} @ $I_{DS} = 1mA$	0.0	4.95E-3	9.14E-3

proposed in this work. Historical evolution of the I_{DSS} is presented in Figure 4.9, which reveals the DUTs degradation along the test. As mentioned before, since leakage current is measured continuously during the stress test, the system can identify whether an anomalous current growth is happening and it can trigger an ECT to identify the failing device in order to turn it off while the test of the remaining DUTs continues running. Final ECT was performed at the end of stress test (see Table 4.2) at the same thermal and electrical conditions as the first one. A graphical comparison between I_{DSS} curves obtained from both initial and final ECT in DUT1 is displayed in Figure 4.10. Also, Table 4.3 summarizes the degradation in terms of normalized percentage variation of leakage current ($\Delta I_{DSS} = (I_{DSS_{final}} - I_{DSS_{initial}})/I_{DSS_{initial}}$) at different levels of V_{DS} performed using the data from Table 4.2. It is worth noting that marked electrical degradation is evident on DUT1 and DUT2.

During the second part of the experiment, a customized test was programmed for electrically and thermally stressing the DUTs in a similar manner of the JESD22A-108D [105] standard procedure for HTRB, but with a time duration of 4.5 hours. Again, COTS devices involved were p-MOSFETs with $B_{VDSS(Th)}$=600 V. Only two devices were stressed at 175 °C and 80% of its $B_{VDSS(Th)}$. The first device was stressed continuously, while the second device was stressed in 45 minutes cycles, performing ECTs at T = 40 °C at the end of each cycle. Figure 4.11 shows the I_{DSS} trend during this short time HTRB stress test (ECT measurement time is subtracted): specifically, the

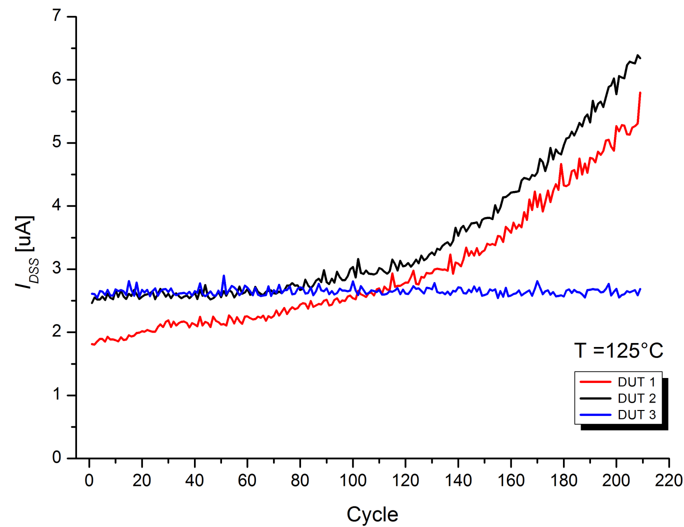
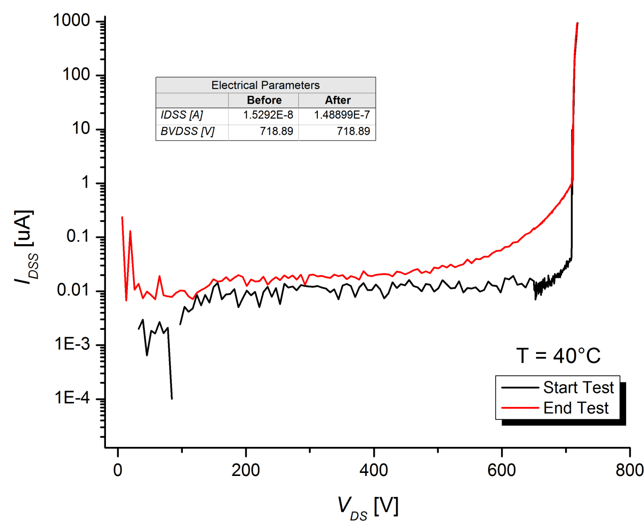


Figure 4.9: I_{DSS} data measured via interim ECT along stress test on DUTs at $V_{DS} = 650V$ and $T_{DUT} = 125°C$.



Electrical Parameters		
	Before	**After**
IDSS [A]	1.5292E-8	1.48899E-7
BVDSS [V]	718.89	718.89

Figure 4.10: Comparison between I_{DSS} curves measured before and after the stress test on DUT1 (power n-MOSFET).

I_{DSS} was measured at the stress temperature. Even when leakage current values of devices are different because of the very low probability of finding two completely identical devices, the leakage current grows continuously and with the same trend for both devices. The authors in [109] concluded that through a significant set of experiments, the methodology and instrumentation proposed could be validated to be adopted as an alternative standard for HTRB test. Also, reliable data, comparable with those obtained

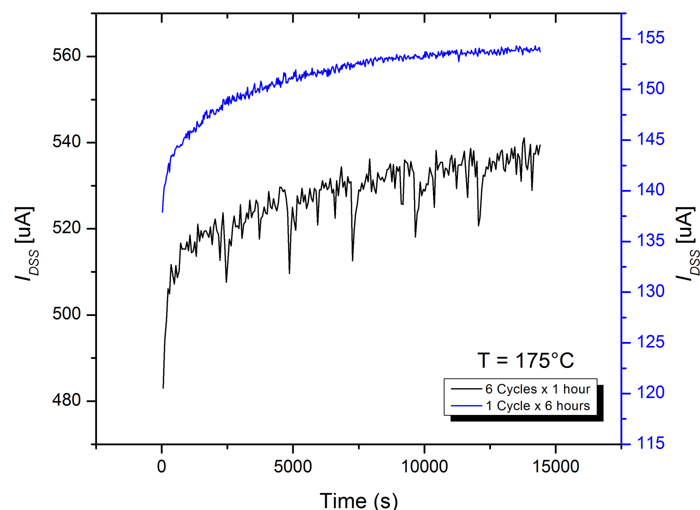


Figure 4.11: Comparison of I_{DSS} trends of two different p-MOSFET DUTs stressed continously (blue line) and by cycle (black line).

in long-time HTRB standard test [90], [105], are obtained with the instrumentation and methodology also concluding that more and frequent interim ECTs during stress test do not affect the degradation trend of DUTs.

4.5 Experiment 3: HTRB on 650V Super Junction Power Si n-MOSFETs

Results contained in this section were reported in [101]. In that work, the methodology and instrumentation for innovative HTRB were used for performing many single stress cycles with the same short time duration. After each cycle, an ECT test was performed to monitor the degradation status of the devices. In this case, 6 COTS Super Junction High Voltage power n-MOSFETs from STMicroelectronics, which are housed in TO-220 package, were tested. Two different sets of measurements were performed. As first step, BV_{DSS} and I_{DSS} electrical parameters of the devices were measured at T_{DUT}=30°C (see Table 4.4). Two groups of stress tests were performed as detailed in Table 4.4. Afterward, main stress parameters together with the failure criteria were defined in Table 4.5.

On the one hand, the test run 1 was scheduled to obtain a constant number of samples for every stress cycle (see Figure 4.12). This approach is achieved by implementing four stress cycles followed by ECTs at 125 °C to check the state of the electrical features of DUTs. Total I_{DSS} trend during the stress cycles is shown in Figure 4.13. As a result of the first run, DUT1 and DUT3 failed during stress test (see Figure 4.13), and as consequence these DUTs were thermal and electrical isolated automatically by the instrumentation. As evidenced in Figure 4.13, even when the loss power dissipation

Table 4.4: Electrical Parameters at $T_{DUT} = 30°C$ measured before and after the HTRB stress test on power n-MOSFETs with percentage variation of BV_{DSS} and I_{DSS}

DUT	Test Run	Initial BV_{DSS} [V] @ $I_{DSS} = 1mA$	Initial I_{DSS} [nA] @ $V_{DS} = 650V$	Final BV_{DSS} [V] @ $I_{DSS} = 1mA$	Final I_{DSS} [nA] @ $V_{DS} = 650V$	$\%\Delta BV_{DSS}$	$\%\Delta I_{DSS}$
1	1	663.16	11.125	—	—	—	—
2	1	663.90	9.6271	673.72	9.16	1.48	-4.89
3	1	664.88	11.049	—	—	—	—
4	2	668.38	8.6734	667.09	9.06	-0.19	4.45
5	2	660.46	9.3880	675.43	10.9	2.27	15.71
6	2	679.36	8.7686	678.14	9.41	-0.18	7.34

Table 4.5: Stress test and failure criteria parameters configured during the third experiment.

Parameter	Value	Observation
Time Duration Stress	55 Hours	Time divided in 5 and 11 cycles for test run 1 and 2, respectively.
Stress Voltage V_{DS}	650 V	100% of BV_{DSS} of the datasheet.
Stress Temperature	175 °C	Max. T_j of DUTs: 150 °C.
Interim VECTs Temperature	125 °C	ECT performed every stress cycle.
Max. I_{DSS} @ $V_{DS} = 650V; T_{DUT} = 125řC$	100 uA	Failure criteria parameter compared in each ECT.
Min. BV_{DSS} @ $I_{DS} = 1mA; T_{DUT} = 125řC$	650 V	

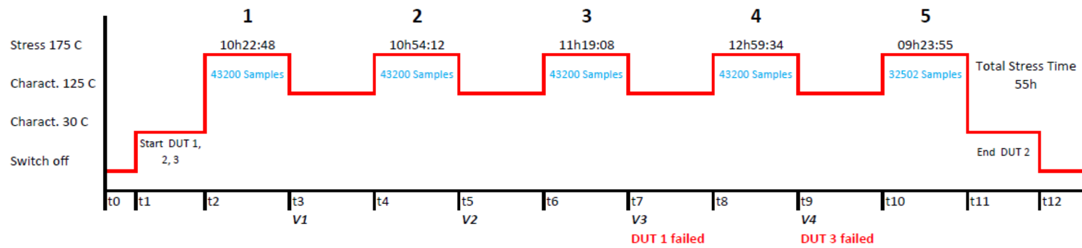


Figure 4.12: Scheduled cycles approach for advanced HTRB test run 1.

increased due to the failed DUTs, the temperature remained quite stable.

On the other hand, the test run 2 was scheduled to perform a stress process with constant cycle's time as shown in Figure 4.14. During this test run, 12 ECTs at T=125°C were performed to detect failures according to the criteria of Table 4.5. Results in term of total I_{DSS} degradation trend during the stress are shown in Figure 4.15. No failures were observed even if the leakage current increased a bit.

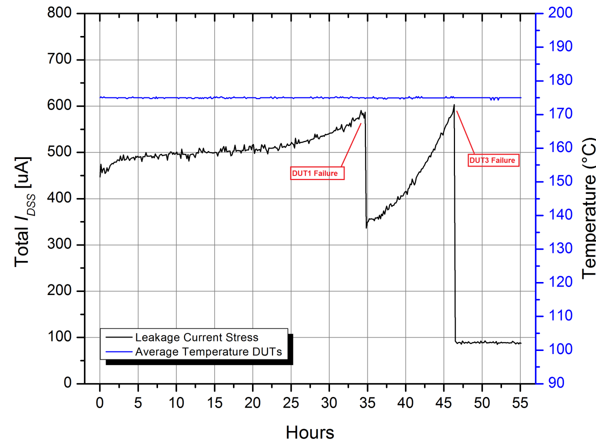


Figure 4.13: Total I_{DSS} trend at T=175°C measured on the DUTs during the test run 1.

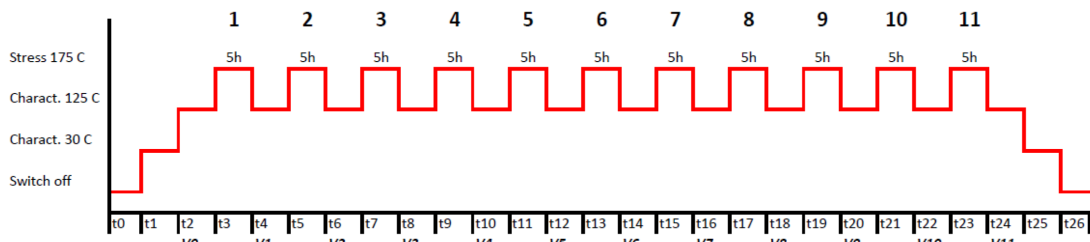


Figure 4.14: Scheduled cycles approach for advanced HTRB test run 2.

About the failed DUTs, Figure 4.16 shows the I-V curves achieved for DUT1 tested during the different four steps stress of the test run 1. In order to complete the analysis, the Table 4.4 also shows the ECTs measurements performed at 30°C at the end of the total stress test to evaluate the parameters degradation monitored. Also, the percentage variation of the BV_{DSS} and I_{DSS} parameters of the survived DUTs is shown.

Authors in [101] conclude that automated instrumentation for HTRB test, together with the advanced methodology proposed, allows to split the time to stress in many cycles of a single short period of the same time duration or samples acquisition. For each of these periods, it is possible to implement the classical interim measurements of the main electrical parameters on the DUTs to evaluate the degradation trend of the devices. Furthermore, it is possible even to estimate the cumulative damages produced during the stress.

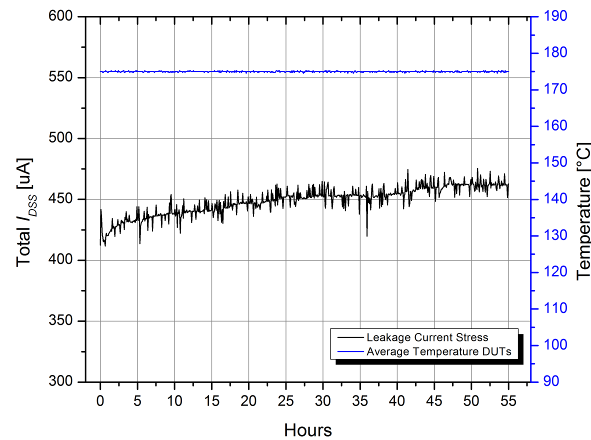


Figure 4.15: Total I_{DSS} trend at T=175°C measured on the DUTs during the test run 2.

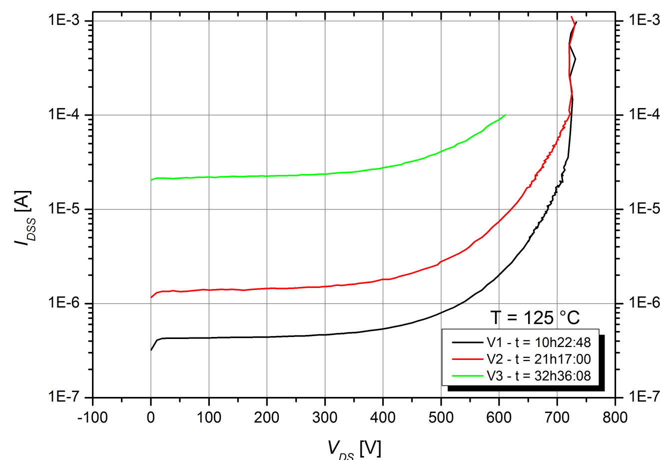


Figure 4.16: I-V curves for I_{DSS} measurements on DUT1 at T=125°C until failure was detected (green line) with interim ECTs.

4.6 Experiment 4: HTRB on $MDmesh^{TM}$ 550V Power Si n-MOSFETs

In order to test the instrument operation through a long stress test, 20 COTS power n-MOSFETs (also from STMicroelectronics) were characterized regarding the I_{DSS} and BV_{DSS} at room temperature. Based on the results obtained, six samples (named DUT 1 to 6) were selected to obtain an experimental BV_{DSS} as uniform as possible (see Table 4.6). In fact, this electrical parameter can have an enormous lot-to-lot variance. Also, two of the former devices were sacrificed to tune the stress conditions (thermal and electrical) in order to observe at least one failure during the HTRB stress test (see Table

Table 4.6: Electric parameters (at 25°C) of selected 6 power n-MOSFET involved in the fourth experiment.

Device ID	BV_{DSS} [V] @ $I_{DSS} = 1mA$	I_{DSS} [nA] @ $V_{DS} = 550V$	DUT #	Process
19	635.73	8.63	—	Sacrificed
09	635.88	8.61	—	Sacrificed
11	636.85	8.42	2	Stressed
15	637.27	8.62	6	Stressed
20	637.52	8.58	1	Stressed
18	637.60	8.15	5	Stressed
12	637.98	8.09	3	Stressed
14	638.10	8.48	4	Stressed

Table 4.7: Determination of best stress conditions to get accelerated failures during the fourth experiment.

Device ID	V_{DS} Stress [V]	% of BV_{DSS}	T_{DUT} Stress [°C]	Time Stress [h]	Failure
09	687.5	125	175	0.15	Yes
19	660.0	120	175	0.5	No
19	671.0	122	175	3	No
19	687.5	125	175	30	No

Table 4.8: Stress parameters and failure criteria for HTRB test in the fourth experiment.

Parameter	Value	Observation
Stress duration time	500 h	Time divided in 42 stress cycles.
Stress Voltage V_{DS}	671 V	122% of nominal BV_{DSS} (105% of practical BV_{DSS} at 25°C).
Stress Temperature	175 °C	T_{jmax} of DUTs is 150 °C.
ECTs Temperature	30 °C	ECTs performed at t=0h and t=500h.
VECTs Temperature	125 °C	EVTs performed at the end of every stress cycle.
Min. P_H	1.5 W	Minimum Heater Power: failure criterion during stress. to detect thermal runaway.
Max I_{DSS} @$V_{DS} = 550V$;T=125°C	100uA	I_{DSS} failure criterion during EVT.
Min Vth @$V_{DS} = V_{GS}$; $I_D = 250uA; T_{DUT} = 125řC$	1 V	V_{th} failure criterion during EVT.

4.7).

In this ambit, results of Table 4.7 demonstrated that an electrical stress of 125% of

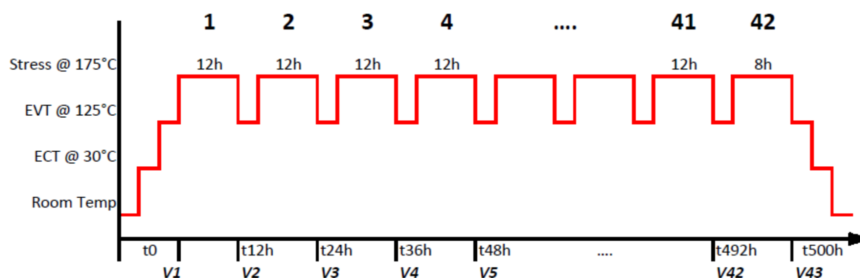


Figure 4.17: Proposed time scheduling for a 500 hours long HTRB test.

the nominal BV_{DSS} could induce at least one failure in minutes. This electric condition, which is managed by the automated instrumentation proposed, over-stresses the devices. However, a more conservative voltage of 671V was used, which represents the 122% of the nominal BV_{DSS}. It is noteworthy that data in Table 4.6 demonstrates that practical BV_{DSS} of DUTs is much higher than nominal one at room temperature. In fact, a mean value of BV_{DSS}=637 V was measured. Because of this, the applied over-stress voltage, at room temperature, is only 105% rather than 122%.

The test lasted 500 hours, divided into 41 stress cycles of 12 hours and one stress cycle of 8 hours (see Figure 4.17). At the end of each stress cycle, EVTs at 125°C was performed. Additionally, ECT at the 30°C was performed both before and after the complex test. Stress parameters and failure criteria set for the experiment are summarized in Table 4.8. The total I_{DSS} degradation trend, presented during the stress, is shown in Figure 4.18. Two failures were observed during the test. In particular, both DUT2 and DUT6 failed in agreement with the V_{th} failure criterion, as in [103]. Regardless, the equipment prevented the DUTs over-damaging, shutting down both the electrical and the thermal stress.

As demonstrated before, the proposed methodology allowed to trace the whole temporal evolution of the electrical parameters of interest, such as I_{DSS}, BV_{DSS} and V_{th} (see Figures 4.19-4.21). In particular, the failed DUTs had a quite different degradation trend, which were caught by the proposed instrumentation. During the first 12 hours, DUT6 leakage current rose suddenly from 1.72 mA until 2.8 mA, but then recovery seemed to start and finally the device failed. On the other hand, DUT2 degradation began to rise slowly until 2.6 mA and, after that, failure also occurred. Furthermore, it is worth noting how the recurrent EVTs cycles, preceded by a partial cooling of the DUTs, did not affect neither the degradation trend nor the electrical properties of devices. This aspect can be appreciated, observing the total I_{DSS} trend in the linear plot displayed in Figure 4.18, where the effects of the DUTs cooling down for each EVT is clearly visible as several and limited I_{DSS} drops as well as the general trend.

Finally, two thermal processes were performed on the failed DUTs to verify whether their degradations were irreversible or not. Also a not failed device (DUT3), during the HTRB test, was included as a reference. In the first process, the mentioned DUTs

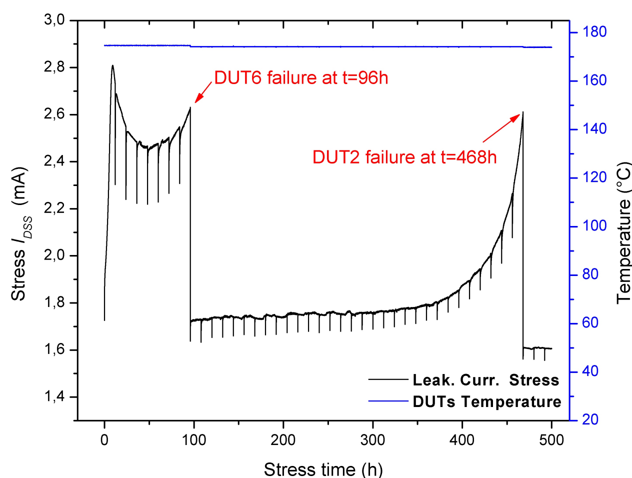


Figure 4.18: Total I_{DSS} degradation during 500h stress over 6 power n-MOSFETs at 175°C and 122% of nominal BV_{DSS}

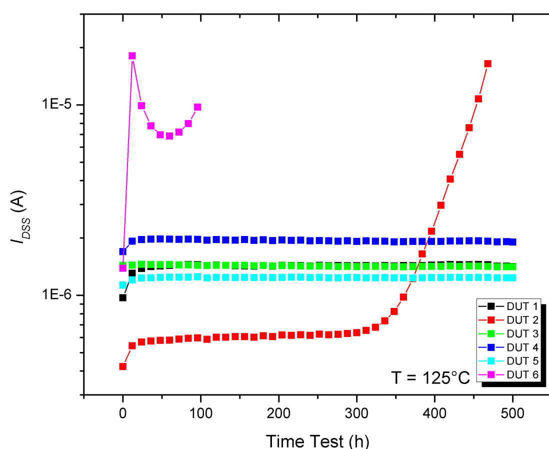


Figure 4.19: Drain-source leakage currents at $V_{DS} = 550V$, during EVTs (T=125°C).

were maintained at the room temperature for 100 hours, without bias. No changes in the degraded electrical parameters were observed. Subsequently, the devices were short-circuited to the ground and heated at 175 °C for 24 hours. As in the HTRB test, several interim EVTs at 125 °C were performed during the test time. In contrast to the other devices, DUT2 continued its degradation trend, revealing that it was not fully damaged during the HTRB test, and only thermal energy is sufficient to degrade even more it electrical parameters as displayed in Figure 4.22. However, these results demonstrated that instrumentation can wear out electric characteristics of power MOSFETs, which

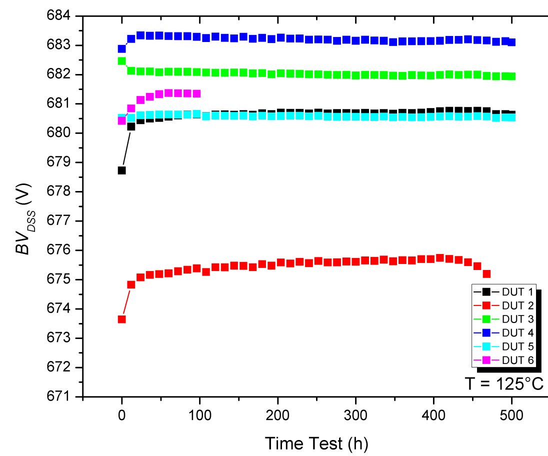


Figure 4.20: Breakdown voltages at $I_{DS} = 1mA$, during EVTs (T=125°C).

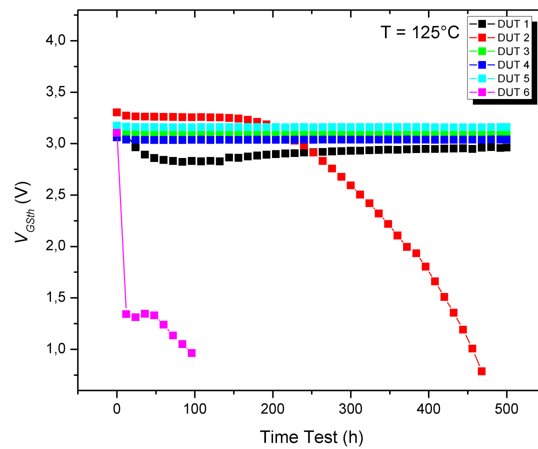


Figure 4.21: Gate-source threshold voltages at $I_{DS} = 250uA$ and $V_{GS} = V_{DS}$, during EVTs (T=125°C).

can be categorized as failures during an HTRB test. Such degradation is also permanent and not recoverable which is favorable for post-failure analysis.

4.7 Experiment 5: HTRB on 1200V Power SiC n-MOSFETs

This section presents the last results from an accelerated HTRB test on power SiC n-MOSFETs in package HIP247. Since these devices are in the R&D phase in STMi-

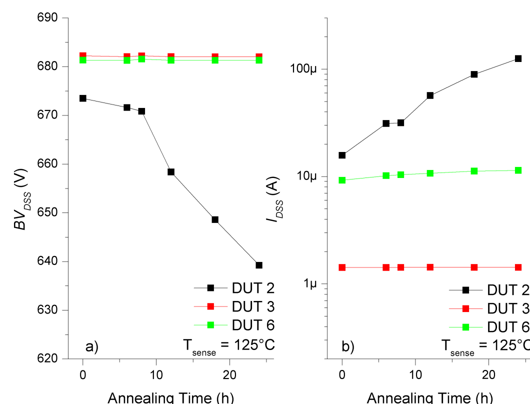


Figure 4.22: Electrical characterization performed at 125°C during the annealing phase (T=175°C). a) Breakdown voltages at $I_{DS} = 1mA$. b) Drain-source leakage currents at $V_{DS} = 550V$.

croelectronics, specific details about the MOSFETs will be avoided. However, the raw data of the electrical characterization and HTRB test during 180 hours are presented. Following the advanced HTRB methodology here proposed, the DUTs were electrically characterized at 30 °C, before and after the advanced HTRB test; while the interim characterization during the advanced HTRB were performed at 125 °C. The maximum or minimum allowed values (failure criteria) for the characterized electrical parameters are presented in Table 4.9. The set plan test for the advanced HTRB is presented in Table 4.10.

It is worth mentioning that the output voltage capability of the SMU is limited to 1100 V at 20 mA. Because of this, a conservative voltage of 1080V was used for the drain leakage current (I_{DSS}) characterization (see Table 4.9). In this way, the reverse breakdown voltage (BV_{DSS}) was not characterized because of such a voltage output limitation in the SMU. Nevertheless, as shown in Table 4.9, three different values of I_{DSS} were characterized to detect the channel formation defects.

The trend of the accumulated leakage current I_{DSS} for the stress test on the six power SiC n-MOSFETs is presented in the Figure 4.23. An initial decrement in the accumulated I_{DSS} of all devices is evident during the first 32 hours. Afterward, the trend is settled around 10 μA. It is worth noting that the HTRB stress test was composed of two parts (see Table 4.10). The first part (32h of stress test) was divided into cycles of 2 hours because of the requirement of more informative data about the initial settlement of the leakage current. Then, the stress cycles were extended to 4h during the second part (66h of stress test).

On the other hand, three different characterization with punctual values of the I_{DSS} characterization performed at reverse voltage V_{DS} of 540 V, 864 V and 1080 V (see Table 4.9) are presented in Figures 4.24, 4.25 and 4.26, respectively. The initial decrement in

Table 4.9: Parameters set for the Electrical Characterization of the 1200V power SiC n-MOSFETs in the fifth experiment.

Parameter	Condition	Rated Values			
		T = 30 °C		T=125 °C	
		Min.	Max.	Min.	Max.
I_{DSS_L}	V_{DS}=640 V; V_{GS}=0 V	—	50 nA	—	500 nA
I_{DSS_M}	V_{DS}=864 V; V_{GS}=0 V	—	100 nA	—	1 μA
I_{DSS_H}	V_{DS}=1080 V; V_{GS}=0 V	—	200 nA	—	2 μA
$+I_{GSS}$	V_{GS}=+21 V; V_{DS}=0 V	—	1 nA	—	10 nA
$-I_{GSS}$	V_{GS}=-10 V; V_{DS}=0 V	—	-1 nA	—	-10 nA
V_{th}	$V_{GS} = V_{DS}$; I_D=1 mA	2.5 V	—	2 V	—

Table 4.10: Plan of the stress test parameters configured during the fifth experiment.

Parameter	Value	Observation
Stress duration time	98 hours	Stress time divided in cycles of 2h (part I) and 4h (part II).
Stress Voltage V_{DS}	960 V	80% of the rated BV_{DSS}.
Stress Temperature	200 °C	Max. rated T_j of devices.
ECTs Temperature	30 °C	Initial and final ECTs.
EVTs Temperature	125 °C	Interim ECTs for verification.

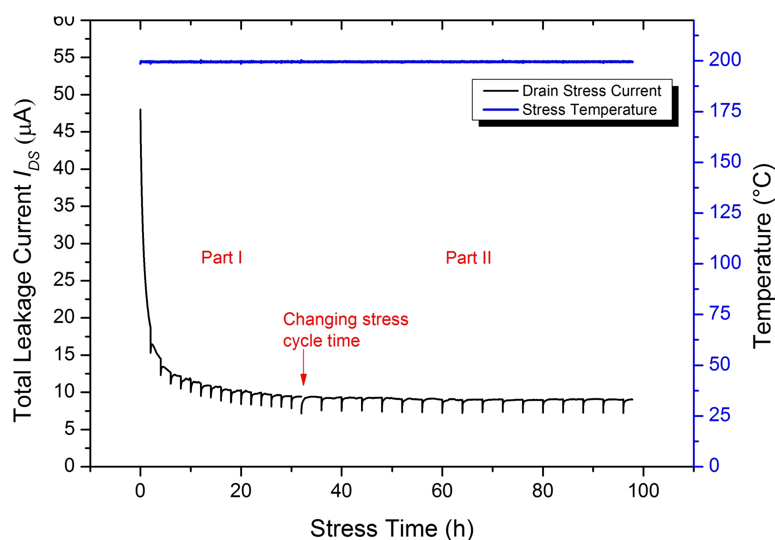


Figure 4.23: Total I_{DSS} degradation during 98h stress over 6 power SiC n-MOSFETs at 200 °C and 80% of the rated BV_{DSS}. First part was with stress cycles of 2h and second one was with 4h for stress cycles.

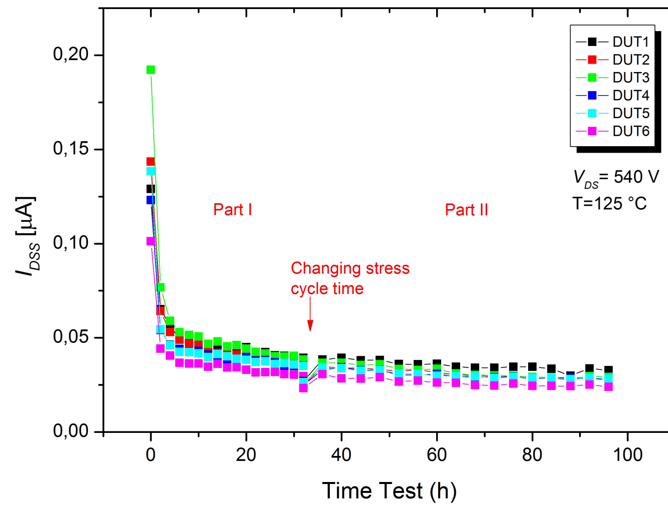


Figure 4.24: Interim measurements of the I_{DSS} (at V_{DS}=540 V and T=125 °C) performed at the end of every stress cycle during the advanced HTRB on power SiC n-MOSFETs.

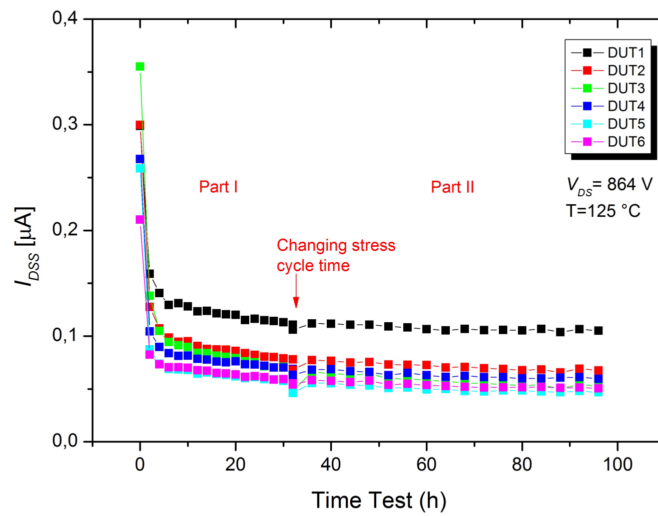


Figure 4.25: Interim measurements of the I_{DSS} (at V_{DS}=864 V and T=125 °C) performed at the end of every stress cycle during the advanced HTRB on power SiC n-MOSFETs.

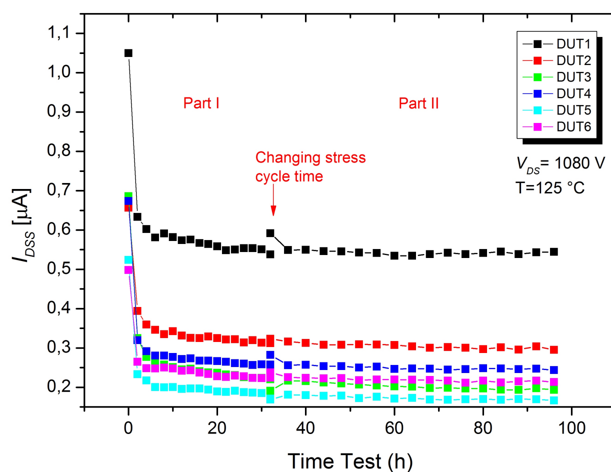


Figure 4.26: Interim measurements of the I_{DSS} (at V_{DS}=1080 V and T=125 °C) performed at the end of every stress cycle during the advanced HTRB on power SiC n-MOSFETs.

the I_{DSS} is again clear for all the DUTs in the three different measurements. At the first glance, the DUT1 presents a higher leakage current at 864 and 1080 V than the other DUTs. While that for 560 V, the I_{DSS} of the DUT1 is similar to the other sample devices.

In fact, the Figure 4.27 shows a comparison between the I-V curves of the I_{DSS} measurement for all DUTs at 125 °C, which definitively demonstrates that DUT1 exhibits the highest leakage for high voltage regime than that of the other samples. Also, DUT3 slightly presents the highest leakage current but at low voltage regime. It is worth noting that this last observation is not reflected in the I_{DSS} periodical measurements presented in Figure 4.24 . Furthermore, Figure 4.28 shows also a comparison between the I-V curves measurements performed during the interim threshold voltage V_{th} characterization at 125 °C. At the first glance, for whichever threshold voltage extraction, the DUT1 will present the lowest V_{th}. This affirmation is supported by Figure 4.29, which shows the historical of punctual values of V_{th} extracted from the EVTs performed at 125 °C, with electrical conditions given by $V_{GS} = V_{DS}$ and I_D=1 mA (see Table 4.9).

Moreover, Figure 4.30 shows the temporal series of punctual values of $\pm I_{GSS}$ extracted from the EVTs performed at 125 °C, with electrical conditions given by V_{GS} = +21 V and -10V and V_{DS} = 0 V (see Table 4.9). There were not notable changes in the gate leakage currents except for the modest recoveries that born from the short interruption in the stress test to change the test conditions. In fact, this behavior was also present for the other electrical parameters before reported.

It is worth highlighting that I_{DSS} and $\pm I_{GSS}$ parameters, measured in the power SiC n-MOSFETs characterization, notably decreased during the first part of the advanced HTRB, and then these electrical parameters stayed stable. This behavior is not related

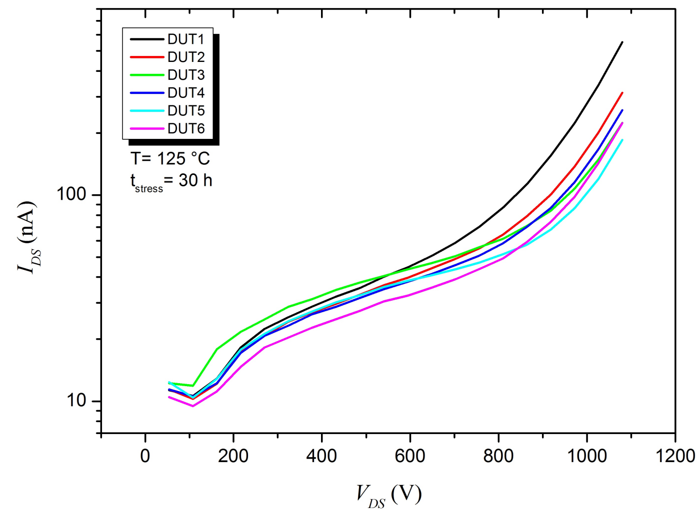


Figure 4.27: Comparison of I-V curves measured for the I_{DSS} characterization on all DUTs at T=125 °C. Such characterization was interim performed at the 30h of the advanced HTRB test on power SiC n-MOSFETs.

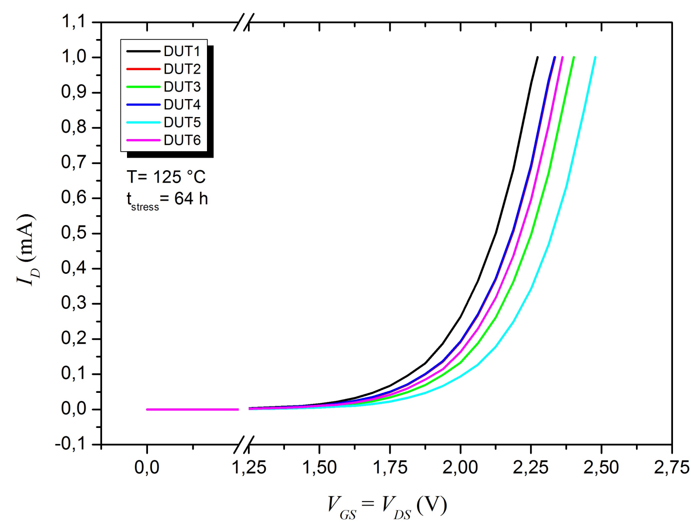


Figure 4.28: Comparison of I-V curves measured for the V_{th} characterization on all DUTs at T=125 °C. Such characterization was interim performed at the 64h of the advanced HTRB test on power SiC n-MOSFETs.

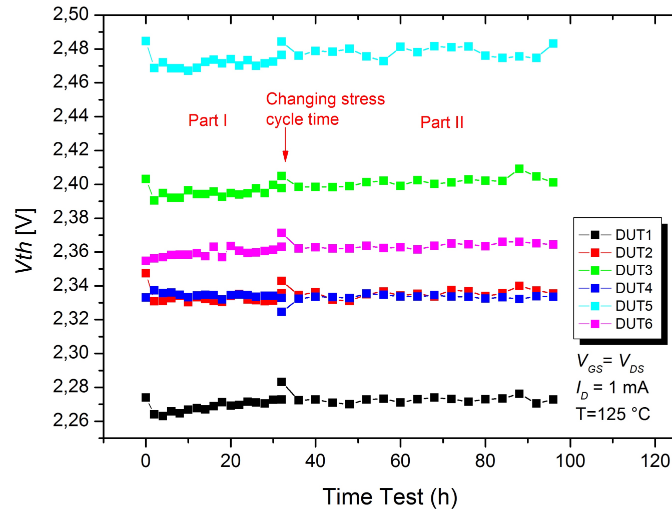


Figure 4.29: Interim measurements of the V_{th} (at $V_{GS} = V_{DS}$, I_D=1 mA and T=125 °C) performed at the end of every stress cycle during the advanced HTRB on power SiC n-MOSFETs.

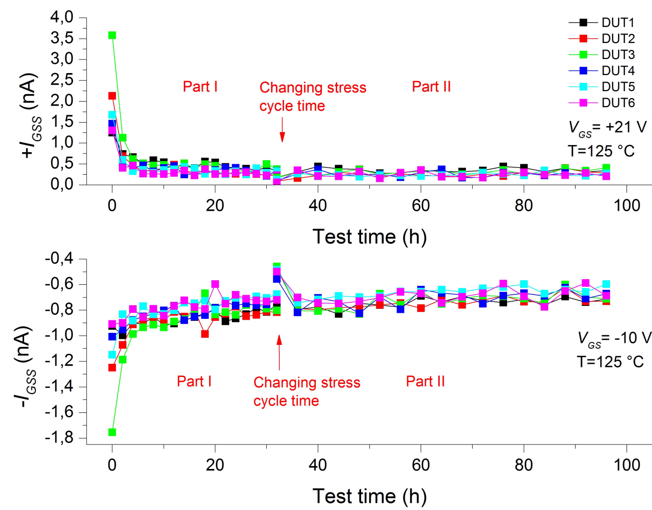


Figure 4.30: Interim measurements of the $\pm I_{GSS}$ at V_{GS} = +21 and -10 V, respectively, performed at T=125 °C at the end of every stress cycle during the advanced HTRB on power SiC n-MOSFETs.

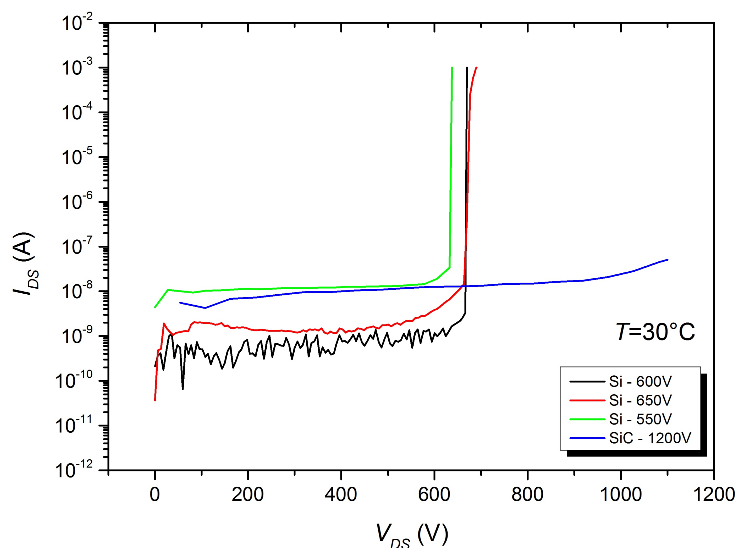


Figure 4.31: I-V curves of the I_{DSS} characterization at T=30 °C on Si and SiC power n-MOSFETs.

to degradation effects, but to some enhancement of the electrical parameters due to the stress temperature. However, the V_{th} parameter stayed almost stable during the whole test. Further work will be performed on this fields.

4.8 Experiment 6: Si and SiC Drain Leakage Current Comparison

A comparison based on the I_{DSS} characterization of three different power Si n-MOSFETs and a power SiC n-MOSFET is performed. The results of such sample devices were presented in the last sections, but here, their measured I-V curves at 30 and 125 °C are compared and commented.

The Figure 4.31 shows the I-V curves at 30°C of 550 V, 600 V, and 650 V Si power n-MOSFETs, together with that of a 1200 V SiC power n-MOSFET. It is evident that the leakage current of the SiC device is comparable to that of Si ones, and even one decade higher than that of 600 V and 650 V best Si devices. However, the leakage current of the Si devices rapidly rises at their respective rated breakdown voltages, while the SiC device continues working till the maximum allowed voltage output of the SMU (1100 V) without notable changes. At the first glance, regardless the higher breakdown voltage, the SiC device does not show greater performance than that of its counterparts at the low-temperature regime.

However, general power applications force devices to reach high junction temperatures increasing the leakage current of the power semiconductor devices. Because of this, the power losses increases and the use of bulky cooling systems are imperative.

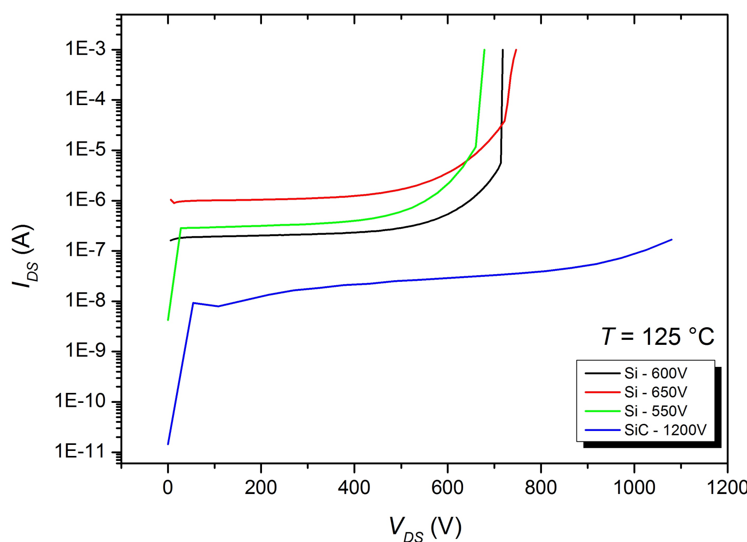


Figure 4.32: I-V curves of the I_{DSS} characterization at T=30 °C on Si and SiC power n-MOSFETs.

In fact, the incremented I-V curves of the Si and SiC devices at 125 °C are presented in Figure 4.32. At the first glance, the leakage currents of the Si devices rises two and three decades at this high temperature, but the curve of the SiC transistor was increased slightly at the high voltage regime.

Finally, it is possible to conclude that SiC power MOSFET demonstrates to be advantageous when it is carried to work in the high-temperature regime if compared with its Si counterparts. Otherwise, the power loss of the SiC device is comparable to that of its Si counterparts at room temperatures.

Chapter Conclusions

The work presented in the last chapter refers to several experiments performed on power n-MOSFETs, which were conducted to verify the effectiveness of the automated instrument developed for applying the proposed advanced High Temperature Reverse Bias (HTRB) methodology. Firstly, a brief description of temperature calibration and extrapolation processes in the Thermal Control Modules (TCMs) is presented (see Figure 4.5). These tasks were automatized through the PC user application. Also, a demonstrative case of the Thermal Runaway control and detection was also reported in the experiment 1 section (see Figure 4.8).

Moreover, several advanced HTRB tests were performed on Commercial On The Shelf (COTS) power Si n-MOSFETs from STMicroelectronics rated for breakdown voltages of 550 - 650 V, and the related results have been recalled in this chapter. In particular, the experimentation 2 reports the results obtained from continuous stress test and stress

cycles of HTRB (see Figure 4.11). Such an experimentation was performed on 650V power $MDmesh^{TM}$ n-MOSFETs.

The experiment 3 uses again 650 V power MOSFETs denominated "super junction". Two different approaches of stress cycles were applied (see Figures 4.12 and 4.14), obtaining two failures in total and testing a particular feature of the instrumentation to isolate the failed devices automatically (see Figure 4.13).

Finally, experiment 4 is one of the several long test time on Si devices performed with the developed instrumentation. It involved 6 COTS power MOSFETs rated for 550V breakdown voltage, which were stressed by the advanced HTRB during 500h (see Figure 4.18). In particular, two failures were observed with different trends: the first one had a monotonic degradation, whereas the second one failed after a partial recovery. In this occasion, a subsequent thermal annealing process (100 hours at room temperature and then 24 hours at 175 °C) revealed a permanent damage in the first case and a further degradation trend for the second failed device (see Figure 4.22). These different behaviors could represent two different signatures of failure that could be analyzed with a post-failure analysis. Consequently, the proposed equipment could be used not only for reliability testing but also for diagnostic and investigation purposes.

It is worth mentioning that all the advanced HTRB tests over Si devices were performed using the first prototype of the developed instrumentation with the SAFeFET as heater element in the TCMs.

Moreover, the preliminary results, from a conservative advanced HTRB stress test on power SiC n-MOSFETs rated for 1200 V of breakdown voltage, are also presented. This test demanded the second prototype of the developed instrumentation, which uses SiC power MOSFETs as heater elements and PT1000 for temperature sensing. The second prototype allows for stress temperatures around 200 °C. In experiment 5, the total stress time of 98h was divided into two parts (see Figure 4.23). The first one was formed by stress cycles of 2h, while the second part consists of stress cycles of 4h. A decreasing trend of the accumulated leakage current of the 6 SiC devices characterized the first part. Historical punctual values for the I_{DSS}, $\pm I_{GSS}$ and V_{th} were presented in Figures 4.26, 4.30 and 4.29, respectively. It is worth highlighting that I_{DSS} and $\pm I_{GSS}$ parameters notably decreased during the first part of the advanced HTRB, and then these electrical parameters are settled. This behavior is not related to degradation effects, but to some enhancement of the electrical parameters due to the stress temperature. However, the V_{th} parameter stayed almost stable during the whole test.

At the end, a collection of measured I-V curves data at 30 and 125 °C, during the I_{DSS} parameter characterization of different Si and SiC devices, were displayed for comparison purposes in the Figures 4.31 and 4.32, respectively. It was demonstrated that SiC power MOSFET presents advantageous electrical characteristics at high temperature regime when compared with its Si counterparts. Otherwise, the power loss of the SiC device is comparable to that of the Si power MOSFETs at room temperatures.

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Chapter 5

Low-Frequency Noise Characterization

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As mentioned in the first chapter, Low-Frequency Noise (LFN) is not a serious problem in power MOSFET devices because of the high densities power that these handle. However, it has been stated also that measurement and characterization of low-frequency noise can be used as a diagnosis tool in semiconductor devices [9], [10]. Therefore, defectiveness formation during device production (oxide interfaces growth, doping processes, packing among other similar) or the that formed during accelerated life testing can be evaluated to be correlated to specific degradation mechanisms like traps formation and impurities diffusion. Moreover, noise measurements can also a diagnostic tool to determine crystal and structure defects as well as charge transport mechanisms in new 2D materials as Graphene [56], [119]–[121].

In this way, methodology followed and instrumentation used for the prosecution of LFN Measurements (LFNM) on power MOSFETs are presented in this chapter. Moreover, the chapter is completed with the report of a specific experimentation results of LFNM in: COTS SMD resistor (R=1 KΩ), COTS high voltage power MOSFET devices (STP18N55M5) and experimental Liquid-Phase Exfoliated Graphene (LPEG) films. It is worth mentioning that the latter were part of a collaboration work with doctoral students from the Department of Physics (UNICAL) and details about production, Raman and SEM spectrum characterization among others, are reported in [122]. Important considerations and discussion on the LFNM results obtained are included below.

5.1 Methodology

General methodology for the LFN measurements consisted in:

- I-V characterization of the DUT to determine better static operation condition for the LFNM.
- Voltage/Current biasing of the DUT to force a point operation.
- Sampling acquisition of the noise signal.
- Calculation of the PSD using Discrete Fourier Transform (DFT) in LabWindows-CVI.
- Visualization and storage of the data results.

Due to not all DUTs were packaged or power devices, specific considerations were taken based on the characteristics and physical disposal of the samples. Thus, for power packaged MOSFETs, devices were directly connected to the measurement instrumentation. Instead, in the case of the COTS SMD resistor and experimental LPEG films, the samples were connected to the instrumentation through a Micro-Probe Station similar reported in [123].

In a first stage, single channel measurements of LFN were used to characterize the background current noise instrumentation in open circuit input condition. Afterwards, measurements were concentrated on SMD resistors. There are several techniques adopted for LFN measurement. More details about these techniques and instrumentation required can be found in [10], [124], [125]. In most of the LFN measurements reported in this section, single channel characterization have been performed.

Moreover, single channel characterization technique was also used to measure LFN in power n-MOSFET devices, which were stressed through HTRB tests using the methodology and instrumentation described in chapter 3. In particular, main parameters of the stress test are summarized in Table 5.1. It is worth noting that the DUTs were over-stressed with 100 % of the BV_{DSS} and stress temperature set to 200 °C, duration 8 hours. LFN was characterized in the DUTs, before and after the stress test. During the stress, one of the devices was heavy degraded and important changes in the noise spectrum were revealed.

Furthermore, the same last technique for LFN measurement was used in LPEG films. Again, the Micro-Probe Station similar reported in [123] was used for the interconnection between the Inter-Digitated Electrodes (IDEs) sample holder pads and the instrumentation. A first stage of I-V measurements permitted to determine important electrical characteristics of the samples that are deeply reported in [122]. Then, LFN measurements at several current biasing on different LPEG films were performed. Important results and discussions related to the noise spectrum and electrical characteristics are presented below.

Table 5.1: Stress test parameters of the HTRB test performed on the COTS power n-MOSFETs (STP18N55M5).

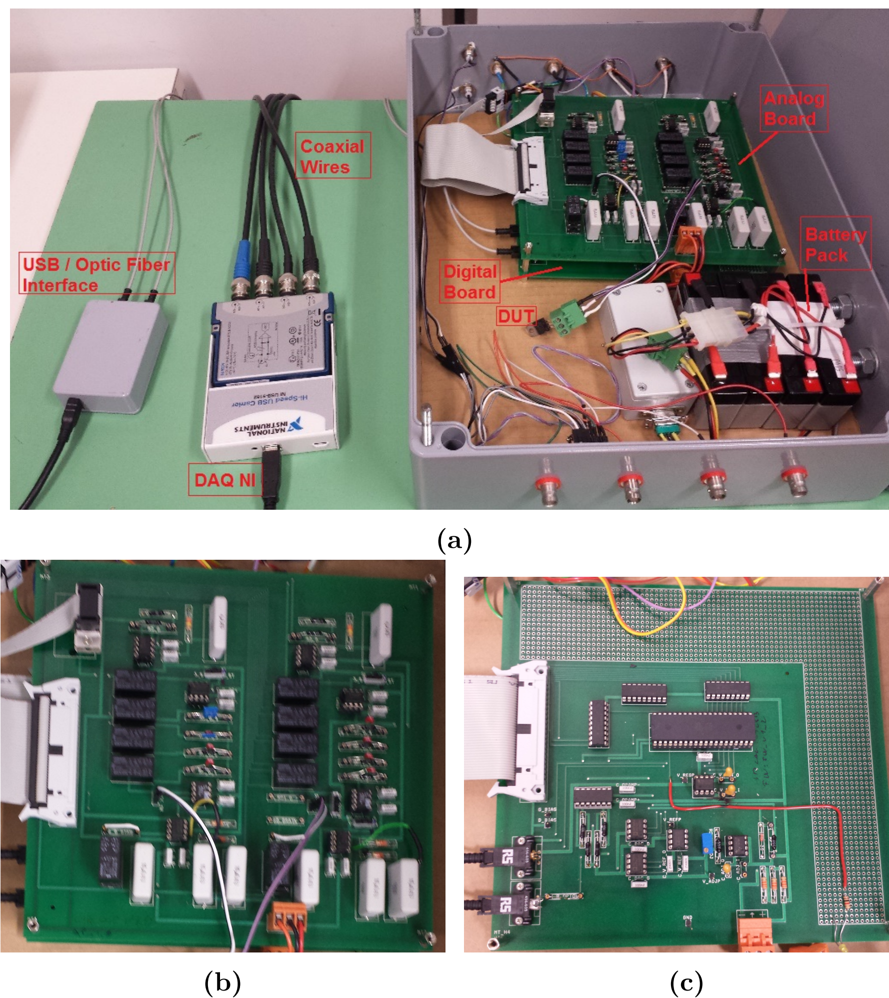
Parameter	Value	Observation
Time Duration Stress	8 h	Time divided in 4 cycles of 2 h.
Stress Voltage V_{DS}	600 V	100% of BV_{DSS} (Datasheet).
Stress Temperature	200 °C	Max. T_j of DUTs: 150 °C.
ECTs Temperature	30 °C	ECT performed before and after stress.
VECTs Temperature	125 °C	ECT performed every stress cycle.

5.2 Instrumentation

Generally, the measurement of LFN is a long time task because of a better accuracy of the spectrum measured in the low-frequency range is reached when the sampling of the signal is performed during long time. Furthermore, low-noise amplifier electronic systems are required to amplify the noise signal [126]. Once, the noise signal has been amplified, its PSD can be analysed through a spectrum analyser instrument. The latter can an apposite expensive commercial instrument or can be implemented thought a DAQ for signal acquisition and discrete treatment in computer applications. In particular, the hardware instrumentation for the noise amplifying and signal acquisition reported in [127] were used. This instrumentation allows for implementation of various amplification gain and configuration channels, which can be configured through a set of SCPI commands sent from a PC application. It is worth mentioning that enhancements to the set of commands (firmware) and particular hardware details were added as a personal contribution for the instrument performance. A whole implementation of the hardware mentioned before is presented in the Figure 5.1a.

Main characteristics and advantages of the hardware instrumentation used for the amplification of noise during the LFNM are:

- Two low noise amplification channels with configurable gain each one.
- DC and AC output noise signal for each channel.
- Low noise bias sourcing to the DUT through battery pack and filtering (see Figure 5.1a).
- Excellent external noise isolation through a shielded box (see Figure 5.1a).
- USB (serial) to Fiber Optic interface communication to avoid injection of any external noise disturbance inside the shielded box (see Figure 5.1a).
- Fully configurable gain remotely through serial terminal using SCPI commands, which avoids to interrupt the electromagnetic isolation or change the environment parameters for the stability of the instrumentation.



(a)

(b) (c)

Figure 5.1: a) Full view of the hardware instrumentation used for the LFNM. b) View of the PCB analog board. c) View of the PCB digital board.

- Programmable voltage/current bias source from serial terminal using SCPI commands for each measurement channel.
- Independent Analog and Digital boards (see Figures 5.1b and 5.1c, respectively).
- Possibility of interfacing with DAQs and Probe Stations using coaxial wires.
- Capability to perform I-V characterization at low voltage/current regime.
- Possibility of turning off the digital board during LFNM.

When LFN measurements were performed in packaged power MOSFETs, the DUTs were placed inside the shielded box together with the noise measurement instrumentation

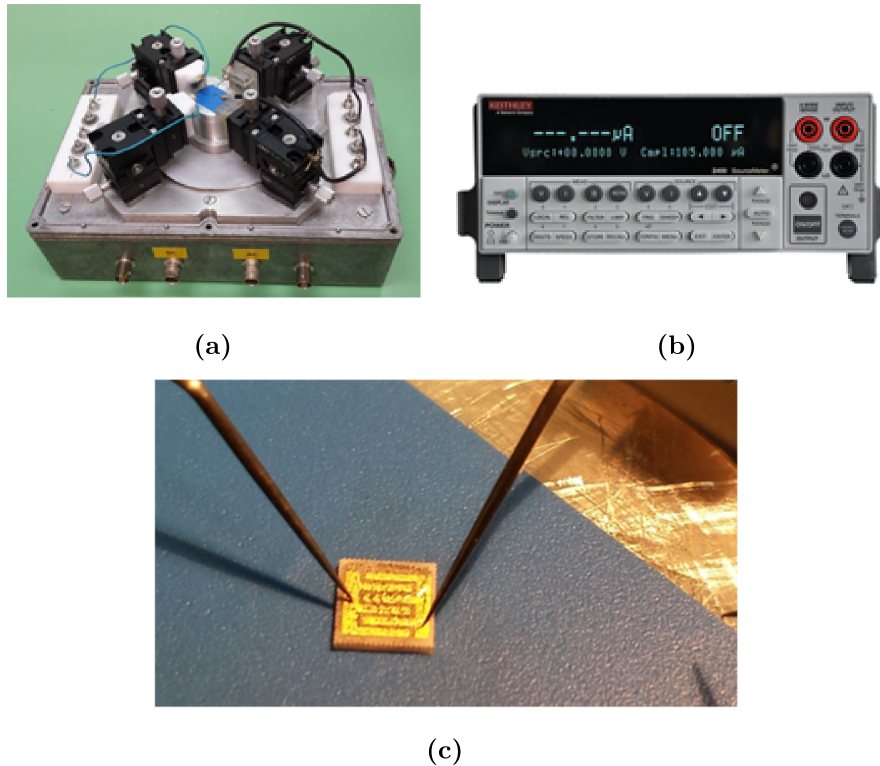


Figure 5.2: a) Mini-Porbe station used for LFNM. b) Frontal view of the SMU Model 2410-C from Keithley Instruments Inc. c) Physical connection of the IDEs sample holder for the LPEG film characterization.

to avoid any electromagnetic or electrostatic disturbances from external noise sources (i. e. power lines distribution, RF Tx/Rx apparatus, bad filtering process in power supply among others) (see Figure 5.1a). External disturbances noise can lead to introduce undesired noise spectrum in the final result.

On the other hand, as shown in the Figure 5.2a, a shielded Mini-Probe station was used complementary to the LFNM instrumentation because of the small contacts terminals of SMD resistor and the micro-pads of the IDEs sample holder for the LPEG films. This Mini-Probe station was aimed to facilitate the interconnection between the samples and the instrumentation and to avoid external electromagnetic disturbances. Physical implementation of Mini-Probe station connecting the sample holder of the LPEG film is displayed in the Figure 5.2c.

Moreover, for certain I-V characterization on the devices (SMD, power MOSFETs, LPEG film) a Source and Measuring Unit (SMU), Model 2410-C from Keithley Instruments Inc., was used as in the last chapter. The front view of the SMU is presented in the Figure 5.2b.

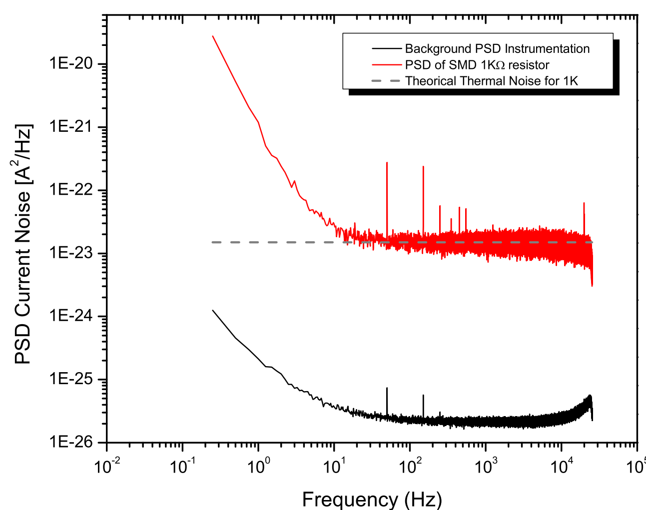


Figure 5.3: PSD measured in a SMD 1 KΩ resistor, which presented thermal noise combined with background noise of the instrumentation amplified by the current bias polarization.

5.3 Experimentation

5.3.1 Thermal Noise Measurement on SMD Resistor

The LFN spectrum of a SMD thick-film chip resistor of 1 KΩ (format 0805) was performed. Current noise PSD of this measurement is presented in Figure 5.3, together with the background current noise of the instrumentation when a open circuit condition is in the input channel. At a first glance, the background noise is well low compared to the noise measured in the resistance. Also, the theoretic value for the thermal noise ($S_I = 4kT/R$) is reported in the Figure 5.3.

It is worth noting that background noise of the instrument is a composite of white noise and 1/f noise sources, and the latter affects also the measurement of the thermal noise in the resistor for the low frequency range. The transition from the 1/f noise to the thermal noise (or white noise) is referred as corner frequency (f_c). When the polarization current I increases, the $1/f$ noise of the instrument also increases scaled by the squared biasing current (I^2) as was defined in the equation 1.50. This first stage was aimed to verify the functionality of the measurement experimental setup to be used in the next stages described below.

5.3.2 1/f Noise Measurement on Power n-MOSFETs

As was mentioned in the last section, LFN was measured on power n-MOSFET devices, before and after that the devices were over-stress with HTRB test using the

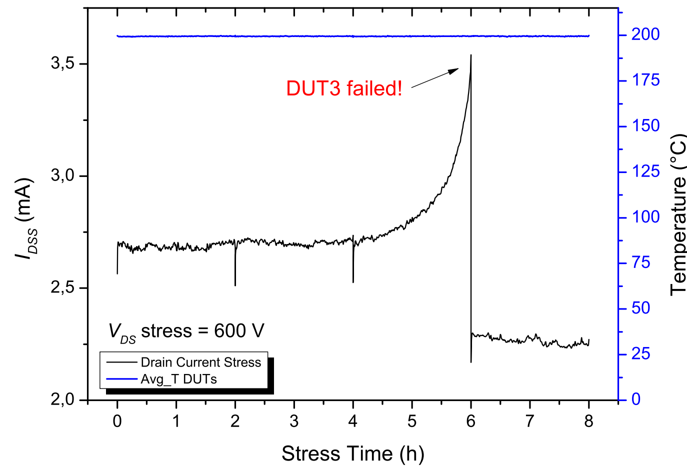


Figure 5.4: Trend degradation of the stress leakage current (I_{DSS}) in six power n-MOSFET devices performed at T=200 °C and V_{DS}=600 V.

conditions test summarized in the Table 5.1. The LFN measurements were performed at room temperature in a laboratory environment. The main aim to combine LFNM with HTRB tests is to seek for early and significant noise spectrum changes, referred to the noise spectrum measured at the t=0h, that can give a significance information about degradation mechanisms acting during the accelerated tests. First, the total stress leakage current of the devices is presented in Figure 5.4, as an antecedent for the description of the LFN measurements. As noted, DUT3 degraded strongly in its stress current contribution until it was separated from the test automatically by the HTRB system explained in the last chapters.

To carry out the measurement of the LFN, first a I-V characterization at low voltage rating was performed using the same instrumentation presented in the last section. An example of the results of these measurements are presented in Figure 5.5. The last measurement is important to determine the better possible operation point of the DUT during the noise measurement. Using the results of the I-V characterization, a set of bias conditions for V_{GS} and V_{DS} was configured for each LFN measurement per every DUT to assure a bias current condition of I_{DS}=250 μA.

In the Figure 5.6, a comparison between the PSD of the noise current measurements in power n-MOSFET devices, performed before the stress test, is presented. It is worth noting that the PSDs have been normalized for the squared bias current (with I_{DS} ~250 μA) to allow direct comparison of the $1/f$ noise between devices. At a first glance, the noise PSD measured in the DUT6 shows a bulge in the range frequency $\sim 10^1$ to $\sim 10^3$ Hz. Also, a particular bulge was evident for the DUT3 starting from 10^0 Hz (see Figure 5.7). These bulges is a typical presences of Lorentzian PSD that reflects the existence of some specific RTS noise mechanism as explained in the first chapter. Such

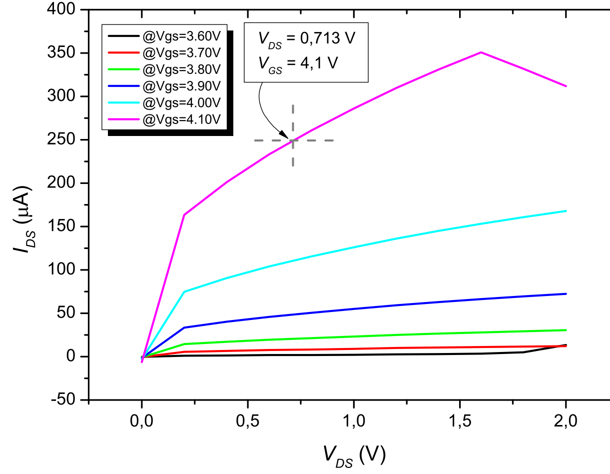


Figure 5.5: I-V characterization of a power n-MOSFET for low voltage/current regime looking for the better operation point for the LFN measurements.

noise mechanism is related with traps generated from impurities or defects in the oxide interfaces of the conductive channels [9], [52]. Moreover, all the DUTs presented the same level of $1/f$ noise, and this is consistent with a power fitting:

$$\frac{S_I}{I^2} = K\frac{1}{f^\gamma} \tag{5.1}$$

with, $K \sim 5.2 - 6.2 \times 10^{-13}$ and $\gamma \sim 1.1$ for all the DUTs.

Once the HTRB stress test was finished, the DUTs were relaxed by 1 hour, and the noise characterization was performed again on the devices. Except for the DUT3 and DUT6, any significant change in the PSD noise spectrum was detected. It is worth mentioning again that the DUT3 was strongly degraded of its V_{th} (>40% @125°C) and I_{DSS} (>100% @125°C) parameters, while that DUT6 only describes an imperceptible variation of its electrical parameters <0.1%. On the other hand, those electrical parameters of all the other DUTs remain constant. Directly comparison between the PSD noise spectrum before and after stress test for DUT3 is presented in the Figure 5.7, while that for DUT6 is presented in the Figure 5.8.

At a first glance to the Figure 5.7, the shape of the noise spectrum of the DUT3 has drastically changed, which is a cause of the strong degradation suffered. In fact, the fitting parameter γ is more than 1.0 (b=-1.57 in the inset of Figure 5.7) which is a clear evidence that $1/f$ was worsened toward a RTS noise mechanism characterized by $1/f^2$ form, which is evidence of a clear proliferation of traps density in the channel interfaces.

Finally, through observations at the Figure 5.8, the original bulges, presented in the PSD noise spectrum measured before the stress test, disappeared as evidenced the noise spectrum measured after the HTRB stress test. In fact, the fitting parameter γ is closer

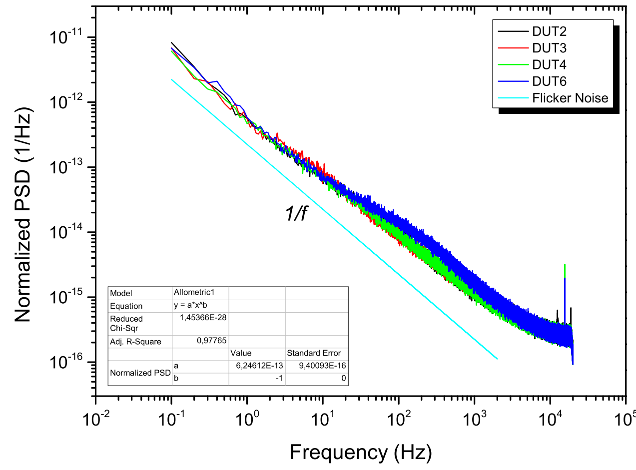


Figure 5.6: Normalized $1/f$ noise measured on the power n-MOSFET devices before HTRB stress.

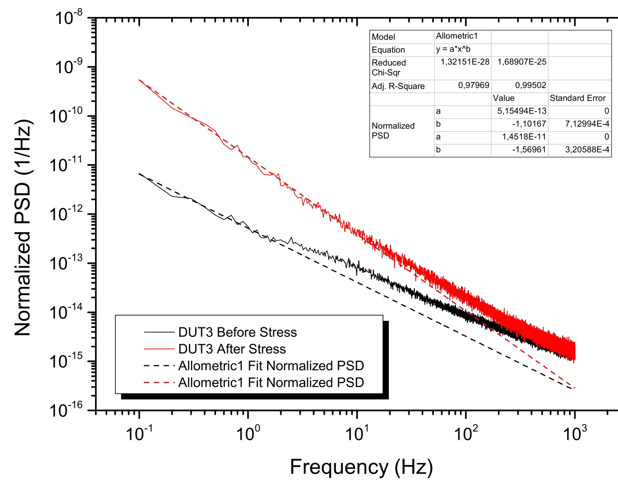


Figure 5.7: Normalized $1/f$ noise measured on the power n-MOSFET DUT3, before and after HTRB stress.

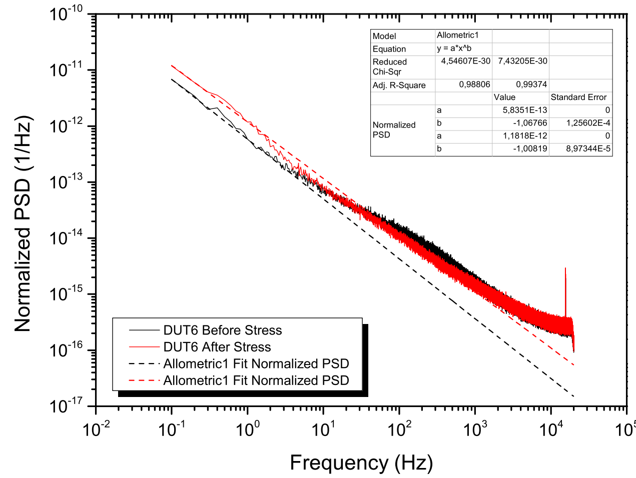
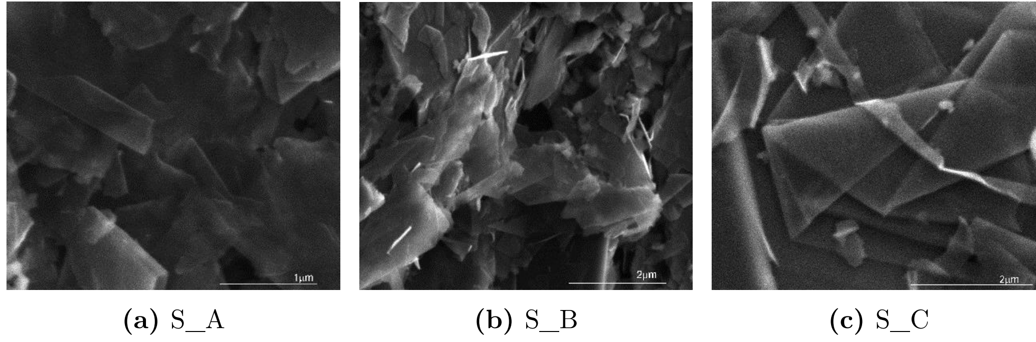


Figure 5.8: Normalized $1/f$ noise measured on the power n-MOSFET DUT6, before and after HTRB stress.

to 1.0 (b=-1.009 in the inset of Figure 5.8) which is a clear evidence that $1/f$ noise was enhanced. The cause of this improvement was a consequence of the bulge cancellation, which demonstrates that specific interface traps (probably caused by impurities) were diffused or cancelled due to the thermal energy (or even electric field) action during the HTRB test.

5.3.3 1/f Noise Measurement on LPEG Films

In this section, the results of a collaborative study with the Department of Physics (UNICAL) are presented. In this collaboration, a comparative study, from the electrical point of view, over three Liquid Phase Exfoliation Graphene (LPEG) in the form of inks was required. Micro films were obtained through the deposition of LPEG material obtained on Al_2O_3 substrates with Au Interdigitated Electrodes (IDE), which thickness is $\sim$1.3 μm. The shape of the sample holders and the pad connection to the instrumentation was commented in the last section (see Figure 5.2c). The sample holder describes a channel relatively larger ($\sim$150μm) compared to the mean length of single flakes graphene obtained (3μm). Total channel area was computed in $\sim$1.39mm^2. Greater details about the procedure to obtain the three LPEG inks, Raman spectrum, Scanning Electron Microscopy (SEM) characterization and films production can be found in [122]. However, singular results of the SEM characterization are presented in Figure 5.9. For practical purposes, and to avoid go out of the topics of this thesis work, the three samples analysed will be nominated S_A, S_B and S_C. For comparison, S_A sample was obtained following state-of-the-art production process for LPGE, but S_B and S_C samples were obtained with alternative procedure also detailed in [122]. In all the cases, graphite was



(a) S_A **(b)** S_B **(c)** S_C

Figure 5.9: Scanning Electron Microscopy (SEM) of the LPEG flakes, that formed the films electrical characterized in this section. Author's courtesy of [122]

used as precursor material and mechanical exfoliation was carried out in liquid phase using solvents.

Using the instrumentation detailed in the last section, the thermal-electrical properties of interconnected graphene films were characterized together to Low-Frequency Noise Measurements (LFNM). Main results of such characterization are presented below.

I-V Characterization at Room Temperature

For this characterization procedure, voltage exploration, in the range V=[-1,1] was applied to sample holder terminals. The measurement results were computed in order to obtain the 2D-resistivity film for each LPEG sample using the conventional expression for 3D-resistivity but neglecting the material thickness t because of its few atomic layers number, as in the case of graphene:

$$\rho_F = \frac{\rho_{3D}}{t} = \frac{\Delta V}{\Delta I} \cdot \frac{W}{L} \quad [\Omega] \tag{5.2}$$

where ΔV is the single delta of voltage applied, ΔI is the delta of current measured, while that W and L are the width and length of channel formed from the IDEs sample holder above mentioned. For comparative purpose, results obtained for all the three films were normalized to their maximum film resistivity ρ_{CNPn} with n as the sample number) and presented in Figure 5.10.

At a first glance to the Figure 5.10, the presence of a so-called Charge Neutrality Point (CNP) around zero Volts bias condition is evident. CNP occurs when the surface charge enters in an equilibrium state for positive and negative charges [128], [129]. At the light of information presented in this section, it can hypothesize that the samples analyzed are composed of several interconnected (micro) nanoscopic LPEG flakes. The interconnection of such flakes, probably attracted each other by Van der Waals forces, forms non-linear Ohmic contacts [130], resulting in the non-linear I-V characteristic displayed in the Figure 5.10. On the other hand, it can also hypothesize that such Ohmic contacts, resulted from the interconnection of LPEG flakes, able the distribution

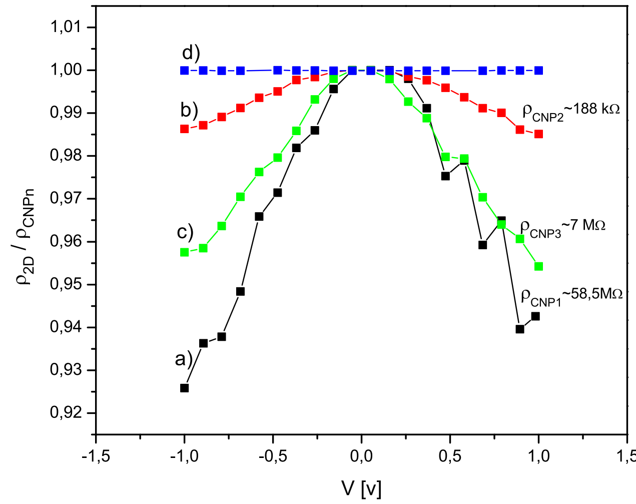


Figure 5.10: Film 2D-resistivity ρ_F normalized for the 2D-resistivity on Charge Neutrality Point (ρ_{CNPn}) for: a) S_A b) S_B and c) S_D samples. d) Normalized resistivity of a standard known resistor is also reported for comparison purpose.

of some electric field between LPEG flakes that unbalances the intrinsic surface or volume charges favouring the criteria by which CNP is formed. If this hypothesis is true, the electric field fixes the positive and negative charges according to the electric field lines direction, and each time the electric field is higher (higher voltage V applied), lesser the free-charges to conduct electric current are. In fact, the CNP is the point of maximum 2D-resistivity (or minimum 2D-conductivity) in 2D materials. Thus, the decrement of resistivity while the voltage V increases, regardless the sign of polarization, could be related to either of the before mentioned assumptions. For comparison, the same I-V characterization and data treatment over a COTS resistor was performed (see Figure 5.10, the blue-linked dots). Instead, the COTS resistor does not present dependence on the voltage applied.

Furthermore, I-V plots of the Figure 5.10 establishes that S_B samples presented the smallest ρ_{CNP} with $\sim$188 kΩ followed by S_C and S_A samples with $\sim$7 MΩ and $\sim$58.5 MΩ, respectively.

LFN Characterization at Room Temperature

Regarding the LFN measurements, in the Figure 5.11, it is evident the overlaying of the different normalized noise spectra (S_I/I^2) measured on S_B sample for different current bias. It is worth noting that when the current is sufficiently low (e.g. 4.5 μA), thermal noise is dominant (black line) forming the so-called "corner frequency" (f_c $\sim$500 Hz) with the 1/f noise curve. Power fitting results, over the $1/f$ part, were

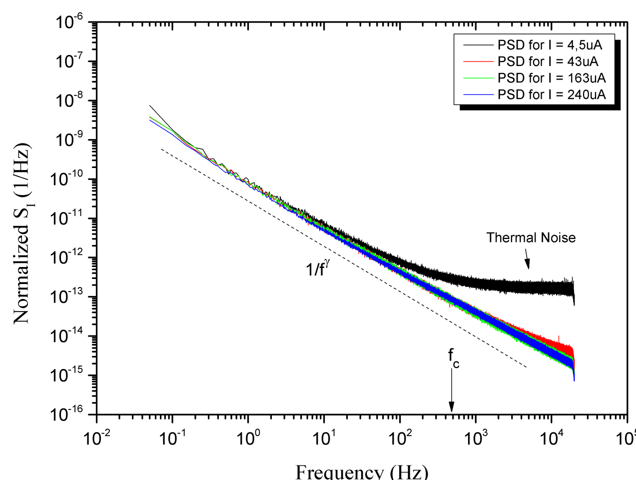


Figure 5.11: Normalized $1/f$ noise measured over the S_B LPEG film sample using different level of current bias. Power fitting results were $K \sim 6.3 \times 10^{-11}$ and γ ~1.08. For sufficiently low current bias (e.g. 4.5uA), thermal noise related to the intrinsic sample resistance is dominant from f_c ~500 Hz with $\sim 3.3 \times 10^{-13}$ [1/Hz].

$K \sim 6.3 \times 10^{-11}$ and γ ~1.08. The last fitting parameters demonstrate that noise spectrum is effectively flicker noise, and that the noise of the S_B sample is higher than that measured for the power n-MOSFET devices reported in the previous section.

To directly compare the noise level between the samples, a collection of $1/f$ noise, normalized for the squared current polarization (I=4.5μA), measured over the S_A, S_B and S_C LPEG films. Also, noise measured on a COTS resistor is present for comparison purposes, describing fundamental current normalized thermal noise of $\sim 4.4 \times 10^{-15}$ [1/Hz] at f=1 kHz, which is superposed to the background noise of the setup instrumentation. At a first glance, S_B film shows again the best performance with the lowest 1/f noise level (8.4×10^{-12} [1/Hz] at f=10Hz) over the S_A and S_C ones (with 1.8×10^{-10} [1/Hz] and 9.0×10^{-11} [1/Hz] at f=10Hz, respectively). It is worth noting that S_A noise spectrum shows a slight bulge in the frequency range [$10^1 - 10^3$ Hz] which is evidence of Lorentzian PSD spectrum presences related to some specific defects in the sample analyzed. Excluding the before mentioned, S_B and S_C LPGE films exhibited a purely $1/f$ noise which is evidence of not particular defects in their conductive surface or volume structure.

Thermal-Electric Characterization Measurements

The electric response to temperature changes was evaluated in the three LPEG films by increasing the temperature of the sample holder film using a singular Thermal Control Module (TCM) described in the chapter 3. Regular steps in the temperature range

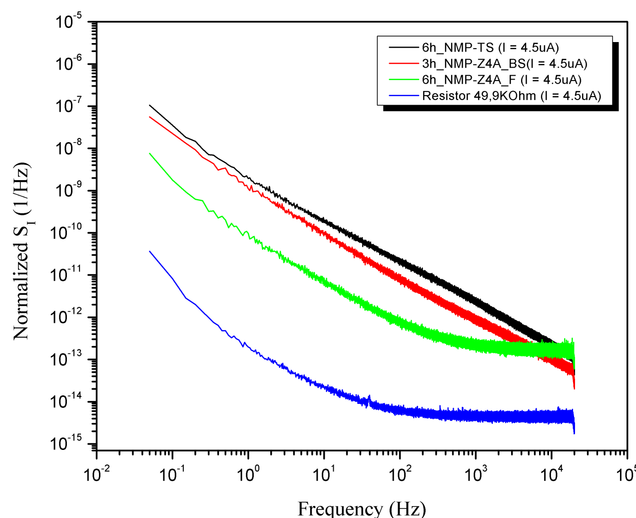


Figure 5.12: Collection of $1/f$ noise, normalized for the squared current polarization (I=4.5μA), measured over the S_A, S_B and S_C LPEG film samples. Also, noise measured on a COTS resistor describing fundamental thermal noise superposed to the background noise instrumentation is present for comparison purposes.

[20–130 °C] were performed, applying the 2D-resistivity characterization method described before. Afterwards, samples were kept at moderated high temperature annealing (T=150 °C) during 3 h in the room laboratory environment. The latter annealing was aimed to test thermal stability and eventual solvent evaporation seeking to avoid the natural oxidation process in the samples. Then, the films were cooling down by conventional heat dissipation. At the end, LPEG films were again thermal-electric characterized to verify whether changes had happened. Figures 5.13a and 5.13b display the 2D-resistivity results obtained before and after of the annealing, respectively, for bias voltage V=0.5 V for all the samples. Results have been deliberately scaled for displaying purpose.

Obtained results demonstrate that resistivity fails down whether temperature increases favoring the current conductance. However, a non-linear dependence in temperature can be observed. It is worth noting that greater current densities could lead to self-heating of LPEG films samples, and by consequence, the decreasing of resistivity starting a positive feedback. Also, it is evident that the annealing enhanced the electric resistivity property of the samples. In fact, all the LPEG samples experienced a resistivity reduction, but particularly, the S_C reduced its resistivity by $\sim 1.75\times$. Another important aspect to highlight was that resistivity changes were maintained in time, which may be explained by evaporation of material (solvent) favoring the interconnection of the LPEG flakes deposited in the samples. Nevertheless, S_B sample remains the better conductive film of such reported in this work, even when its resistivity only was reduced

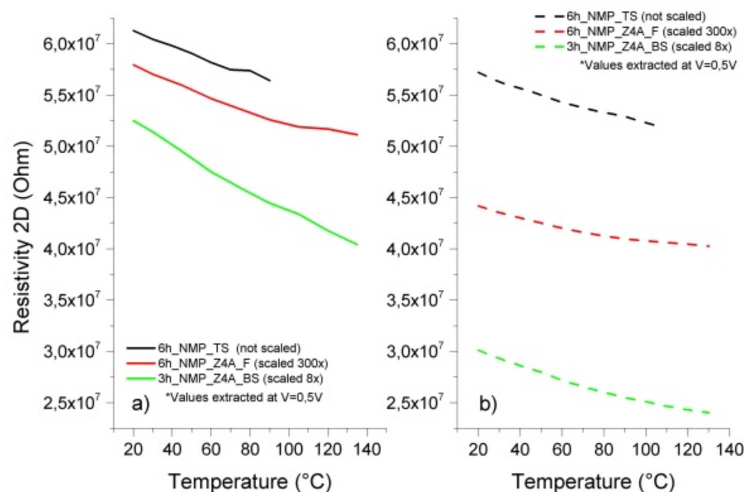


Figure 5.13: Punctual measurements of 2D-resistivity at V=0.5 V in dependence of temperature T. a) Results before the annealing at T=150 °C in laboratory environment. b) Results after the latter treatment. All the results have been deliberately scaled for displaying purpose.

by $\sim 1.3\times$.

Chapter Conclusions

Even if the Low-Frequency Noise (LFN) conceptualization were not deeply reviewed, remains the precedent that LFN spectrum characterization constitutes an excellent diagnostic tool of defectiveness at micro and nanoscopic level in semiconductor devices as that treated in this work: power MOSFETs. Discarding the fact that any instrumentation was developed, and consequently not documented in this work; for the prosecution of the contents presented in this chapter, experimental setups, based in previous works, were adapted to carried out LFN measurements on well different devices and technologies.

Firtly, thermal noise was measured on COTS SMD 1 kΩ resistor testing the experimental setup. The results obtained verified the correct operation of the instrumentation and settled the methodology to follow for further measurements.

Afterwards, LFNM was practised in power n-MOSFET devices, which were stressed using HTRB over-accelerated test. Thus, noise spectrum, characterized before and after the stress, was compared for single device observing interesting behaviours. Moreover, a hard degraded devices described a transition of the noise spectrum from $1/f$ shape, before the stress, toward a quasi $1/f^2$ form, after the stress. The latter was explained a the enhancement of certain RTS noise mechanism as product of the strong increment in the leakage current parameter, which is the result of compromised interface traps

near the channel. Contrary, other device analyzed presented an enhancement of its characteristic $1/f$ noise spectrum after the stress test, which was previously denoted by the presence of a bulge that characterise the RTS noise mechanism activated for a certain interface traps that were cancelled or diffused during the stress test (probably by the thermal activation energies or action of electric fields).

Finally, the main results of a collaborative work on the electrical characterization of Liquid-Phase Exfoliated Graphene (LPEG) films were presented. Initially, the I-V characteristics of the films were determined and compared using the 2D-resistivity parameter. Such a parameter described a parabolic function of the voltage V applied. At this point, the information presented allowing to hypothize a possible explanation for the obtained results. Specific film resistivity was determined at the so-called Charge Neutrality Point (CNP) of the samples. Latter, LFN measurements were performed on the films. The noise spectrum characterized demonstrates that the films are purely $1/f$ noise dominated, but one of them presented a light bulge that could be related to specific defects in the film structure, which is congruent with the higher resistivity in the CNP registered for such a film. Finally, the trend of the 2D-resistivity of the films as function of the temperature was also determined. The resistivity decreases with the temperature increment, which is a clearly signal that the films describe a Negative Temperature Coefficient (NTC). Furthermore, annealing at 150 °C was performed over the LPEG films during 3h. After that, the resistivity was again characterized founding that the values were reduced when compared with the previous ones. Hypothesizing about this phenomenon, some residual solvent material evaporation was considered, which is consistent with the fact that the new resistivity of the films remains.

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Conclusions

This thesis focused on the reliability accelerated tests and instrumentation to carry out High Temperature Reverse Bias (HTRB) test on power semiconductor devices as MOSFET. Standard methodologies in HTRB are not well delimited and can lead to validation errors. Some drawbacks of typical HTRB application can be: long duration of interim measurements, uncontrolled thermal runaway, package explosion of failed devices and uncertainties on the right failure time of devices. Thus, more quantitative and qualitative reliability data during the stress tests is required.

In contrast to such drawbacks, an advanced methodology and automated instrumentation for HTRB testing was reported in this work. As far as the instrumentation is concerned, the strenght is the Thermal Control Module (TCM). Such a module implements a mini-heater that dissipate power in a controllable way to heat a single DUT by joule effect. In a first stage, the mini-heater consisted of a Si SAFeFET (power MOSFET + temperature sensing diode) allowing for 175 °C of temperature stress. On the other hand, the last upgrade of the tool allows for reaching temperature as high as 200 °C by exploiting a SiC power MOSFET and a PT1000. Focusing on the methodology, all the instrumentation features allow for a more frequent cyclic iteration between stress and electrical characterization phase. Thus, a division of the total stress test in shorter cycle duration was proposed, where the electrical characterization can be automatically performed even at higher temperature than room one. As a result, the data collected can reconstruct the progressive deterioration of the DUTs over the time. This instrumentation and methodology have been crucial for reliability study on new technologies devices as SiC, Graphene among others.

Experimentation using the advanced HTRB metholodlgy and instrumentation was performed. One experiment case was the control and detection of Thermal Runaway problem. Moreover, several advanced HTRB tests were performed in COTS power Si n-MOSFETs rated for breakdown voltages of 550 - 650 V. Main results of such experimentations have been used to support the effectiveness of the developed instrumentation and proposed methodology. In particular, the congruence between HTRB results for continuous and cycled HTRB stress test was demonstrated. Further experimentation demonstrated that the advanced HTRB instrumentation can also be used for diagnostic

and investigation purposes. In fact, crucial degradation and density failure information are obtained in shorter time, which is beneficial for R&D of electronic devices. In this ambit, advanced HTRB stress test on power SiC n-MOSFETs rated for 1200 V of breakdown voltage was also performed. A decreasing trend in the accumulated leakage current of the SiC devices characterized the stress. A direct comparison, between the collected data for Si and SiC power MOSFET devices, were displayed for comparison purposes. It was possible to conclude that SiC power MOSFET demonstrates to be advantageous when it is carried to work in high-temperature regime, compared to the Si counterparts. Otherwise, the power loss of the SiC device is comparable to that of its Si ones at room temperatures.

Furthermore, Low-Frequency Noise (LFN) characterization was conceptualized as an excellent diagnostic tool of defectiveness at micro and nanoscopic level in semiconductor devices. Thus, noise characterization using experimental setups available in laboratory was performed on power n-MOSFETs. The devices were stressed using HTRB accelerated test. Thus, noise spectrum, characterized before and after the stress were compared observing interesting diagnostic results. Moreover, a hard degraded device described a transition of the noise spectrum $1/f$ shape, before the stress, toward a quasi $1/f^2$ form, after the stress. The latter was explained as the enhancement of certain noise mechanism (RTS) as product of the strong increment in the leakage current parameter, which is the result of compromised interface traps near the channel. Contrary, other analyzed device presented an enhancement of its $1/f$ noise spectrum after the stress test, which was noted from the cancellation or diffusion of the traps responsible of a bulge presence in the noise spectrum before the stress.

Finally, the main results of a collaborative work on the electrical characterization of Liquid-Phase Exfoliated Graphene (LPEG) films were presented. Initially, the 2D-resistivity of the films was determined through I-V characterisation. 2D-resistivity described a non-linear function when plotted vs. voltage V applied. Specific film resistivity was determined at the so-called Charge Neutrality Point (CNP) of the films. Afterwards, LFN measurements were performed on the films. The noise spectrum demonstrates that the films are purely $1/f$ noise dominated, but one of them presented a light bulge that could be related to specific defects in the film structure, which is congruent with the higher resistivity in the CNP registered for such a film. Finally, the films 2D-resistivity as a function of temperature was also characterized. The resistivity decreases with the temperature increment, which is a clearly signal of a Negative Temperature Coefficient (NTC) property. Furthermore, annealing at 150 °C was performed over the LPEG films during 3h. Afterwards, the resistivity was again characterized founding that the values were reduced when compared with the previous ones. Hypothesizing about this phenomenon, some residual solvent material evaporation was considered, which is consistent with the fact that the new resistivity of the films remains in time.

Summarizing, typical HTRB methodology and drawbacks were revisioned, together with LFN conceptualization. Instrumentation and alternative methodology for advanced HTRB on power MOSFETs was developed and tested. Similarly, noise characterization was practised as a diagnostic tool of defectiveness in stressed power MOSFETs and in the

development of new materials. Important observations and conclusion were performed about the results obtained, when HTRB tests for reliability of semiconductor devices and LFN measurements were combined.

Appendices

Appendix A

Flowcharts Implemented in the Firmware of the HTRB Instrumentation

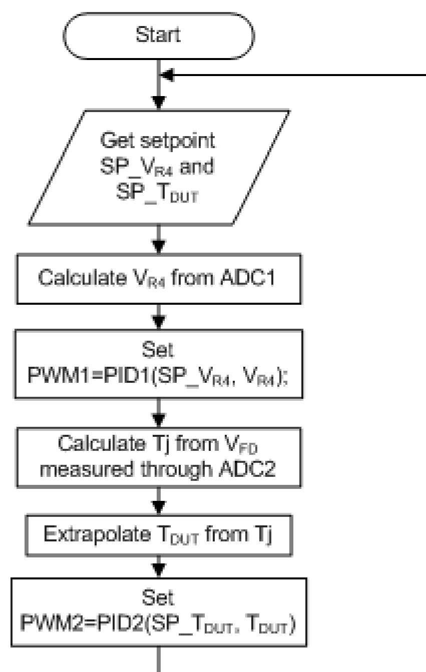

Figure A.1: Summary flow chart of the algorithm (firmware) developed to control the TCM.

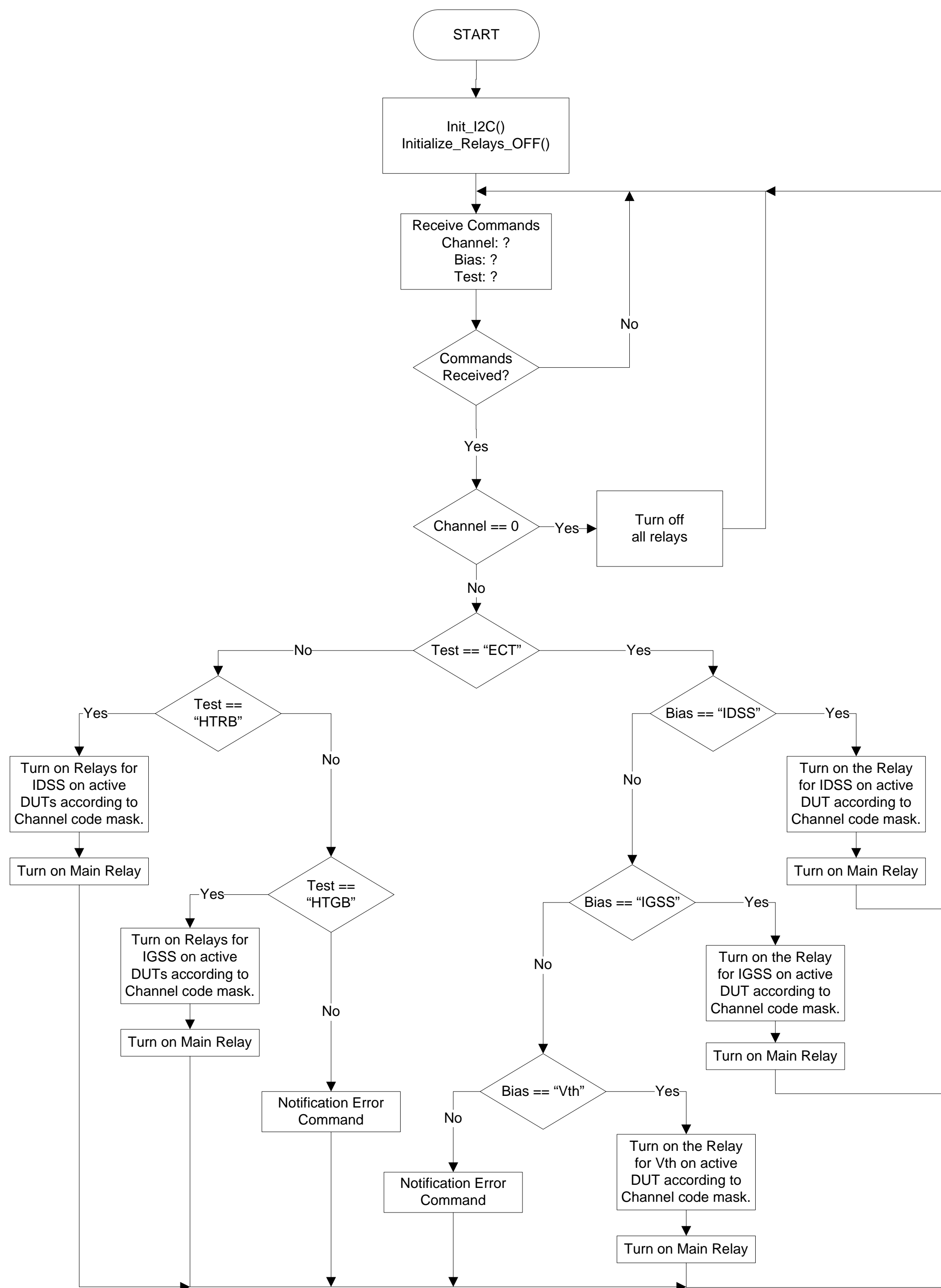

Figure A.2: Simplified flowchart of the control firmware programmed in the Switch Matrix Module (SMM).

Symbols, Constants and Abbreviations

Greek Symbols

α_{eff}	Effective Impact Ionization Rate	cm^{-1}
$\alpha_{n,p}$	Impact Ionization Rate for electrons, holes	cm^{-1}
λ	Failure Rate	failures/s
$\mu_{n,p}$	Mobility of free electrons, holes	$\mathrm{cm}^2/\mathrm{Vs}$
ψ_S	Surface Potential in the channel	V
τ_g	Carrier generation lifetime	s
τ_p	Hole carrier lifetime	s
$\tau_{n0,p0}$	Minority carrier lifetime for electrons and holes	s
ε	Dielectric constant of materials ($\varepsilon_r \cdot \varepsilon_0$)	F/cm

Roman Symbols

A	Active area	cm^2
E	Electric Field	V/cm
h	Planck's constant	J.s
k	Boltzmann's constant (1.38064852×10^{-23})	$\mathrm{m}^2 \cdot \mathrm{kg}/(\mathrm{s}^2 \cdot \mathrm{K})$
q	Elementary charge (1.60218×10^{-19})	As

Subscripts

A_F	Acceleration Factor	
BV_{DSS}	Drain-to-Source Breakdown Voltage	V

$c_{n,p}$	Capture coefficient for electron, holes	$\mathrm{cm}^{-3}s^{-1}$
C_{ox}	Oxide Capacitance	F
D_p	Diffusion constant of holes	$\mathrm{cm}^2.\mathrm{s}^{-1}$
D_S	Sensing Diode	
E_a	Activation Energy	eV
E_F	Fermi level energy	eV
E_i	Intrinsic level energy	eV
E_r	Recombination level energy	eV
E_C	Critical electric field	V/cm
G_{ava}	Avalanche Generation Rate	$\mathrm{cm}^{-3}\mathrm{s}^{-1}$
I_D	Drain Current	A
I_{DSmax}	Total Stress Leakage Current Maximum Limit	A
I_{DSS}	Drain-to-Source Leakage Current	A
I_{GSS}	Gate-to-Source Leakage Current	A
I_{ref}	Reference Current	A
j_r	Reverse current density	$\mathrm{A.cm}^{-2}$
j_r	Reverse current density	$\mathrm{A/cm}^2$
j_s	Diffusion current density	$\mathrm{A.cm}^{-2}$
j_{sc}	Space charge current density	$\mathrm{A.cm}^{-2}$
L_p	Hole diffusion length	cm
$M_{n,p,sc}$	Avalanche multiplication factor for electrons, holes and space charge	
N_A	Acceptor density	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
N_r	Total recombination centers	cm^{-3}
n_r	Electron carrier concentration when $E_F = E_r$	cm^{-3}
N_D	Donator density	cm^{-3}
P_H	Heating Power	W

p_r	Hole carrier concentration when $E_F = E_r$	cm^{-3}
P_{Hmax}	Maximum Power Heating	W
P_{Hth}	Power Heating Threshold	W
Q_S	Total charge in the semiconductor channel	C
R_a	Accumulation region resistance	Ω
R_{ch}	Channel resistance	Ω
R_{DSon}	Drain-to-Source On-Resistance	Ω
R_{epi}	Epitaxial region resistance	Ω
R_{n^+}	Source region resistance	Ω
R_{sp}	Source package resistance	Ω
R_{sub}	Drain substrate resistance	Ω
T_c	Case Temperature	°C
T_j	Junction Temperature	°C
T_o	Operating Temperature	K
T_t	Test Temperature	K
t_t	Minimum Time for Stress Test	s
t_u	Expected Operation Lifetime in Normal Conditions	s
T_{DUT}	Temperature of the Device Under Test	°C
V_r	Reverse voltage	V
V_{bi}	Built-in voltage	V
V_{DS}	Drain-to-Source Voltage	V
V_{FD}	Diode Forward Voltage	V
V_{GS}	Gate-to-Source Voltage	V
V_{ox}	Oxide Voltage	V
V_{th}	Threshold Voltage	V
w_D	Drift region width	cm
w_{sc}	Space charge width	cm

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