UNIVERSITÀ DELLA CALABRIA

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Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica

**Dottorato di Ricerca in**

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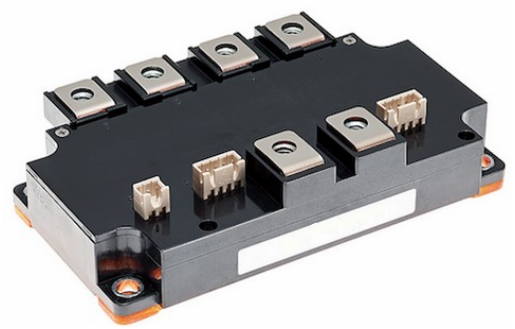
**XXXIII**



# STUDY AND CHARACTERIZATION OF MODERN 4H-SiC POWER MOSFETs

**Settore Scientifico Disciplinare ING-INF/01**

**Coordinatore:** Ch.mo Prof. Felice Crupi

**Supervisore/Tutor**: Ch.mo Prof. Felice Crupi

**Dottorando**: Dott. Giuseppe Consentino

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COSENZA, 03/01/2021

# Contents

# Acknowledgement

I would like to express my sincere gratitude for my tutor and friend Prof. Felice Crupi for his guidance, continuous support and encouragement during this dissertation research. He taught me in the field of transistor noise study and gave me the opportunity to take this challenging course and complete this thesis.

**On the front cover:**
Full-SiC module of power MOSFETs
“https://eepower.com/technical-articles/the-next-generation-of-sic-power-modules/”

*Thank God for all the goals you have allowed me to achieve in my life*

*and for all those that I hope you will allow me to reach in the future*

*To my wife, my daughter*

*and*

*to the memory of my parents,*

*in particular,*

*of my mother*

*who passed away recently.*

*They supported me morally in this enormous effort*

*with their affection and encouragement.*

*"There is nothing more difficult to take in hand, more perilous to conduct,*

*or more uncertain in its success than to take the*

*lead in the introduction of a new order of things."*

*Niccolò Machiavelli in his work entitled "The Prince" of 1513*

# About the author

Giuseppe Consentino was born in Messina (ME), Italy, on July 26, 1972. He received the "Diploma di perito Elettrotecnico", with full grade (60/60) from IT IS "Verona Trento" of Messina (ME), Italy, in 1991. He graduated in Electronic Engineering from University of Messina, Italy, in 1997. He also graduated in Statistical, Demographical and Social Science cum Laude from University of Messina, Italy, in 2005. He obtained the Qualification to the Profession of Engineer from University of Messina in 1998. He also obtained the Qualification to the Profession of Statistical Science from University of Messina in 2005. Currently he is tenured teacher of mathematics at ITE "Luigi Sturzo" in Gela (CL). Previously, until AS 2019/2020, he was tenured teacher of mathematics at the ITCT "Dionigi Panedda" in Olbia (SS). From 3 February 1997 to 24 October 1997, he carried out in the internship in the department NPPD (New Product Power Devices) department of STMicroelectronics of Catania in the power transistors design team. He was hired at STMicroelectronics in Catania on January 7, 1999. Until October 2001, he worked as a device engineer for no-volatile FLASH memory in the Central Front-end Manufacturing team (CFM). From November 2001 until March 2005, he worked as an Senior Application Engineer in the Power Transistor Division (PTD) always in STMicroelectronics. From April 2005 until August 2016, he worked as Senior Design engineer, in particular, for power MOSFETs, in the R&D department of the PTD division. In November of 2011, he was appointed an effective and permanent member of STMicroelectronics' technical staff as an expert in the design and development of power MOSFETs. During his time spent in STMicroelectronics, he was the inventor of four U.S. and European patents:

P1: US20120014057 entitled "Integrated power adapter system for portable computers" in 2010.
https://www.google.com/patents/US8472176?dq=consentino&hl=it&sa=X&ved=0ahUKEwjwqvXmgMzOAhWHyRoKHf9oDRQQ6AEIXTAH;

P2: US20050088859 entitled "Push-pull converter, in particular for driving cold-cathode fluorescent lamps" in 2004.
https://www.google.com/patents/US7423890?dq=consentino&hl=it&sa=X&ved=0ahUKEwjwqvXmgMzOAhWHyRoKHf9oDRQQ6AEIZjAI;

P3: EP1879229A1, US7715159 entitled "Esd protection circuit" in 2006.
https://www.google.com/patents/US20080013231?dq=consentino&hl=it&sa=X&ved=0ahUKEwjYjs2SgczOAhVE2xoKHf_bACg4ChDoAQgkMAE;

P4: US9190492 entitled "Semiconductor device with improved linear and switching operating modes" in 2012.
https://www.google.com/patents/US20140054685?dq=consentino&hl=it&sa=X&ved=0ahUKEwjYjs2SgczOAhVE2xoKHf_bACg4ChDoAQgtMAI.

During his time spent in STMicroelectronics, he has published technical articles in numerous International Conferences as shown below:

C1: G. Consentino, G. Bazzano, “Investigations on electro-instability of low voltage, high-current MOSFETs: Theoretical Models and Experimental Comparison Results for different Structures”, POWER ELECTRONICS TECHNOLOGY, PET, Chicago, USA, 2004.

C2: G. Consentino, G. Bazzano, “Safe Operating Limits In Linear Mode for the latest generation of Low Voltage Power MOSFETs: a mathematical model and experimental results”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2005.

C3: G. Consentino, “Threshold Voltage Thermal Coefficient (TVTC) of Power MOSFETs: Theoretical Study, Measures and Simulation”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2006.

C4: G. Consentino, “How the carriers’ mobility in the transistor channel and its thermal gradient affects the power MOSFET thermal coefficient (TC) during the linear zone operation mode: theoretical study, measurements and simulation”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2007.

C5: G. Consentino, “How the Power MOSFET Inversion layer carriers’ mobility and its thermal gradient affects the TC”, INTERNATIONAL SYMPOSIUM ON INDUSTRIAL ELECTRONIC, ISIE, Vigo, Spain, 2007.

C6: G. Consentino, G. Ardita, “Anomalous Failures in Low-Voltage P-Channel Power MOSFETs during the Intrinsic Diode Recovery Time”, International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM, Ischia, Italy, 2008.

C7: G. Consentino, G. Ardita, “A simplified and approximate power MOSFET intrinsic capacitance simulation: theoretical studies, measures and comparisons”, INTERNATIONAL SYMPOSIUM ON INDUSTRIAL ELECTRONIC, ISIE, CAMBRIDGE , UK, 2008.

C8: G. Consentino, G. Ardita, R. Conti, “Power MOSFET in Linear Zone working as amplifier”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2008.

C9: G. Consentino, G. Ardita, “Power MOSFET working in switching mode: study and analysis of the device’s switching time considering different operating conditions”, AUTOMOTIVE POWER ELECTRONICS, APE, Paris, France, 2009.

C10: G. Consentino, “A new approach to establish the thermal instability condition and the failure time during the drain current focusing process in a power MOSFET working in linear zone”, International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM, Bari, Italy, 2010.

C11: G. Consentino, T. Scandale, “Power MOSFET with integrated poly-silicon diode to monitor junction temperature, with simplified external electrical shutdown circuit to prevent thermal runaway”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2009.

C12: G. Consentino, A. Perri, “MOSFETs or IGBTs in the modern ERC and Sustain Modules of PDPs? An empirical approach for choosing suitable Power Switches”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2010.

C13: G. Consentino, “Power MOSFETs reliability during harsh power cycling and the importance of the temperature control technique”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2011.

C14: G. Consentino, A. Gaito, “Which Power MOSFET technologies in LLC HB converters?”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2012.

C15: G. Consentino, “Power MOSFETs working in Linear Zone: the dangerous effect of the K gain factor on thermal instability”, International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM, Sorrento, Italy, 2012.

C16: D. Cavallaro, G. Consentino, “Irradiated HV Power MOSFETs working in Linear Zone: a comparison of electro-thermal behavior with standard HV products”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2013.

C17: S. La Mantia, G. Consentino, “Gate oxide defectiveness levels: an experimental comparison between Planar and Trench Low Voltage Power MOSFET technologies”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2013.

C18: G. Consentino, M. Laudani, G. Privitera, C. Pace, C. Giordano, J. Hernandez, M. Mazzeo, “Effects On Power Transistors Of Terrestrial Cosmic Rays: Study, Experimental Results and Analysis”, POWER ELECTRONICS TECHNOLOGY, PET, Forth Worth, USA, 2014.

C19: G. Consentino, Y. Damante, “Study of the dependence between the dissipated power and the inductance when an HV power MOSFET works in UIS passive mode test”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2014.

C20: G. Consentino, “P-channel Power MOSFETs working in Lineare Zone: theoretical and experimental studies and comparison with N-channel devices”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2014.

C21: G. Consentino, M. Laudani, M. Macauda, C. Pace, C. Giordano, J. Hernandez, “Are SiC HV power MOSFETs more robust of standard silicon devices when subjected to terrestrial Neutrons?”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2015.

C22: G. Consentino, “HV Power MOSFETs working in Linear Zone: performances comparison between standard Planar and SJ devices”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2015.

C23: F. Scrimizzi, G. Bazzano, D. Cavallaro, M. Comola, G. Consentino, S. Fortuna, G. Longo, G. Pignataro, “New LV Wide SOA Power MOSFET technology for Linear Mode operation”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2016.

C24: A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, A. Magrì, “Thermal instability of low voltage power-MOSFETs”, 30$^{th}$ Power Electronics Specialists Conference, PESC, 1999.

C25: G. Consentino, D. Corona, A. Grimaldi, S. Pisano, G. Sammatrice, “A hole barrier IGBT with enhanced breakdown voltage by floating P-well",2012,"PCIM Europe Conference Proceedings”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2012.

C26: G. Consentino, M. Laudani, G. Privitera, A. Parlato, N. Marchese, E. A. G. Tomarchio, C. Pace, C. Giordano, M. Mazzeo, J. Hernandez, “Dangerous effects induced on power MOSFETs by terrestrial neutrons: A theoretical study and an empirical approach based on accelerated experimental analysis”, Associazione Elettronica Informatica Telecomunicazioni, AIET, Palermo, Italy, 2013

C27: G. Consentino, D. De Pasquale, S. Galiano, A. D’Ignoti, C. Pace, J. Hernandez, M. Mazzeo, C. Giordano, “Innovative instrumentation for HTRB tests on semiconductor power devices”, Associazione Elettronica Informatica Telecomunicazioni, AIET, Palermo, Italy, 2013.

During his time spent in STMicroelectronics, he has published technical articles in numerous International Journal as shown below:

J1: A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, A. Magrì, “Thermal instability of low voltage power-MOSFET's”, IEEE Transactions on Power Electronics, 2000.

J2: C. Pace, S. Pierro, V. Cilia, G. Consentino, “A model for avalanche breakdown calculation in low-voltage trench power MOSFET devices”, Semiconductor Science and Technology, 2012.

J3: C. Pace, J. Hernandez-Ambato, D. De Pasquale, G. Consentino, “Instrumentation for Innovative Semiconductor Power Devices Reliability Tests”, International Journal of Engineering and Industries, IJET, 2013.

J4: I. Bertuglia, G. Consentino, M. Laudani, “Proton Irradiation on SJ HV Power MOSFETs to Realize Fast Diode Devices”, HINDAWI, 2014.

J5: C. Pace, J. Hernandez-Ambato, L. Fragomeni, G. Consentino, A. D’Ignoti, S. Galiano, A. Grimaldi, “A new Effective Methodology for Semiconductor Power Devices HTRB Testing”, IEEE Transactions on Industrial Electronics, 2017.

He was also a company tutor for thesis students as listed below:

T1: “PDP: study and analysis of the whole system placing particular attention on the Sustain and ERC modules and on the power switches used on them”, Università della Calabria, student: Andrea Perri, Supervisor: Prof. Felice Crupi.

T2: “Studio e caratterizzazione di un power MOSFET con integrato un diodo per la misura della temperatura di giunzione. Implementazione e realizzazione di un circuito elettrico esterno che traduce la tensione di forward del diodo in un segnale elettrico proporzionale alla temperatura di giunzione”, Università della Calabria, student: Tommaso Scandale, Supervisor: Prof. Felice Crupi.

T3: “Studio della generazione e della trasmissione del calore all'interno dei power MOSFET: teoria, simulazioni e misure”, Università della Calabria, student : Antonio Furlano, Supervisor: Prof. Felice Crupi.

T4: “Studio di un SMPS di tipo Flyback con particolare riferimento al funzionamento del power MOSFET e all'analisi della stabilità del sistema”, Università della Calabria, student : Domenico Pingitore, Supervisor: Prof. Felice Crupi.

T5: “Progettazione e realizzazione di un SMPS di tipo HB per applicazioni industriali con particolare riferimento al funzionamento del power MOSFET”, Università della Calabria, student: Antonio Bianco, Supervisor: Prof. Felice Crupi.

T6: “A forward DC/DC Converter for Aerospace Application. Realizzazione e test di un convertitore DC/DC Rad-Hard”, Università della Calabria, student: Andrea Palmieri, Supervisor: Prof. Calogero Pace.

# List of publications during the PhD course

## INTERNATIONAL CONFERENCES AND JOURNALS

C1: C. Parisi, G. Consentino, V. Martino Cinnero, Y. Damante, A. Grimaldi, D. Murabito, “Evaluation of Miller capacitance depending on drain-source voltage when SJ HV Power MOSFETs are in reverse mode”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2018.

C2: G. Consentino, E. Guevara, F. Crupi, L. Sanchez, S. Reggiani, G. Meneghesso, “Threshold Voltage Instability in SiC Power MOSFETs”, POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY, PCIM, Nuremberg, 2019.

C3: G. Consentino, E. Guevara, F. Crupi, L. Sanchez, S. Reggiani, G. Meneghesso, “Threshold Voltage Instability in SiC Power MOSFETs”, First International Workshop, Tours, France, 2019.

C4: G. Consentino, “On the reversible Threshold Voltage Shift in SiC power MOSFETs”, XXV International congress of aeronautics and astronautics, AIDA, Rome, Italy, 2019.

C5: D. Cornigli, A. N. Tallarico, S. Reggiani, C. Fiegna, E. Sangiorgi, L. Sanchez, C. Valdivieso, G. Consentino, F. Crupi, “Characterization and Modeling of BTI in SiC MOSFETs”, 49$^{th}$ European Solid-State Device Research Conference, ESSDERC, Krakow, Poland, 2019.

J1: G. Carangelo, S. Reggiani, G. Consentino, F. Crupi, G.Meneghesso, "TCAD Modeling of Bias Temperature Instabilities in SiC MOSFETs", submitted to Solid-State Electronics, special issue devoted to INFOS2021

# Abstract of the dissertation

This PhD thesis is focused on the study and characterization of the defectiveness observed in the interface between the substrate and the oxide of modern SiC power MOSFETs. In particular, all analyses carried out in this work have been implemented on two different families of devices having the same planar technology, different die size and having a breakdown voltage equal to 1200 V. This PhD thesis work was included in the framework of the European project WInSiC4AP (Wide Band Gap Innovative SiC for Advanced Power) in which the DIMES department of UNICAL participates through the IUNET consortium. The dissertation is divided in two parts. The first part, chapter 2 and chapter 3, introduces the state of art of power MOSFET technologies. In these chapters, the properties of the SiC material are also discussed and a comparison is made with the silicon. In these chapters the theoretical bases of the experiments carried out on the tested devices are also introduced. In the second part of this thesis the experiments conducted on the tested devices are described in detail and the results have been carefully analysed and explained. The experiments conducted concern the threshold voltage instability phenomenon, the BTI and the analysis of flicker noise observed in the SiC power MOSFETs analysed. Simulations based of on the threshold voltage instability phenomenon and on the BTI tests were carried out using the TCAD. The conclusions obtained by the experimental results of these tests have also been validated by some spectroscopic analyses conducted by the CNR team in Catania also within the European project WInSiC4AP.

# 1 Introduction

Power electronics is a branch of electronics that deals with devices and applications for high currents and high voltages. Generally, the applications of power electronics are the DC-DC power converters used, for example, to supplier energy for computers, laptops, mobile phones, etc…, and inverters used to convert DC voltages in AC voltages in photovoltaic applications or in motor control applications. However, power electronics involves many other application segments relating to the automotive, lighting, health care, space, avionics, etc… The power electronics devices placed within the applications are resistors, inductors, capacitors, drivers and, in particular, power transistors. Typical power transistors are Bipolar Junction Transistors, BJTs, Insulated Gate Bipolar Transistors, IGBTs, and power Metal Oxide Semiconductor Field Effect Transistors, power MOSFETs. In many cases, these components are used as switches to commutate from on state to off state and vice versa. BJTs have been widely used in power electronics in linear amplifiers and lighting applications for many years up to past two decades. However, they have been replaced by power MOSFETs and IGBTs even if they are used again in low-end applications, small signals and very high voltages (over 1800V). In fact, BJTs are bipolar devices, thus, the conduction mode involves both electrons and holes and cannot be effectively used in high frequency applications due to the higher switching times when compared, in particular, with n channel power MOSFETs which are unipolar devices. In addition, longer switching times result in higher switching losses which reduce the efficiency of entire system. Another disadvantage regarding BJTs is that the base is not insulated as in IGBTs and power MOSFETs, thus, this leads to greater current leakages when driving transistors. IGBTs are basically BJTs with insulated gate terminal, so the leakage currents are comparable to the power MOSFETs when driving the devices. They are used as switches in applications that manage high power and high voltages such as, for example, motor controls for washing machines and welders. They are preferred over BJTs because they can be used in applications that require higher switching frequencies. In some applications, conduction losses becomes predominant over switching losses. Power transistors such as BJTs and IGBTs have lower conduction losses than power MOSFETs because both charges, electrons and holes, are involved in the conduction mechanism and reduce resistance in the on state. However, nowadays, power MOSFETs are largely the most used power transistors in power electronics applications, in particular, if we consider applications that can work at very high frequencies, above 100KHz, and when they have to manage medium and low power levels. Since they were introduced, power transistors have been made with silicon and this semiconductor is still the main choice today. At any rate, worldwide, reducing energy consumption and efficient energy management have become two of the biggest challenges of the modern times. The most used form of energy is the electricity generated, in the most of cases, by fossil fuels that create environmental pollution. Furthermore, even if renewable sources have been introduced to increase the ability to produce clean energy, traditional energetic resources are decreasing with the passage of time, thus, it is necessary to optimize their use by avoiding waste. In power electronics, minimizing losses in power devices can result in a significant increase in the reduction of the overall energy consumption. In case of power transistors and, in particular, power MOSFETs, the designers have implemented various suitable actions to reduce the conduction and switching losses in the standard silicon based devices. In fact, the improvement of processes in all manufacturing phases, such as lithography, oxidation, etching, also thanks to the use of new high-performance equipment, together with the introduction of new design technologies, such as the trench and the super-junction, have made it possible to drastically reduce the size of the devices while also reducing their losses in order to

approach the limits imposed by silicon. Furthermore, from another point of view, power applications manufactures require very high performance power transistors for specific segments of high end applications in order to drastically increase the switching frequency to reduce the size of magnetic components and, thus, the volume and the weight of the whole system and significantly increase the power density managed. Silicon has been for long time, and will still be used for many years to produce electronics components because it is present in large quantities in the earth, is available at low cost and can be easily processed to produce wafers. However, in this new scenario, new semiconductor materials have recently been introduced to greatly improve the performances of power transistors in order to overcome the physical limits of silicon. These new materials are called Wide Bandgap semiconductors, WBG, because they have a greater energy bandgap than silicon. Today, the two main WBG semiconductors used to replace silicon are gallium nitride, GaN, and silicon carbide, SiC. Both materials allow to significantly increase the switching frequencies, since they have a higher electron saturation speed, reduce the switching losses, increase the breakdown voltage and decrease the resistance in the on state compared to silicon devices. In particular, the higher bandgap allows to work at higher electric field values since the impact ionization energy is higher than silicon. In fact, the critical electric field in SiC is an order of magnitude higher than silicon. Furthermore, the higher bandgap allows to obtain a much smaller concentration of intrinsic carriers in SiC and GaN compared to silicon, thus, WBG devices can work at very high temperatures. In particular, the SiC material has excellent thermal conductivity which improves power dissipation and allows operating at very high current densities. The main advantages of SiC and GaN materials compared to silicon are summarized in figure 1.1. However, SiC has a big advantage over GaN in power MOSFETs. In fact, native silicon dioxide can be grown by means of a simple thermal oxidation as in case of silicon devices. Another advantage of SiC is that high quality monocrystalline bulk substrates they can be grown at 4” or even 6”. Instead, GaN is available in monocrystalline bulk substrates smaller than SiC and with extremely expensive manufacturing processes. Therefore, GaN monocrystalline bulk substrates are usually grown on silicon or sapphire substrates by heteroepitaxy processes. However, due to the lattice mismatch between GaN and silicon, many crystallographic defects are created in the active region of the device [1]. Furthermore, in GaN transistors the current generally flows horizontally while in silicon and SiC devices it flows vertically from the top to the bottom of the die to strongly increases its density. In fact, it has been observed that when making vertical GaN devices the breakdown voltage is lower and the leakage currents increase with respect to the horizontal transistors [2]. Therefore, the ability to hold high voltages in GaN devices is reduced compared to SiC transistors and, thus, they are designed to operate in low and medium voltage applications (a few hundreds of volts maximum). However, one of the main problems observed in SiC power MOSFETs concerns the high density of defects in the SiC-$SiO_2$ interface compared to the silicon devices that can cause reliability problems. In fact, it has been experimentally observed that the density of the interface defectiveness in SiC transistors can be even two orders of magnitude higher than in silicon devices. It has been observed that the interface traps in SiC devices are thermally activated and it is in stark contrast to what has been seen in silicon transistors. Consequently, the mobility of charge carriers in the channel can be at least one order of magnitude lower than the theoretical value and certainly lower than mobility measured in the silicon devices. The lower channel mobility observed in SiC devices significantly increases the channel resistance and for this reason the SiC power MOSFETs are designed to work in high or very high voltage applications where most of the resistance is mainly due to the drift region that supports the drain-source voltage applied during the off state. Finally, the high defectiveness observed in the interface region of SiC power MOSFETs entails reliability problems as instability of the threshold voltage.

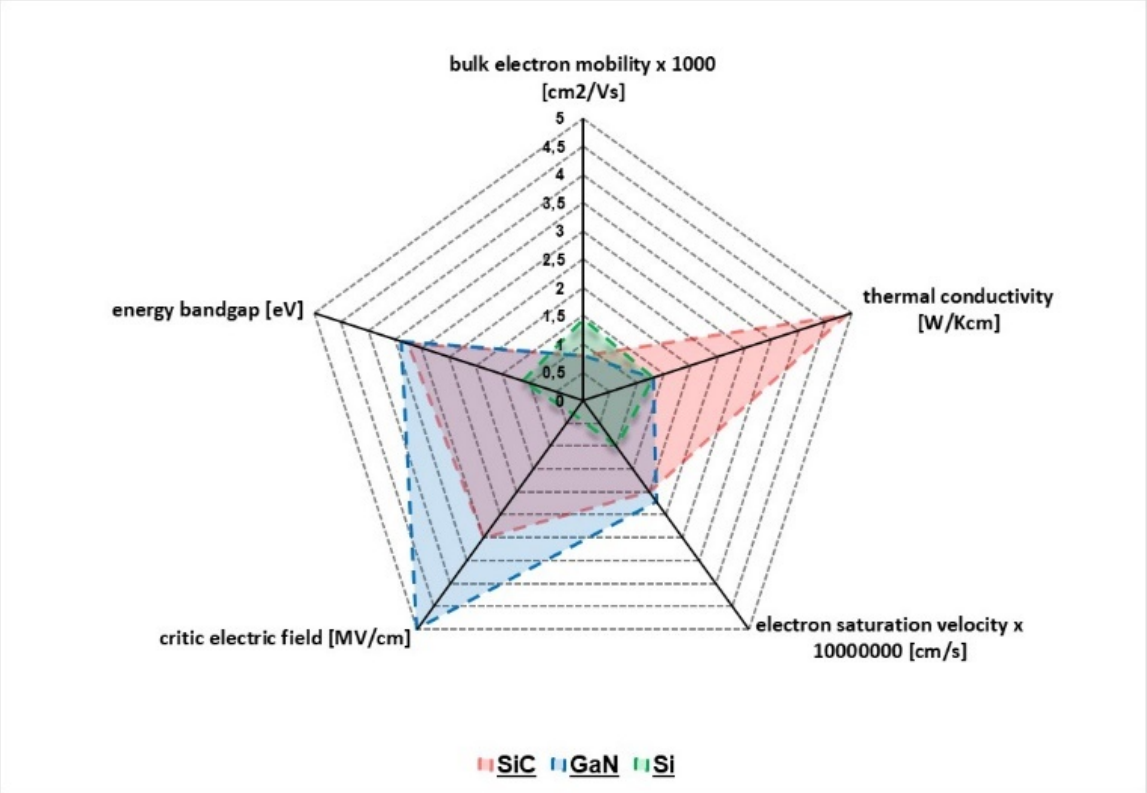



**Figure 1.1: Most relevant material properties of Si, SiC and GaN [5].**

# 2 Power MOSFET transistors

## 2.1 Evolution of Power MOSFET technologies

Power devices based on semiconductor materials were developed in the second half of the last century to replace large and less reliable vacuum tubes. The first commercial semiconductor device was introduced in 1954 and was a silicon based Bipolar Junction Transistor (BJT) [77]. BJT devices have been widely used for several tens of years. However, since the end of the last century they have been gradually replaced by power MOSFETs in many electronic applications even though BJTs are still used in some low-end power electronics applications [81], [92]. Indeed, it has been shows that BJTs cannot be used successfully in many new power applications due to some problems [78], [79]. One of these problems is related to the possibility that BJTs goes into thermal runaway because the coefficient between temperature and the current is positive [82]. The second point concerns the charge stored in the base of BJTs which makes the device slow during the switching regime [83], [84]. In fact, in modern devices, the switching frequencies of the BJTs do not exceeds 100kHz. Furthermore, BJTs are subjected to the phenomenon of the secondary breakdown which leads to failure of the transistors [85], [86] and have a very low base resistance which implies the passage of a high current for driving the devices [87]. Instead, power MOSFETs have the oxide and the gate current is very low because the input impedance is very high. In addition, power MOSFETs are unipolar devices and thus the charge due to minority carriers does not accumulate in the devices, thus, they are capable of supporting high switching frequencies [88]. Nowadays, considering the most advanced technologies, power MOSFETs are able to switch even beyond 300KHz. The power MOSFETs have a negative coefficient between the temperature and the current and do not go into thermal runaway, thus, power MOSFETs can be connected in parallel. However, the power MOSFETs have a greater resistance in the on state compared to the BJTs which leads to higher conduction losses. At any rate, in recent years, this disadvantages has been limited thanks to the improvements introduced in the technologies and materials of power MOSFETs that have greatly reduced the $R_{DSON}$ with the same die volume. However, lateral planar technology MOSFETs are not suitable for use in power applications due to DIBL problems [89], the breakdown voltage snapback phenomenon and GIDL problems near the drain [90]. Therefore, in the modern power MOSFETs, the current flows in a vertical direction from the source to the drain of the devices. The only lateral planar power MOSFETs used concerns LDMOS technology in which a light doped region is introduced into the edge of the drain to limit the drawbacks just described. However, LDMOS power MOSFETs are used only in power applications for radio frequency because they have a very limited integration capability compared to vertical devices. MOSFETs were invented by Atalla and Kahng in 1959 at Bell Labs. The first vertical power MOSFET prototype called VMOS was produced only in 1969 thanks the introduction of a V-groove shape in the gate region [80] (see figure 2.1.1). As can be seen in this figure, the current flows vertically from the drain to the source (even if in n-channel devices electrons flow in the opposite direction). The drain contact is placed on the bottom of the die while the source wells are placed on the surface. The gate structure is placed inside the substrate between two adjacent source wells. The channel is created in the interface region between the substrate and the gate oxide. The drift region allows to sustain the voltage applied between the source and the drain during the off state since the body-drift junction is reverse polarized. In particular, the drift layer is slightly doped with respect to the body region and, thus, the depletion region will widely extend along the drift layer. VMOS structures can be considered the first prototypes of modern Trench power MOSFETs.

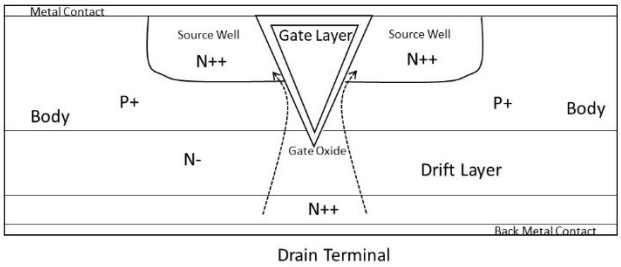



**Figure 2.1.1: Cross section of a cell of a n-channel power MOSFET with a VMOS gate structure.**

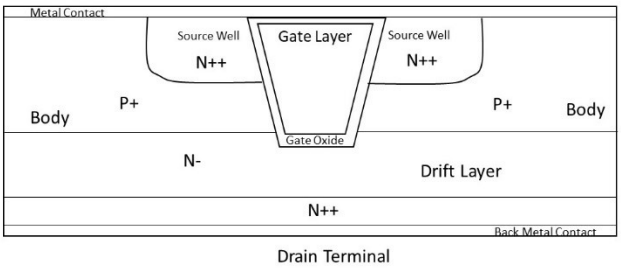



**Figure 2.1.2: Cross section of a cell of a n-channel power MOSFET with a UMOS gate structure.**

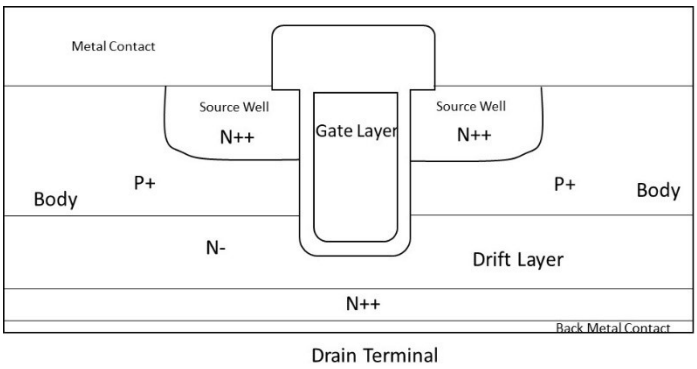



**Figure 2.1.3: Cross section of a cell of a n-channel Trench power MOSFET (UMOS of the gate structure).**

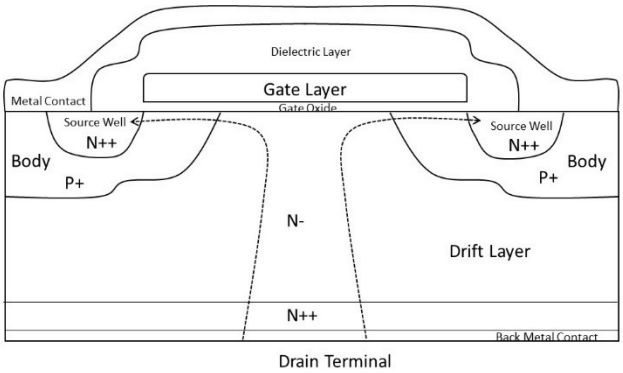



**Figure 2.1.4: Cross section of a cell of a VDMOS n-channel power MOSFET.**

As can be seen in the same figure, power MOSFETs have an intrinsic BJT component composed of the drift and body regions. This intrinsic bipolar component could be activated if a sufficient current flows in the base (body) due to a snapback of the voltage of the device.

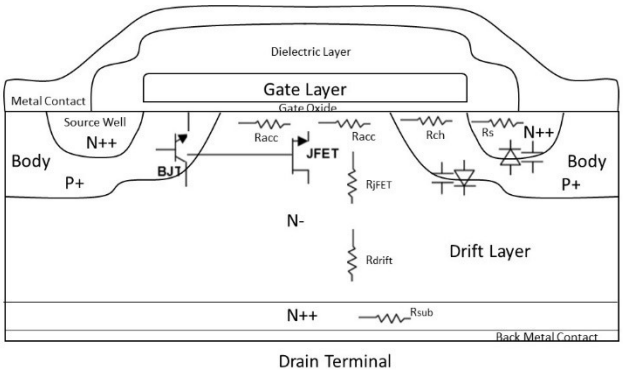



**Figure 2.1.5: Cross section of a cell of a n-channel VDMOS power MOSFET which highlights the parasitic components.**

Therefore, the body and source regions (the source is the BJT emitter) must be short-circuited and the concentration of the body layer must be high enough to reduce the base resistance and disable permanent bipolar conduction [91]. However, the VMOS structure of a power MOSFET is used to make low voltage devices due to the crowding of electric field lines on its bottom of the gate which does not allow to obtain particularly high breakdown voltages [93]. Subsequently, this problem was partially solved by smoothing the V-shape of the gate into a U-shape (see figure 2.1.2). Only in 1985, thanks to the introduction of the Reactive Ion Beam Etching (RIBE) process [94], a perfect rectangular groove was created in the gate structure which almost entirely solved the phenomenon of crowding the electric field (see figure 2.1.3). However, nowadays, commercial silicon-based Trench power MOSFETs are designed to withstand breakdown voltages up about to 200V even if they also starts to be used in high voltage applications together with other technical solutions that will explore later. The most common structure of power MOSFETs is planar VDMOS (Vertical Diffused MOS) as shown in figure 2.1.4. In VDMOS power MOSFETs, the gate structure is made in the upper part of the substrate and the source wells are doubly diffused in the body regions. As in case of Trench power MOSFETs, the current flows in vertical direction. VDMOS power MOSFETs are planar devices because the gate oxide has thermally grown on the die surface. The VDMOS structure introduces a parasitic JFET component that does not exist in Trench devices. The JFET is composed of the P+ regions of two adjacent cells and the drift layer between them. The JFET transistor introduces an additional resistive component to the $R_{DSON}$ called $R_{JFET}$. When VDMOS power MOSFETs work in the on state, a suitable positive polarization is applied on the gate terminal and a carrier accumulation layer is created under the interface in the intercell region. This accumulation layer, composed of electrons in n-channel devices, introduces a new resistive component which is added to the $R_{DSON}$ called $R_{acc}$ which does not exist in the Trench power MOSFET. Others resistive components of $R_{DSON}$ are $R_{drift}$, due to the drift layer, $R_{sub}$, due to the epitaxial layer N++, $R_s$, due to the source regions. Furthermore, it is also necessary to consider the resistance introduced by the wires, which connect the die to the package, the contact resistances of the source, drain and substrate, and the resistance of the lead frame ($R_{wcml}$) (figure 2.1.5). Therefore, $R_{DSON}$ is equal to:

$$R_{DSON} = R_s + R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{sub} + R_{WCML} \quad (2.1.1)$$

Typically, $R_s$ and $R_{acc}$ can be neglected if compared to other resistive components of the $R_{DSON}$. All these resistive components differently affect the $R_{DSON}$ of a standard silicon VDMOS device based on the breakdown voltages for which they were designed (see figure 2.1.6 referenced to typical commercial devices [7] ). As can be seen in this figure, in a 500V silicon device, $R_{drift}$ is about 60% of the entire $R_{DSON}$ while its contribution decreases for devices that have lower breakdown voltages.

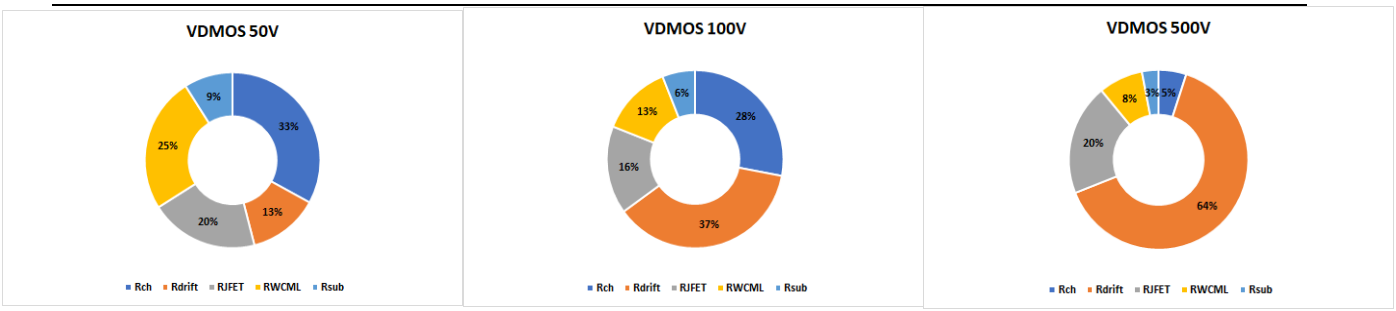



**Figure 2.1.6: Contribution of the different resistive components of $R_{DSON}$ for VDMOS devices in silicon having different $BV_{DS}$ and referenced to typical commercial devices [7].**

In fact, the greater the breakdown voltage the greater the depth of the drift layer and the related resistive component. Instead, the contribution of $R_{JFET}$ increases slightly in a range of 15-20% of $R_{DSON}$ to the increase of the breakdown voltage. $R_{ch}$ is about 30% of $R_{DSON}$ for devices with breakdown voltage up to 100V. Instead, in 500V devices, its contribution decreases rapidly down to 5% of $R_{DSON}$ becoming almost negligible. The other components of $R_{DSON}$, $R_{sub}$ and $R_{wcml}$, maintain the same resistance values as the breakdown voltage increases but their contribution decreases because $R_{DSON}$ increases due to the growth of $R_{drift}$. $R_{JFET}$ does not exist in Trench transistors, thus, they are the preferred solution for making devices with breakdown voltages up to 200V. Instead, for device with a higher breakdown voltage, it is necessary to introduce new technologies and/or materials that allow to reduce the impact of the $R_{drift}$ as will discussed later in this chapter. It is also important to note that the capacitances and diodes relating to the body-drift and source-body junctions respectively are also included in figure 2.1.5. In particular, the diode due to the body-drift junction is used in some applications as freewheeling diode as, for example, in boost converters. If used in this operating conditions, the diode must be able to quickly switch from the on to the off states and vice versa, thus, the lifetimes of the carriers in the junction region must be very low. To create very fast diodes, permanent damages are created in the body-drift junctions through ionizing radiations with electrons, protons or helium or, still, in some other cases, through thermal diffusion of gold or platinum atoms [123]. These damages create traps within the semiconductor bandgap which reduce the lifetimes of the carriers due to SRH generation and recombination processes. One of the main goals of power MOSFET manufactures is to minimize $R_{DSON}$, die size and intrinsic capacitance components. The decrease in $R_{DSON}$ allows to reduce the conduction losses while the decrease in the die size allows to lower the switching losses and, thus, to increase the switching frequency. $R_{DSON}$ can be reduced by acting on each of the resistive components of which is composed. For example, it is possible to reduce $R_{ch}$ by decreasing the length of the channel and thickness of gate oxide through a process of scaling of the technology (front-end process). Instead, $R_{wcml}$ can be decreased by optimizing the diffusion processes of the source, introducing new more performing materials and improving the metallization processes (back-end process). Finally, $R_{sub}$ can be reduced by acting on the back of the wafer by means of chemical and mechanical scrubber processes which thins the substrate thickness or by using degenerate substrates to reduce the resistivity of the same. Regarding the Trench power MOSFETs, even after the introduction of the RIBE process [94] and the planarization of the bottom of the trench, other process innovations have been introduced to create reliable devices such as shielding of the electric field in the Trench region, the introduction of a sacrificial oxide before realizing the gate structure, the protection against avalanche multiplication phenomena of the carriers. The introduction of a fully planarized polysilicon gate in the Trench region was initially proposed by Blanchard [95], [96]. In this process of making the Trench, the source and body regions are firstly implemented through a double diffusion of the dopant, thus, the Trench is created which has a width of about 0.8-1.5µm.

Subsequently, the etched region is oxidized to grow the gate oxide and, finally, it is filled with in situ doped polysilicon with phosphorus through a Chemical Vapor Deposition process, CVD. The polysilicon completely fills the Trench and overflows, thus, it must be etched in surface. The polysilicon is slightly overlapped with the source wells and these geometries are made through a recessed etching process as shown in figure 2.1.3. The process of the Trench gate can be optimized through thermal oxidation which seals the recessed polysilicon with a protective oxide layer. Alternatively, instead of growing the protective oxide, it can be deposited by the CVD process after the oxidation phase of the polysilicon. This protective layer of oxide must be etched with a suitable mask since a metallization layer will be deposited to contact the source wells. The oxide etching can be performed by a wet chemical etch containing HF acid or a plasma dry etch or, also, by a combination of both methods. After the deposition of the metal layer, the photolithographic patterning are performed by interconnecting the distinct VDMOS cells of the Trench to create the power MOSFET. It has been experimentally proved that the resulting cell pitch was half that obtained with any other vertical device, thus, this leads to a strong increase in the cell density and a decrease of the $R_{DSON}$ [92]. However, due to the variability of the process in fixing the depth of the diffused regions of the body and the Trench, avalanche multiplication phenomena could occur when the device is reverse polarized in the area near the bottom of the gate oxide which can cause both catastrophically rupture and permanent damages in the dielectric due to the injection of hot carriers. Therefore, in 1987, Blanchard proposed to grow a thick bottom oxide (TBOX) [97]. An interesting alternative approach to solving the problem was subsequently proposed by Bulucea and Rossen by introducing a deep diffusion p++ between two adjacent cells as shown in figure 2.1.7 [98], [99]. However, a small drawback with regard to this solution is related to the spreading of the current in the drift region and to the higher intercell space that must be created between the p++ wells and this increases the $R_{DSON}$ a little. Another solution was also proposed by Baliga in 1999 introducing oxides with graduated thickness along the vertical direction of the wall-shaped die to smooth the electric field near the bottom of the gate structure [100]. Furthermore, the peak of the electric field in the edges of the bottom of the gate structure can be greatly reduced rounding the corners of the gate oxide and optimizing the curvature of the edges, the oxide thickness and the doping concentration by using appropriate annealing processes in a hydrogen environment to increase the breakdown voltage of the Trench power MOSFETs [101]. It has been observed that while optimizing the depth of the Trench and the length of the drift region, it is possible that an increase in the breakdown voltage may occur [132]. As already explained, the drift region sustains the $V_{DS}$ voltage when the device is turned off since it is slightly doped with respect to the body. In any case, the low doping concentration increases the resistivity of the layer which leads to an increase in the $R_{drift}$ and, thus, in the $R_{DSON}$. This phenomenon is more marked in high voltage devices because the drift region is deeper. Therefore, it is necessary to reach a trade-off between the two electrical parameters in the designing phase to optimize the performances of the transistors considering the specific power applications in which power MOSFETs are used. The relationship between $R_{DSON}$ and breakdown voltage, $BV_{DS}$, in silicon-based power MOSFET technologies is proportional to [102], [107]:

$$R_{DSON} \propto BV_{DS}^{2.5} \tag{2.1.2}$$

However, the introduction of new technologies has improved the trade-off between $R_{DSON}$-$BV_{DS}$ as in the case of Super Junction devices, SJ, where some floating islands are inserted in the drift layer and also through the Reduced Surface Field (RESURF) techniques based on the lateral charge balancing principle [106], [109]. In particular, SJ devices show an almost linear relationship between $R_{DSON}$-$BV_{DS}$ [103]:

$$R_{DSON} \propto VB_{VDS}^{1.03} \tag{2.1.3}$$

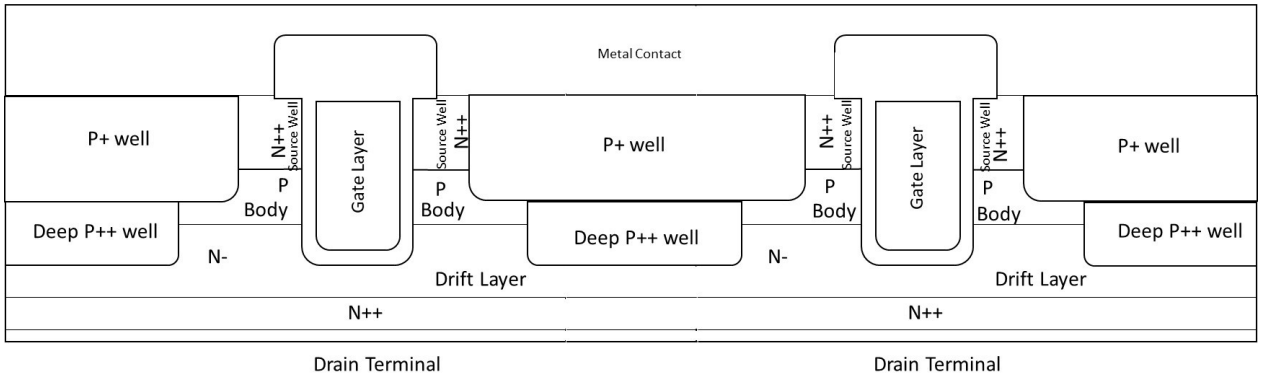



**Figure 2.1.7: Cross section of a n-channel Trench power MOSFET with p+ deep regions between two adjacent cells.**

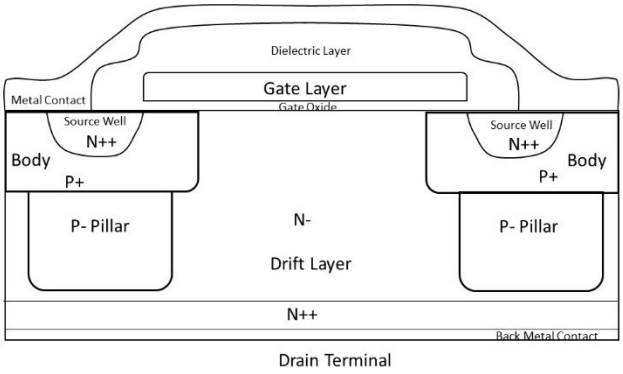



**Figure 2.1.8: Cross section of an SJ cell of a n-channel VDMOS power MOSFET with floating islands of elliptical shapes.**

In fact, the addition of suitable floating islands within the drift region under the body changes the distribution of the electric field in the same drift region creating several small peaks depending on the number of floating islands, thus, avoiding having a single high peak [104]. This technique greatly increases the $BV_{DS}$ by decreasing the depth of the drift region and also significantly reducing the $R_{drift}$ (see figure 2.1.8) [105]. In addition, this technique also improves the performances of the body-drift intrinsic diode because it increases its switching speed. However, the floating islands in the drift region layer increase the effects produced by the JFET of the power MOSFETs which make $R_{DSON}$ partially grow, in particular, during the switching regimes. This latter drawback was solved by introducing passive hole gates to control the density of minority carriers [105]. The typical shapes of the floating islands used during the multiple diffusion processes by power MOSFETs manufactures have elliptical forms. From figure 2.1.8, when the body-drift junctions are reverse polarized, it is seen that the electrical field in the drift layer is arranged both along the horizontal direction and along the vertical one. Furthermore, pillars made under the P+ doped body regions do not cause any effect during the on state of the device but only contribute to increase the $BV_{DS}$. When they are reverse polarized, pillars deplete completely before reaching the breakdown and the profile of the electric field becomes almost flat along the vertical direction since there are only small electrical peaks. Instead, in standard devices the shape of the electrical field along the vertical direction assumes a triangular shape. The pillars begin to deplete along the horizontal direction and then, once they are completely depleted, the electric field increases vertically until the breakdown is reached.

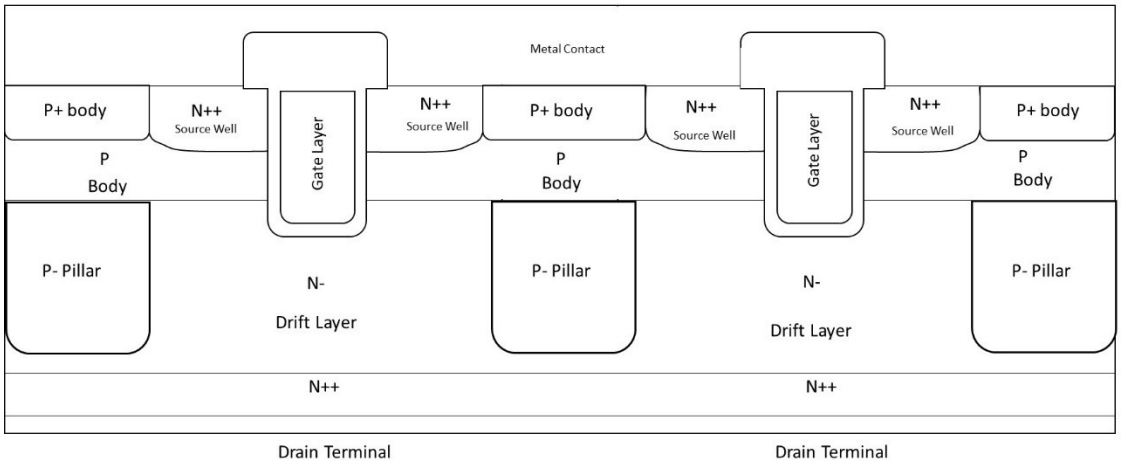



**Figure 2.1.9: Cross section of a n-channel VDMOS SJ-Trench power MOSFET: solution 1.**

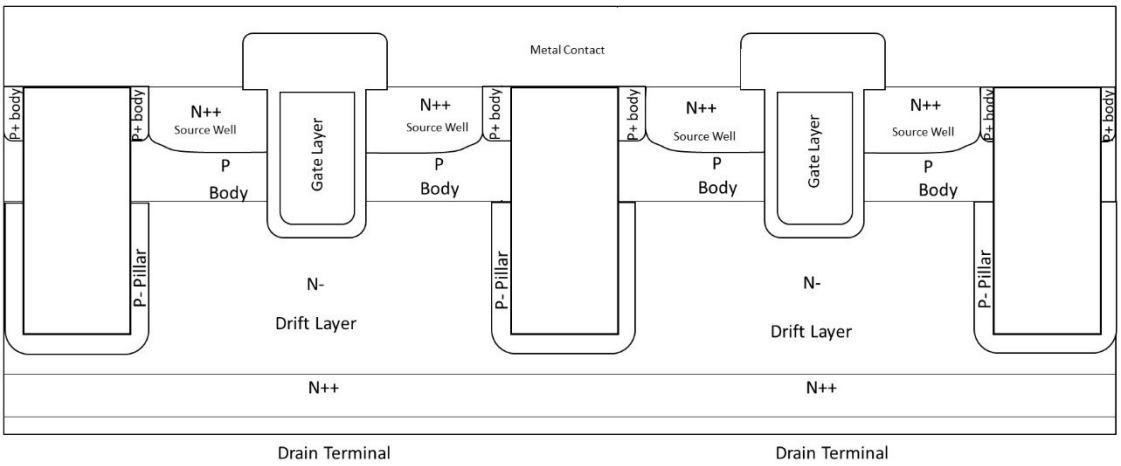



**Figure 2.1.10: Cross section of a n-channel VDMOS SJ-Trench power MOSFET: solution 2.**

Based on how the charge is balanced in the pillars and in the drift layer, $R_{DSON}$ can be reduced at least 5 times compared to the VDMOS structures and the $BV_{DS}$ grows by about 50% for devices that have the same drift depth of the standard devices [108]. However, the ability to efficiently reduce $BV_{DS}$ also depends on the cell pitch. In particular, it has been shown by some simulation with TCAD that when the pitch and the doping concentration in the drift region are increased, the electric field starts to increase vertically rather than horizontally and the $BV_{DS}$ decreases [108]. However, it is important to emphasize that making SJ devices is a rather complex and expansive process. At any rate, despite this issue, SJ design technique is in some cases combined with Trench technology to strongly improve the performances of the devices in high-end power applications (see figure 2.1.9). The first SJ-Trench power MOSFET as shown in figure 2.1.9 was made by Hattori in 2001 [116]. In this figure it is noted how the doped pillars P- are implanted several times and subsequently diffused between two adjacent structures of Trench gate under the body regions P [110], [111]. Another example of solution of the SJ-Trench power MOSFETs is shown in figure 2.1.10 where a deep Trench with P- type implants create pillars between two adjacent Trench gate structure. The columns of the Trench can be filled with suitable deposited epitaxial layers [112], with oxide, or with sealed air gap [113]. A further new and interesting solution is also shown in figure 2.1.11 where the drift region is created under the bottom of the gate trench by means of high energy implants, typically using phosphorus, while the pillars P- are created by the layer epitaxial [114], [115].

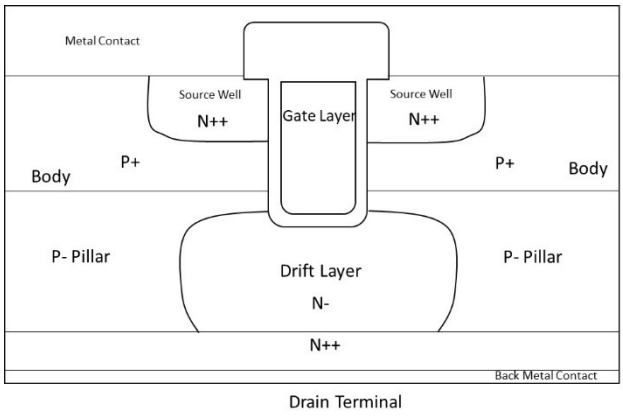



**Figure 2.1.11: Cross section of a VDMOS n-channel SJ-Trench power MOSFET: solution 3.**

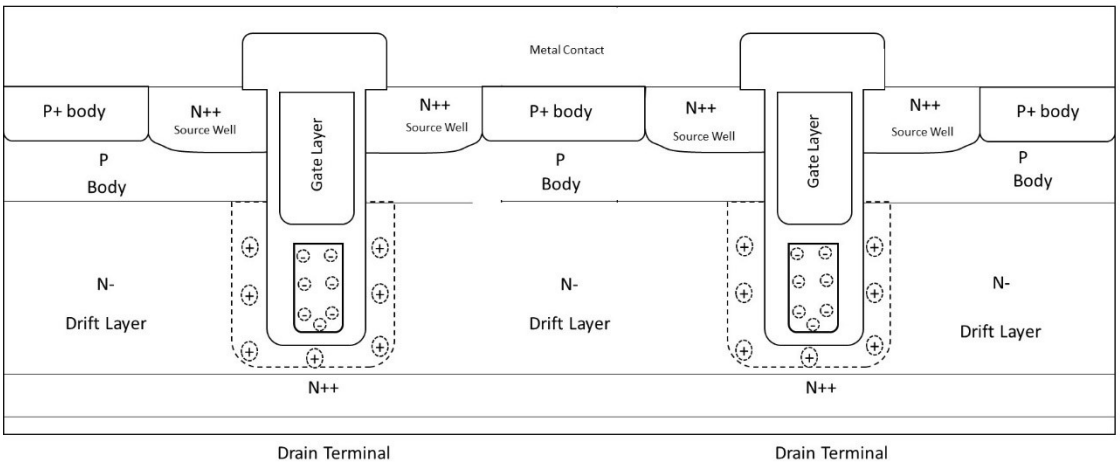



**Figure 2.1.12: Cross section of a VDMOS n-channel SJ-Trench power MOSFET: solution 4.**

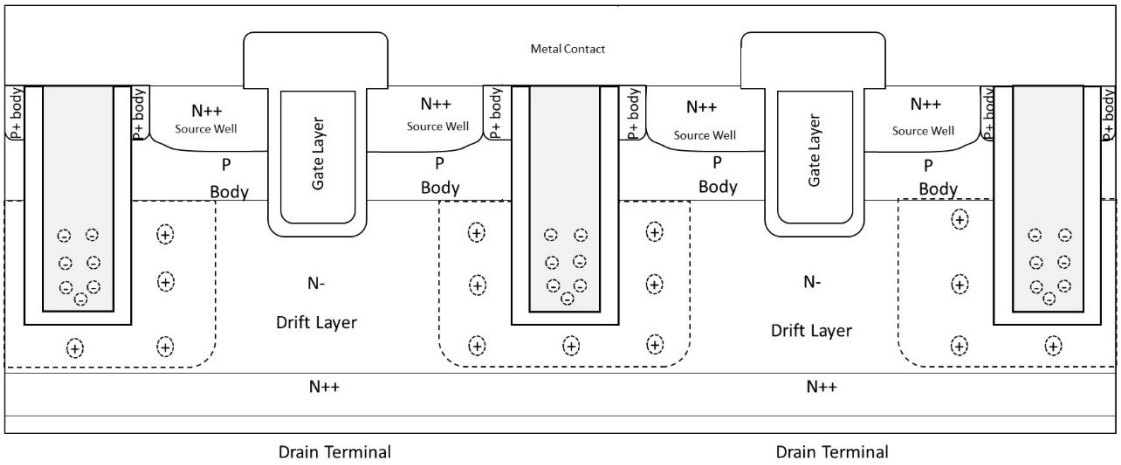
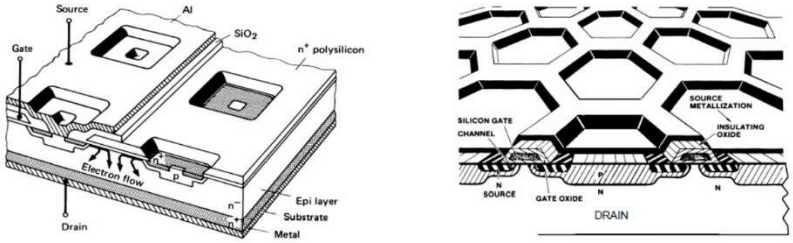



**Figure 2.1.13: Cross section of a VDMOS n-channel SJ-Trench power MOSFET: solution 5.**

Finally, two other new technological solutions of the SJ-Trench power MOSFETs are shown in figures 2.1.12 and 2.1.13. In these two last methodologies the charge balancing process can be carried out using MOS capacitors instead of P- pillars since they induce a depletion region due to a negative polarization in the polysilicon layers [118], [119], [120].




**a)** **b)**

**Figure 2.1.14: Two different design topologies to create power MOSFETs (figures taken from page 75 of ref. [123]): a) square cells; b) hexagonal cells.**

This technique can be implemented through field plates buried in trenches where the gate is split into two regions (see figure 2.1.12) or by field plates obtained from trenches alternating with the gate structures (see figure 2.1.13).The latter two techniques are called RSO. This type of technology was initially introduced in very low voltage devices but later it was even extended to power MOSFETs with higher breakdown voltages [121]. All the technological solutions just described allow to reduce the $R_{DSON}$ down to 30-35% compared to the Trench devices [117]. As already explained, the current flowing in power MOSFETs passes through many cells. The density of the cells is inversely proportional to the breakdown voltage of the device and depends on the technology and the scaling process. This density is in the range of 200,000-1,000,000 cells per $cm^2$ [123]. Figures 2.1.14a and 2.1.14b show two different methodologies used to integrate the cells in the structure of a power MOSFET. In the first solution, figure 2.1.14a, the power MOSFET is made by integrating square cells with standard planar VDMOS structure. Instead, in the second solution, figure 2.1.14b, the power transistor is composed of the integration of hexagonal cells. All cells are connected in parallel. These were the first solutions adopted to make power MOSFETs. Subsequently, power MOSFETs were also made with strip-shaped cells. In addition to the active region of the cell, it is also necessary to design the edge of the device in order to prevent the thickening of the electric field lines in this region by reducing the breakdown voltage of the transistor. Typically, in trench VDMOS devices along the perimeter of the die a thick oxide is grown on which metal layers are deposited which allow to lower the electric field. In very high voltage devices, design solutions have also proposed with floating field rings and new terminations that use the trench to reduce the size of the edge [124]. Typically, the doping concentrations of n++ source wells and the epitaxial drain region are in the order of $10^{19}cm^{-3}$. In the body region, the p doping concentration reaches up to $10^{16}cm^{-3}$. Instead, in the n- drift layer, the doping concentration is in the order of $10^{15}$-$10^{16}cm^{-3}$ [122]. The silicon carbide substrates are nitrogen doped if n-type and aluminium or boron if p-type by ion implantation or with epitaxial growth. Instead, typically, silicon substrates are doped with arsenic or phosphorous to create n-type semiconductors and boron for p-type semiconductors.

## 2.1.1 Optimization of FOM and switching of power MOSFETs

Figure Of Merit, FOM, is given by the product between the gate charge, $Q_G$, and $R_{DSON}$ and it is often used to evaluate the performances of power MOSFETs given their breakdown voltages. In particular, the FOM must be minimized to improve the transistor performances because the lower is the FOM the lower the conduction and switching losses. As $R_{DSON}$ has already been studied thoroughly in the previous paragraph, attention will now be placed on $Q_G$. The dynamic characteristics of power MOSFETs depend on the intrinsic capacitances of the devices. Figure 2.1.1.1 shows the intrinsic components for a packaged n-channel power MOSFET. In this figure it is possible to observe that within the power MOSFETs there are three equivalent variable capacitances: $C_{GS}$, $C_{GD}$ and $C_{DS}$. These capacitances are largely determined by the size of the chip and the cell topology used and also strongly depends on the external potentials applied, $V_{GS}$ and $V_{DS}$. With reference to the VDMOS topology, $C_{GS}$ is essentially given by the $C_{OX}$. $C_{GD}$ depends on either the capacitance in the channel interface region and the drift region between two adjacent cells or on the capacitance due to the lower part of the interface with the oxide of the gate structure of a Trench power MOSFET as shown in figure 2.1.3. Therefore, to greatly reduce the $C_{GD}$, for example, the cell pitch and width of the Trench could be reduced, or even the thickness of the oxide in the affected area could increase as in the case of TBOX solution for Trench devices. In planar VDMOS structure, the thickness of the oxide between two adjacent cells has grown considerably compared to the oxide along the channel. In this intercellular region, the so-called field oxide is grown which has a thickness similar to that of the edge of the die and is in the order of 1,000nm against 50-100nm in the channel region. In the case of Trench devices, even if TBOX solution is widely used to decrease $C_{GD}$, other solutions have been introduced that allow to reduce the $C_{GD}$ along the sides of the Trench as shown in figure 2.1.1.2. In this solution the upper part of the oxide of the Trench gate has a thinner thickness but it increases going towards the bottom so that the shape resembles a terraced or stepped structure with an extended field plate [125], [126], [127]. This extended field plate allows to shield the electric field in the region where the gate oxide is thinner but, on the other hand, slightly increases the $C_{GD}$ by reducing the effect of the TBOX. In 2003 Baliga proposed a new design solution defined as split-gate or shielded-gate Trench VDMOS as shown in figure 2.1.1.3 [128], [129].

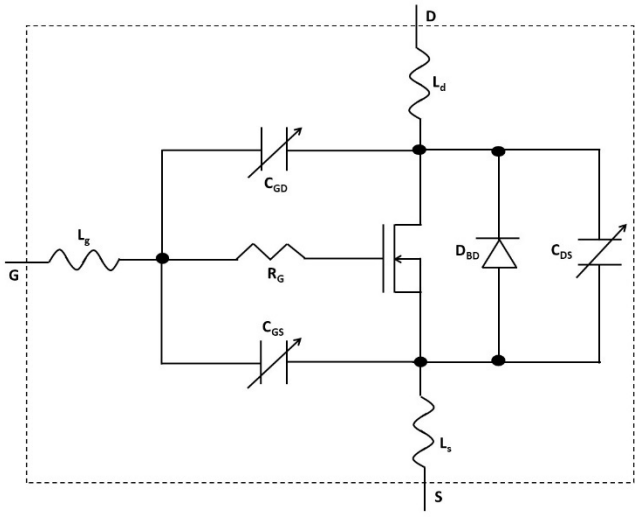



**Figure 2.1.1.1: Equivalent circuit of a n-channel power MOSFET with intrinsic components included.**

In the latter figure, the gate structure is divided in two parts filled with in situ doped polysilicon: the upper polysilicon is connected to the gate electrode while the lower one is a grounded polysilicon field plate. However, it is important to highlight that the grounded buried polysilicon introduces a capacitance placed in parallel with the gate electrode which slightly increases the $C_{GS}$. Furthermore, the buried polysilicon introduces as additional capacitance placed in parallel with the $C_{DS}$ which increases its value overall. These latter one is mainly due to the depletion region of the junction between the body and the drift regions. Figure 2.1.1.1 highlights three small inductances, generally of few nanohenrys, $L_g$, $L_s$ and $L_d$, which are those introduced by the wires that connect the gate, source and drain terminals to the package.

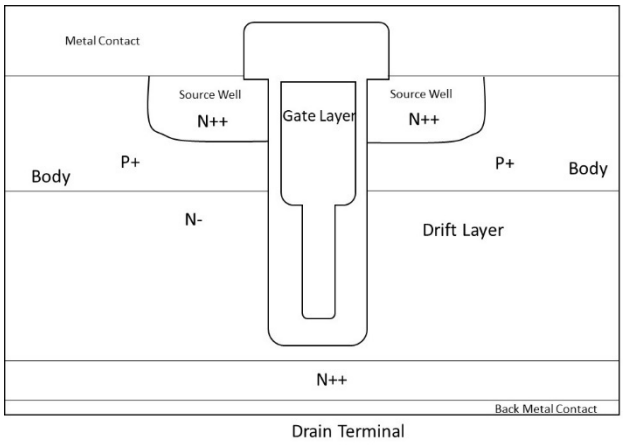



**Figure 2.1.1.2: Cross section of a n-channel Trench power MOSFET with the polysilicon gate with terraced oxide.**

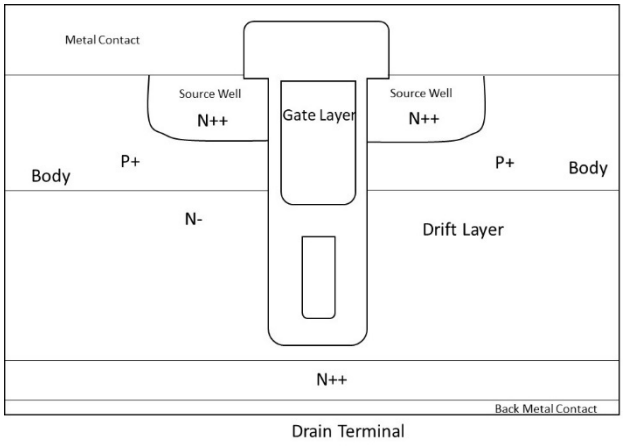



**Figure 2.1.1.3: Cross section of a n-channel Trench power MOSFET with split gate VDMOS structure.**

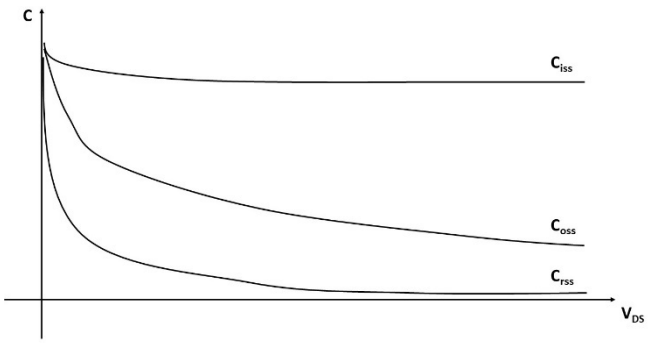



**Figure 2.1.1.4: Typical variation of the intrinsic capacitances of the power MOSFET with the $V_{DS}$.**

Furthermore, the intrinsic diode due to the junction between the body and the drift region was also highlighted. The resistor shown in figure 2.1.1.1, $R_G$, is the intrinsic resistance observed dynamically by the gate terminal due to the resistivity of the polysilicon layer on which the displacement current flows during the switch on and switch off processes. It is important to underline that the manufactures of the power MOSFETs do not indicate the $C_{GS}$, $C_{GD}$ and $C_{DS}$ in their datasheets but the input capacitance, $C_{iss}$, the output capacitance, $C_{oss}$ and the reverse capacitance, $C_{rss}$ [123]. The $C_{iss}$ is measured when the drain and source terminals are short-circuited and is given by:

$$C_{iss} = C_{GS} + C_{GD} \tag{2.1.1.2}$$

$C_{oss}$ is measured when the gate and source terminals are short-circuited and is given by:

$$C_{oss} = C_{DS} + C_{GD} \tag{2.1.1.3}$$

Instead, the $C_{RSS}$ is roughly equal to the $C_{GD}$. Typically, these capacitances are measured with signal that have a frequency of 1MHz and their variations with respect to $V_{DS}$ are shown in figure 2.1.1.4. $C_{RSS}$ is the component that connect the output voltage, $V_{DS}$, to the input terminal and, in the analysis of small signal, it is even defined as Miller capacitance. It can be classified as a feedback capacitance which is larger than real value as it can be observed in vacuum tubes amplifiers (Miller effect) [131].

## 2.1.2 Breakdown voltage of power MOSFETs and design rules

When a power MOSFET is turned off, no current flows in the device even if a voltage is applied between the terminals of the drain and source because the $V_{GS}$ is lower than the $V_{th}$. In any case, the power MOSFETs are designed to sustain a predetermined maximum $V_{DS}$ when they are turned off. Exceeding this voltage, the power transistors can no longer sustain this potential and a current begins to flow into the device. This $V_{DS}$ value is called the breakdown voltage, $BV_{DS}$, of a power MOSFET. As already mentioned, power MOSFETs have an intrinsic diode connected between drain and source terminals and this is composed of the body and drift junction. Therefore, when a power MOSFET reaches to its breakdown voltage it means that $BV_{DS}$ of this diode has been reached. The breakdown mechanisms are mainly three: thermal instability, tunneling and avalanche multiplication [3]. In general, even if the breakdown of the power MOSFET is due to the phenomenon of avalanche multiplication, in this section, all mechanisms will be briefly discussed for a complete analysis of the phenomenon. When the body-drift junction is reversed polarized, a small current flows due to minority carries. This current strongly depends on the junction temperature and, in particular, it is correlated to the concentration of the intrinsic carriers: the higher the temperature the higher the concentration of intrinsic carriers. The product between the potential of the reverse junction applied and the current produces power losses which increase the junction temperature. As the temperature rises, more intrinsic carriers are thermally generated in the junction, the current increases and, thus, the junction temperature increases even more. Therefore, the device may fail due to this positive feedback between current and temperature responsible for thermal instability even called thermal runaway process. In germanium or silicon, semiconductors with low bandgap energy, this phenomenon is more evident than in silicon carbide devices. In the junctions with high concentrations of impurities on both sides, the tunnel effect due to a large reverse potential applied is the main breakdown mechanism. In fact, carriers can jump a potential barrier due to a large electric field applied if this barrier is sufficiently thin (Zener effect of band-to-band tunneling from that of valence of the body to that the conduction of the drift). When a breakdown phenomenon due to the tunneling effect occurs, the $BV_{DS}$ decreases with increasing temperature. In fact, as the temperature increases, it is possible to obtain the same tunneling current for smaller reverse potentials. As will be explained later, in the avalanche process the breakdown voltage increases with increasing junction temperature, thus, it is easy to distinguish between the two tunneling mechanisms. Avalanche breakdown is caused by a physical mechanism called impact ionization. In fact, when the body-drift junction is reverse polarized, the high electric field applied on the space charge layer may be sufficient to increase the kinetic energy of the free electrons until they can break the reticular bonds when they impact the structure creating additional free electrons (impact ionization mechanism). These additional electrons can in turn gain enough kinetic energy to break other bonds by creating further free electrons. Therefore, in a small time, this cascade mechanism produces a large number of free electrons which, when dragged by the reverse electric field, cause a great loss of power in the junction region until a failure occurs. This mechanism is irreversible and occurs when the electric field applied in the reverse polarized junction reaches a critical value defined as $E_{BD}$. To generate an additional free electron, the incident electron must release energy at least equal to or greater than the energy bandgap during the collision. Therefore, if $\tau_C$ is the average period so that a released electron impacts with the reticule, $E_{BD}$ can be estimated as [122]:

$$E_{BD} = \sqrt{\frac{2mE_g}{q{\tau_C}^2}} \qquad (2.1.2.1)$$

For example, in silicon semiconductors, $\tau_C$ is in the order than $10^{-13}$s and, thus, $E_{BD}$ is equal to about 0.3MVcm$^{-1}$, thus, a value quite similar to that experimentally measured in power MOSFETs (0.2MVcm$^{-1}$). Probably, the measured value which is lower than the estimated theorical one is due to the fact that the incident electrons do not completely lose their kinetic energy in collision with the reticule. Instead, in SiC semiconductors the $E_{BD}$ is equal to about 3MVcm$^{-1}$. As already mentioned, the p-type body region is more doped that than the n-type drift region, thus, applying a reverse potential in the junction, the depleted region spreads almost entirely in drift rather than in the body layer, thus, the $BV_{DS}$ can be obtained as (see figure 2.1.2.1a):

$$BV_{DS} = \frac{E_{BD} x_d}{2} = \frac{\varepsilon_{SiC} {E_{BD}}^2}{2qN_D} \tag{2.1.2.2}$$

Therefore, once the $E_{BD}$ has been set, the $BV_{DS}$ depends heavily on the $N_D$. In particular, Eq. (2.1.2.2) can be rewritten as:

$$x_d = 2\frac{BV_{DS}}{E_{BD}} \tag{2.1.2.3}$$

Therefore, with the same $x_d$, the $BV_{DS}$ in SiC substrates is 10 times greater than the $BV_{DS}$ in silicon ones. In fact, in the SiC power MOSFETs the drift region is about a tenth compared to those in silicon. Now, considering that $R_{DRIFT}$ can be obtained as:

$$R_{drift} = \frac{x_d}{q\mu_n N_D} \tag{2.1.2.4}$$

from Eq. (2.1.2.2) and Eq. (2.1.2.3), it is possible to obtain:

$$R_{drift} = 4\frac{{BV_{DS}}^2}{\varepsilon_{SiC}\mu_n {E_{BD}}^3} \tag{2.1.2.5}$$

As it is possible to see, $R_{drift}$ can be obtained on the square of the $BV_{DS}$ even if this is a theoretical approach because in real power MOSFETs this relationship can be better approximated as in Eq. (2.1.2). Even if $\varepsilon_{SIC}$ is about 80% of the $\varepsilon_{SI}$ and the $\mu_n$ in the SiC is about 60% of the $\mu_n$ in silicon, $R_{drift}$ depends on the inverse of cube power of the $E_{BD}$ which in silicon is one tenth of the SiC, thus, once the $BV_{DS}$ is fixed, the drift resistance in SiC is very low compared to silicon devices. In addition, the doping concentration on the drift layer can also be about one hundred times higher than that in silicon power transistors. As it is possible to see in figure 2.1.2.1a, the maximum value of the electric field, $E_{BD}$, is reached in the border between the body and the drift layers. The electric field decreases linearly along the body and the drift regions up to zero with a triangular shape. Since the drift region has a lower doping concentration than the body, the electric field extends along a large portion of the drift layer while only a very small portion spreads in the body and, thus, the latter part can be neglected. The breakdown potential, $BV_{DS}$, is obtained from the area of the triangle as in Eq. (2.1.2.2). In this case we work in non-punch-through conditions. If the drift region is too light doped, the depleted layer can spread down to the N++ layer before reaching the breakdown condition as shown in figure 2.1.2.1b. In this case, the device is in punch-through condition, the electric field decreases drastically in the N++ region and it takes a trapezoidal shape in the drift region. Therefore, the $BV_{DS}$ becomes equal to the sum of the rectangular and triangular areas of the electric field in the entire drift region. The area of the triangular portion is given by:

$$V_1 = \frac{qN_D {x_d}^2}{2\varepsilon_{SiC}} \tag{2.1.2.6}$$

and the portion of rectangular area is equal to:

$$V_2 = E_2 x_d \tag{2.1.2.7}$$

Considering that:

$$E_{BD} = E_1 + E_2 \tag{2.1.2.8}$$

and:

$$BV_{DS} = V_1 + V_2 \tag{2.1.2.9}$$

we obtain:

$$BV_{DS} = E_{BD}x_d - \frac{qN_D{x_d}^2}{2\varepsilon_{SiC}} \quad (2.1.2.10)$$

Therefore, it is possible to obtain: $$BV_{DS} > E_{BD}x_d \quad (2.1.2.11)$$

and, again:

$$x_d < \frac{BV_{DS}}{E_{BD}} < 2\frac{BV_{DS}}{E_{BD}} \quad (2.1.2.12)$$

However, even if $x_d$ is lower in punch-through devices, the greater resistivity in the drift region due to the lower doping concentrations increases $R_{drift}$, and, thus, increases the conduction losses. In case of SJ devices as shown in figure 2.1.8, the electric field in the drift region is quite flat and can be represented as a rectangular rather than a triangle along the x axis (see figure 2.1.2.2). As seen in figure 2.1.2.2, while the breakdown voltage is reached quickly in the standard devices, in the SJ power transistors the electric field remains lower than the critical $E_{BD}$ value and, thus, the $V_{DS}$ can also be doubled before reaching the critical electric field. In any case, in SJ devices the doping concentrations in the drift and body regions must be readjusted to obtain an adequate balance of charge in the pillars and, thus, the study is more complicated to describe. In these example the $BV_{DS}$ is obtained by considering flat junctions but this case is not realistic in practice. In fact, the region of the body is created through diffusion of impurities which determine a certain degree of curvature of the body-drain junction. The radius of curvature depends on the size of the substrate etch masks, on the time and temperature of the diffusion processes, also considering that impurities spread more quickly laterally rather than vertically.

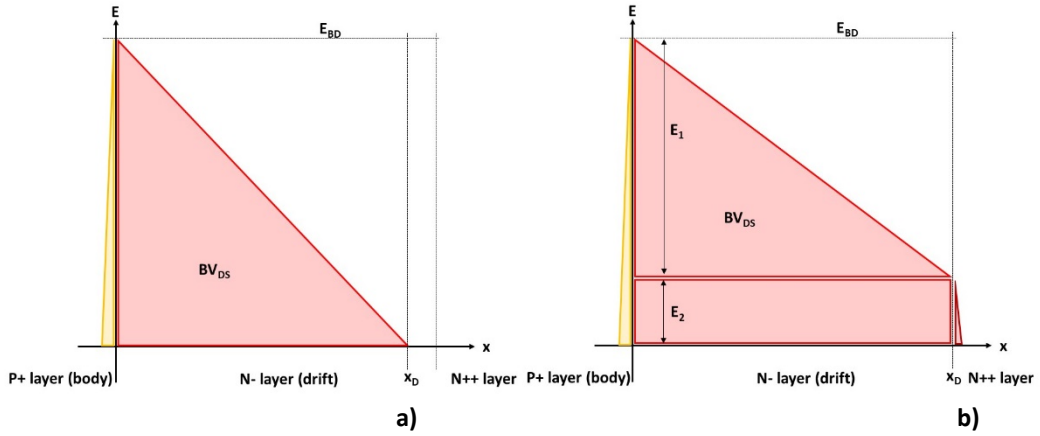



**Figure 2.1.2.1: Spread of the depleted region along the body-drift junction: a) no punch-through; b) punch-through.**

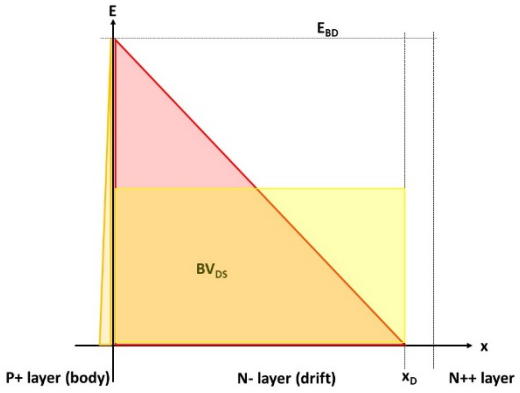



**Figure 2.1.2.2: Spread of the depleted region along the body-drift: comparison between standard VDMOS and SJ.**

This phenomenon is particularly evident when the radius of curvature becomes comparable to the width of the depletion layer of the junction. In fact, the electric field increases in the junction and becomes larger as the radius of curvature decreases and this determines a lowering of the breakdown voltage of the device with respect to a perfectly flat junction. Therefore, the radius of curvature must be controlled and metal plates must be introduced to smooth the electric field along the edge of the junction. However, in the case of power MOSFETs as shown in figure 2.1.4, the gate plates located in the intercell region perform this function, thus, it is not necessary to introduce other structures for this scope.

## 2.1.3 Absolute maximum ratings and SOA of power MOSFETs

SOA stands for Safe Operating Area and is the region of a $I_{DS}$-$V_{DS}$ chart in logarithmic scales where the power MOSFETs operates in safety conditions. SOA is always indicated in the power MOSFET datasheets. Two different SOA graphs can be considered: RBOSA (Reverse Bias Safe Operating Area) and FBSOA (Forward Bias Safe Operating Area). Both graphs are shown in figure 2.1.3.1. The RBSOA is the SOA of the $I_{DS}$-$V_{DS}$ graph identified during the power MOSFETs switching off process (see figure 2.1.3.1a). The safe region during the turn off regime is simply limited by the maximum permissible current value of the power transistor, $I_{DSmax}$, and by the maximum voltage it can sustain, $BV_{DS}$. Instead, FBSOA is the safe operating area identified when the device turns on or during the on state. The theoretical FBSOA under DC operation conditions is limited by four lines: the maximum sustainable voltage, $BV_{DS}$, region A, the maximum power that can dissipate, region B, the maximum allowed current, $I_{DSmax}$, region C, and the maximum current flowing in the device limited by $R_{DSON}$, region D. In particular, in region B, it is possible to obtain:

$$\Delta T_{max} = T_{Jmax} - T_C = R_{thJC}(V_{DS}I_{DS}) \tag{2.1.3.1}$$

$T_{Jmax}$ is the maximum allowed junction temperature, $T_C$ is the temperature of the case and $R_{thJC}$ is the thermal resistance of the junction-case and is a measure of the difficulty in removing the heat from the junction to the case region. In fact, the die is housed in a suitable package and the operating temperature of the latter is different from the internal temperature. The FBSOA of the power MOSFETs is assessed by setting the ambient temperature, generally 25°C, and fixing the $V_{DS}$. The maximum allowed current can be obtained as:

$$I_{DS} = \frac{\Delta T_{max}}{V_{DS}\, R_{thJC}} \tag{2.1.3.2}$$

If the device works in switching mode instead of DC, it is necessary to introduce the junction-case thermal impedance and Eq. (2.1.3.2) can be rewritten as ($Z_{thJC}$ is the thermal impedance):

$$I_{DS} = \frac{\Delta T_{max}}{V_{DS}\, Z_{thJC}} \tag{2.1.3.3}$$

$Z_{thJC}$ is lower than the $R_{thJC}$ and its value decreases as the stress time decreases. Under these operating conditions, the shorter the time the device remains on, the greater the maximum power that can be dissipated (see operating regions E and F in figure 2.1.3.1b). In case the time in which the device is switched on is very small, the FBSOA becomes equal to RBSOA. In region D, the device works completely in the on state, thus, once the $V_{DS}$ is fixed, the maximum current that can pass through the device is equal to:

$$I_{DS} = \frac{V_{DS}}{R_{DSON}} \tag{2.1.3.4}$$

It is important to underline that the maximum allowable limits of the current, applied voltage and power dissipation are defined as the maximum ratings and that none of these values can be exceeded if the device is to work for a long time and in reliable conditions. These maximum ratings strongly depends on the materials used, structures, the design rules, the assembly techniques and processes and, in some cases, the application conditions as well as the operating temperatures. For example, the rated current can be established as the value at which the junction temperature does not exceed the maximum allowed value or at that value for which the wires that connect the die to the package do not evaporate. The maximum allowable junction temperature depends on the quality of the materials used, also considering that the higher the junction temperature, the higher the deterioration rate and, thus, the shorter the life of the device.

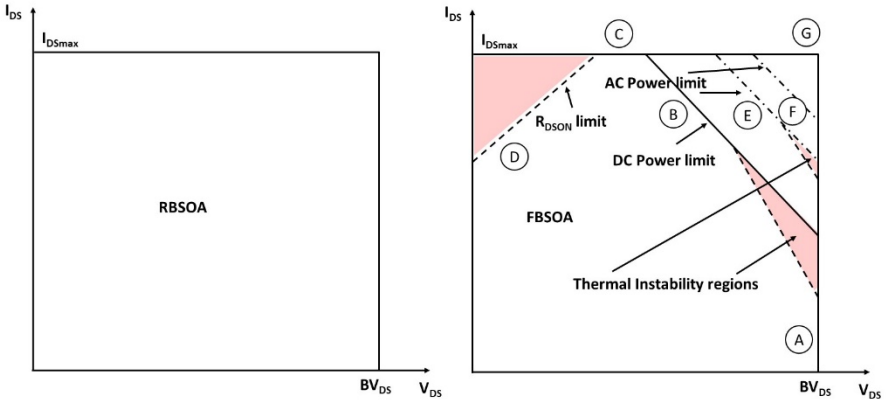



**Figure 2.1.3.1: SOA of power MOSFETs: a) RBSOA; b) FBSOA.**

It is also important to highlight that the area of the real FBSOA is lower than theoretical one because when the device works in saturation mode it can be subjected to the phenomenon of thermal runaway due to an electrothermal instability mechanism between current and temperature [131] (see figure 2.1.3.1b). In fact, when the operating temperature increases, even if the mobility of the carriers decrease, the $V_{th}$ decreases and the $I_{DS}$ could increase until a failure occurs. The normalized increase of the $I_{DS}$ as function of T can be obtained by:

$$\frac{1}{I_{DSsat}}\frac{\partial I_{DSsat}}{\partial T} = \frac{2}{V_{GS}-V_{th}}\left|\frac{\partial V_{th}}{\partial T}\right| - \frac{1}{\mu_n}\left|\frac{\partial \mu_n}{\partial T}\right| \tag{2.1.3.5}$$

When the applied $V_{GS}$ is slightly larger than the $V_{th}$, a small current flows in the device, the first term of Eq. (2.1.3.5), containing the derivative of $V_{th}$, prevails over the second term, containing the derivative of the mobility of the carriers in the channel of power MOSFET, the thermal coefficient becomes positive and the phenomenon of thermal runway is triggered. Instead, for high values of $V_{GS}$, thus, for high values of $I_{DS}$, the second term of Eq. (2.1.3.5) prevails over the first term, the thermal coefficient becomes negative and the device works in safe conditions. Deriving the Eq. (2.1.3.1), it is possible to obtain:

$$V_{DS}\frac{\partial I_{DS}}{\partial T} = \frac{1}{R_{thJC}} \tag{2.1.3.6}$$

If the left term of Eq. (2.1.3.6) becomes greater than that on the right, the heat cannot be extracted quickly from the junction, the temperature starts to increase and the phenomenon of thermal instability cannot be avoided.

## 2.1.4 BTI effect

BTI stand for Bias Temperature Instability phenomenon in MOSFETs. This instability is believed to be caused by the creation of interface traps and fixed charges in the oxide of MOSFETs [4]. In particular, this phenomenon was initially observed in p-channel transistors when a negative voltage was applied on the gate terminal under high temperatures [52]. When the BTI appears by applying a negative potential in the gate terminal the phenomenon is called NTBI. Instead, if positive potential is applied, it is called PTBI. In general, BTI problems leads a decrease in $I_{DS}$ and $g_{fs}$ and, in particular, an increase in $V_{th}$ in absolute value. In this type of stress test, the $V_{GS}$ must not be high enough to exceed the $6MVcm^{-1}$ value of the electric field in the oxide. The MOSFETs affected by the BTI effect quickly recover a $\Delta V_{th}$ fraction after the gate potential has been removed and can completely recover what is lost during the stress phase by applying a potential to the gate of opposite sign and increasing T. The degradation mechanisms of $V_{th}$ and $g_{fs}$ have been studied by Kimizuka et al. [53] during BTI test as a function of stress time. It has been empirically shown that both parameters decrease linearly by increasing the stress time in a logarithm scales chart. $g_{fs}$ is believed to decrease because carriers mobility also decreases during the stress test.

In any case, in this paragraph the BTI phenomenon will not be described in detail because this will be discussed in chapter 4.3 when the experimental results will be explained according to the method proposed by Pobegen based on the reaction diffusion model applied on the tested Power MOSFETs in SiC.

## 2.1.5 Scaling down process of MOSFETs

Scaling down process occurs when the manufactures of MOSFETs migrates from one technology to another decreasing the critical dimensions of the devices. For example, one of the most important parameter involved in the scaling down process is the length of the channel. The scaling down process is a very important factor in the industrial environment because it allows to reduce the volume of the devices and, thus, to have less switching and conduction losses producing more dices for a single wafer. It is important to underline that the scaling down process applied to MOSFET transistors is not typical only of signal devices but also of power MOSFETs, in particular, those of low voltage. By introducing a dimensionless scaling factor which is characteristic of the reduction of dimensions passing from generation to generation, any transistor size of the new technology can be derived from the old technology as shown in figure 2.1.5.1. This scaling down technique is called as voltage constant scaling down process when working conditions of the application remains the same by changing the technology used [48]. However, when the applied voltages remains constant, it is necessary to reorganize the doping concentrations in the new technology MOSFETs in order to optimize the electric fields and charges inside the devices [215], [3], [9]. This scaling down technique is the main usually adopted to design power MOSFETs. Another scaling technique adopted to realize, in particular, signal MOSFETs is the constant electric field process. In the latter case, the electric field inside the device remains constant by increasing the doping concentrations by same scale factor and decreasing the applied external potentials. However, the latter technique is less used because the $V_{th}$ of the devices decreases and the external voltages applied cannot be changed. Obviously, smaller critical dimensions of the device entail the onset of parasitic effects which could be considered negligible in larger transistors such as, for example, short channel effects, problems of the hot carriers in the drain edge, problems of depletion of polysilicon, problems of DIBL and GIDL and, finally, quantization effects in the inversion layer.

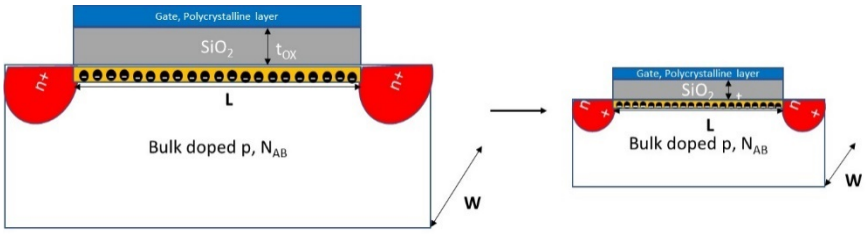
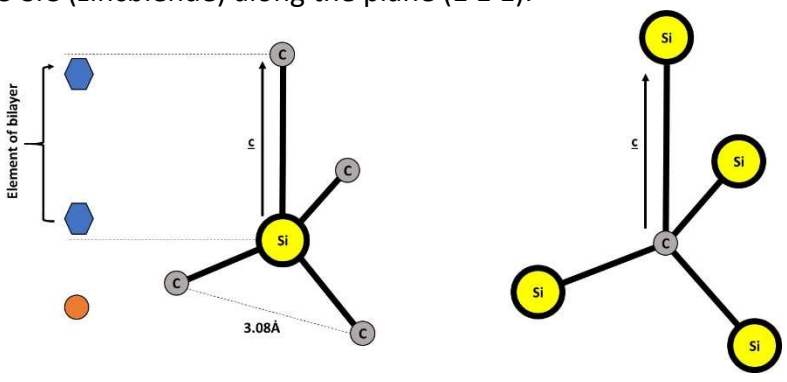



**Figure 2.1.5.1: Scaling down process in a MOSFET.**

## 2.2 Properties of the Silicon Carbide material

SiC was first synthetized about 200 years ago [134] and in 1891 Acheson discovered a process for making it by defining this material as carborundum [135]. It has particular abrasive and hardness properties. Subsequently, it was discovered that SiC have several crystal symmetries and this property has been called polytypism [136]. The different polytypes were classified according to the stacking and orientation of the unit cell layers by Ramsdell in 1947 [137]. In nature this compound exists in more than 250 different polytypes [141] but only a few are commonly used and reproducible as semiconductors in electronics [138]. The elementary structure of the SiC crystal is tetrahedral with carbon and silicon atoms covalently bonded with a threefold symmetry around the axis parallel to the direction of stacking as shown in figure 2.2.1. In the crystal structure of SiC the closest to a silicon atom is a carbon atom and the closest to a carbon atom is a silicon atom and both are surrounded by orbitals in the $sp^3$ hybridization. All closed-packed SiC polytypes are made in the same way and are composed of bilayers having three possible spatial configurations indicated as A, B and C. For example, in figure 2.2.1a, the elements of the bilayer are the central atom of silicon and the atom of carbon (hexagonal symbol) along the c direction. The others carbon atoms does not belong to the bilayer (circle symbol). Looking along direction c, the crystal configuration is shown in figure 2.2.2. Therefore, each polytype can be made repeating the unit cell in two or even more stacking layers with the constraint that the layers having the same orientation cannot be stacked on each directly. There are two types of tetrahedral in the SiC unit cell. The first type is obtained by rotating the next tetrahedron along the c-axis by 180°. The second type of tetrahedron is obtained by stacking another obtained from the mirror image of the first along the c-axis. An example of arrangement of the stacking layers is shown in figure 2.2.3 in which the ABCB sequence of the 4H-SiC polytype is represented. The polytypes of hexagonal unit cell have different stacking sequences such as ABAB, ABCB and ABCACB, referring to 2H-SiC (wurtzite), 4H-SiC and 6H-SiC, while, the ABC sequence produces the cubic polytype as 3C-SiC (zincblende) along the plane (1 1 1).




**a)** **b)**

**Figure 2.2.1: SiC Tetrahedral structure: a) with four carbon atoms around one silicon atom; b) with four silicon atoms around one carbon atom.**

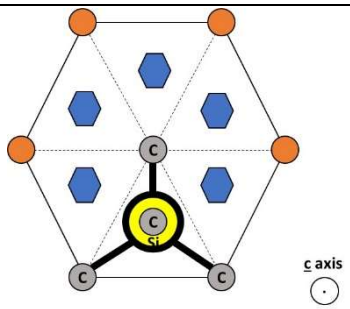



**Figure 2.2.2: Front view of the SiC cell along the c axis with layers in sequence ABC.**

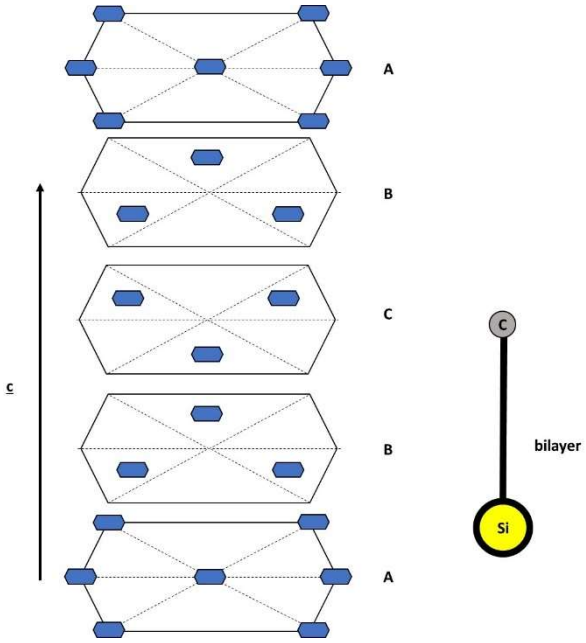



**Figure 2.2.3: Stacking sequence of bilayers of a 4H-SiC crystal structure.**

When two hexagonal lattices are alternated, each layer is attached to the underlying layer through the silicon atoms and to the top layer through the carbon atoms and, thus, the surfaces of the wafer will end with a layer of silicon atoms on one side and atoms of carbon on the other side. The face of the wafer made up of silicon atoms indicates the plane (0001) while the face made up of carbon atoms indicates the plane $(000\bar{1})$. The cubic SiC lattices, as in the case of 3C-SiC, are also called β-SiC structures while the hexagonal and rhombohedral reticules are called α-SiC polytypes. However, it is import to emphasize that carborundum materials as 4H-SiC have two different lattice arrangements. The first arrangement is cubic and refers to the site indicated with k while the second is hexagonal and refers to the sites indicated with h. Cubic sites are located in layers B because the structures immediately below and above resemble 3C-SiC. Instead, the hexagonal sites are located in layers A and C because the surrounding structures resemble the 2H-SiC polytype. In fact, the 3C-SiC and 2H-SiC polytypes are perfectly cubic and hexagonal structures respectively. The three most common hexagonal polytypes are 2H-SiC, 4H-SiC and 6H-SiC and the stacking sequences of their layers are AB, ABCB, and ABCACB (see figure 2.2.4). Abbreviation such as 4H-SiC and 6H-SiC are written according to Ramsdell's notation. Ramsdell's notation is the most widely used notation in crystallography. In Ramsdell's notation the number refers to the periodicity in the stacking direction and the letter refers to the crystalline structure H for the hexagonal and C for the cubic one.

There are other common notational systems used to describe SiC polytypes such as Jagodzinski [139], also known as Wyckoff notation [140], Pauling's notation and the ABC one that considers the different sequences of the layers. Jagodzinski's notation described the type of packaging layout of double layers (k for cubic and h for hexagonal). For example, the 4H-SiC polytype can be represented as khkh. Furthermore, different polytypes can also be classified according to their hexagonality property by defining the percentage of hexagonal double layers with respect to the total in the unit cell. For example, 4H-SiC has a hexagonality is equal to 50% because there are two cubic bilayers and two hexagonal bilayers in the unit cell. It is important to emphasize that all polytypes are indirect bandgap semiconductors. It is also important to underline that 4H-SiC is the polytype most used in electronics for high power and high frequency applications and to work at high temperatures for its peculiar properties. In fact, 4H-SiC has a higher critical field and greater carrier mobility than the 6H-SiC and 3C-SiC polytypes. Furthermore, in 4H-SiC the wafer growth technique is more mature and 4" and 6" diameter wafers are widely available on the market. In addition, the electron drift saturation velocity in 4H-SiC is more than double the silicon, thus, these devices can operate at high switching frequencies. A comparison of the main properties between 4H-SiC and other polytypes and semiconductors is shown in tab. 2.2.1 at room temperature. Even though diamond and GaN have comparable properties or in some cases better than 4H-SiC, the ease with the oxide can grow in 4H-SiC allows to obtain enormous benefits comparable to those that are obtained using the silicon. The advantage of 4H-SiC over silicon can be measured by the figure of merit introduced by Baliga. Baliga with this parameter connects the conduction losses in MOSFETs with the characteristics of materials as [146]:

$$\mathrm{BFOM} = \varepsilon_r \mu_n E_c{}^3 \tag{2.2.1}$$

The BFOM for 4H-SiC and silicon are 34.7 and 1 respectively, confirming that 4H-SiC shows significantly better performances.

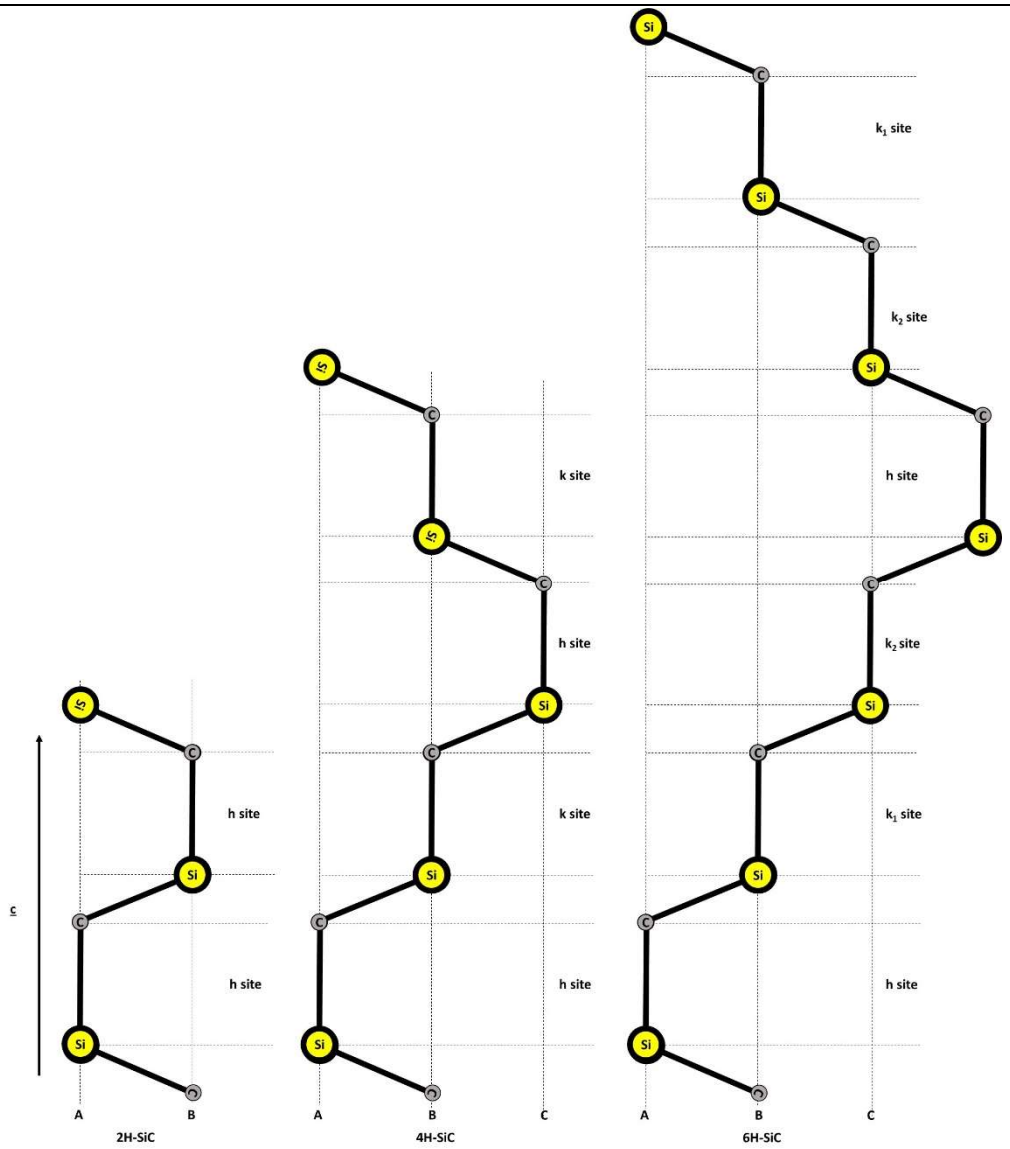



**Figure 2.2.4: Stacking sequences of some of the main SiC polytypes: a) 2H-SiC; b) 4H-SiC; c) 6H-SiC.**

**Tab. 2.2.1: Material properties of 4H-SiC compared to other semiconductors [142], [143], [144], [145].**

| | $E_g$ [eV] | $E_c$ [MVcm$^{-1}$] | $n_i$ [cm$^{-3}$] | $v_s$ x 10$^7$ [cms$^{-1}$] | $\mu_n$ [cm$^2$V$^{-1}$s$^{-1}$] | $\mu_p$[cm$^2$V$^{-1}$s$^{-1}$] | $\varepsilon_r$ | C [Wcm$^{-1}$K$^{-1}$] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Si | 1.12 | 0.3 | 1.5 x 10$^{10}$ | 1 | 1350 | 450 | 11.8 | 1.5 |
| 3C-SiC | 2.3 | > 1.5 | ~ 10 | 2.5 | 750 | 40 | 9.6 | 4.9 |
| 4H-SiC | 3.26 | 3.2 | ~ 10$^{-7}$ | 2.2 | 700-1200 | 120 | 9.7 | 4.9 |
| 6H-SiC | 3.02 | 3.2 | ~ 10$^{-5}$ | 2.5 | 60-400 | 90 | 9.7 | 4.9 |
| GaN | 3.39 | 3.3 | ~ 10$^{-11}$ | 2.5 | 900-1250 | 30 | 9.0 | 1.3 |
| GaAs | 1.42 | 0.6 | 1.8 10$^6$ | 2.0 | 8500 | 320 | 12.8 | 0.46 |
| Diamond | 5.45 | 5.6 | ~ 10$^{-27}$ | 2.7 | 2200 | 1600 | 5.5 | 22 |

## 2.2.1 Doping mechanisms of Silicon Carbide

As in the case of silicon, SiC can also be doped. Doping is carried out by spreading or implanting in the crystal impurity atoms that generate energy states near $E_c$ and $E_v$. In n-type substrate the states placed near the conduction band cause an increase in the concentration of electrons in the same band. In p-type substrate, states are close to the valence band and the concentration of holes is increased in the same band. Ionization energy is defined as the difference in energy between the state of the dopant and that relative to the edge of the band considered. Once fixed T, the doping concentration of donors and acceptors can be obtained through ionization energy [142]. In SiC, dopants have low diffusivity even by carrying out rather high heat treatments [150], thus, it is necessary to carry out an ion implantation even if this process introduces defects in the reticule. After the implantation process, to activate the dopant, eliminate reticular damage and relax the crystal, it is necessary to carry out annealing at high temperatures even up to 1700°C [151]. The doping concentrations that are carried out are in the range from $10^{16}$ $cm^{-3}$ to about $10^{20}$ $cm^{-3}$. An important aspect of SiC is that dopants can be spread in situ during substrates grown. The element of the group V such as N, P, As are used to make n-type substrates even if, usually, nitrogen is the most utilized. The nitrogen atoms replace the carbon atoms in the reticule at the hexagonal and in cubic sites. In p-type substrates, doping is carried out through group III elements such as B, Al and Ga although it is often preferred to use aluminium for its lower ionization energy. These dopants form acceptor states just above the valence band.

## 2.2.2 Epitaxial growth of Silicon Carbide crystals

In the case of silicon, every single crystal is grown from molten silicon from a crystal seed and this process is called Czochralski [148]. However, this standard technique cannot be used to make high quality SiC crystals. In the case of silicon, the growth rate of the crystal is in the order of few mm/min instead in SiC it is quite low in the order of few mm/hr. To produce SiC crystals, a seeded sublimation growth process is used [152]. This technique was introduced by Tairov and Tsvetkov in 1978. The process consists in the Physical Vapor Transport (PVT) of the sublimated SiC powder placed inside a cylindrical graphite crucible where the pressure and temperature are carefully controlled (see figure 2.2.2.1). In particular, the seed of the crystal is located in the upper part of a reaction chamber and the source material is placed in the lower part. The latter material is heated to about 2000°C and above, sublime, and is released in the form of a vapor containing silicon and carbon atoms [148] flowing towards the seed [153]. Typically, the crystal grows in the direction (0 0 0 1) of the lattice called the silicon face. Another method used for the growth of the SiC crystal is the high temperature CVD process [154]. Typically, in the CVD process SiC is grew using a hot wall reactor as shown in figure 2.2.2.2. In particular, the SiC wafer is located on a graphite support of the hot wall reactor in which the reaction gases containing silicon and carbon atoms flow.

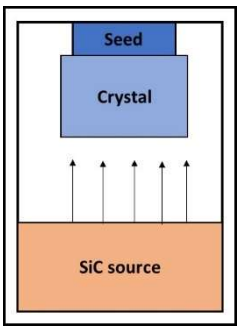



**Figure 2.2.2.1: Crystal growth process by PVT.**

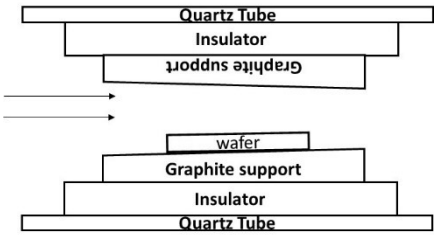



**Figure 2.2.2.2: Hot wall reactor for the growth of SiC in a CVD process.**

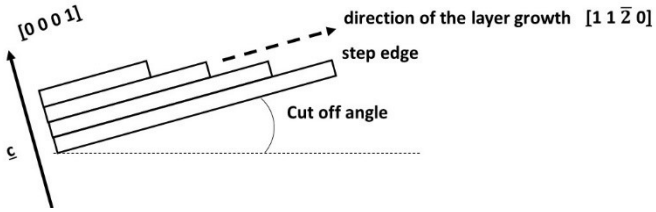



**Figure 2.2.2.3: Crystal growth technique for making 4H-SiC wafers.**

Typically, these gases are silane ($SiH_4$) and propane ($C_3H_8$) transported in a stream of dihydrogen gas ($H_2$) which react on the surface of the wafer and allow the SiC crystal to grow [156]. One of the most important parameter to monitor during the SiC crystal growth process is polytype control since it is important to maintain the order of the bilayer stacking layer. Polytype control can be performed by a step-controlled epitaxial process [157], [158]. In fact, from figure 2.2.4b and 2.2.4c it is possible to observe that the 4H-SiC and the 6H-SiC have the same sequence of stacking bilayer up to the third level and after their differ due to the angle that the fourth bilayer has with the third bilayer. Therefore, there are two possibilities that can occur. In the first, the stacking sequence is the same as for 4H-SiC. In the second one, the stacking sequence becomes equal to the 6H-SiC polytype. The step-controlled epitaxial process for 4H-SiC growth is shown in figure 2.2.2.3 by setting a suitable tilt angle. This technique allows to maintain more the correct stacking sequence of the bilayers even if it forms steps along the edges. It is important to underline that the cutting angle plays an important role in the growth of the process: it is usually set at 4° [159]. Recently, to obtain faster growth, the substrates have growth with a tilt angle equal to 8° [149], [155]. In the latter case, the crystal growth rate reaches up to 25-30 $\mu mh^{-1}$.

## 2.2.3 Defects in SiC crystal

Defects in the SiC crystal can be intrinsic and extrinsic. The former are small faults in the crystal reticule as vacancies or interstitial. Instead, the latter are due to atoms of other species that replace the silicon and carbon sites. For example, the dopant atoms can introduce extrinsic defects to provide the desired electrical properties of a semiconductor. Generally, the defects can be incorporated during the growth of the crystalline process or generated in high concentration during the ion implantation processes. The unwanted intrinsic and extrinsic defects introduce deep levels in the bandgap which deteriorate the electronic properties of the substrate. Intrinsic defects are points in the SiC crystal and can be vacancies, interstitials and antisites in the case of compound materials such as in the carborundum. A vacancy occurs when an atom is missing from the crystal. An Interstitial defect occurs when an atom is added between the reticule sites of the crystal by distorting the lattice in the surrounding area or by sharing a site with an atom of the host crystal (split-interstitial defect). Vacancies and interstitials occur together because when an atom of the reticule moves away from its origin site it moves into the interstice. In the latter case, if the created pair remains close enough the defect is called the Frenkel-pair while, it moves on the surface, the defect is called the Schottky-pair. In the case of the SiC crystal, an antisite defect occurs if, for example, a carbon atom takes the place of a silicon atom ($C_{Si}$). Conversely, if a silicon atom takes the place of a carbon atom, the defect is called $Si_C$. The defects in the SiC reticule affect the structural and electronic properties of the crystal based on the position they occupy, their geometries, the length of the bonds with other atoms of the lattice and the symmetries by introducing energy states into the bands and, in particular, in the bandgap. For example, vacancies create dangling orbitals in the reticule that introduce deep energy states into the bandgap. The interface traps act as acceptors or as donors depending on their energy levels within the bandgap. However, some deep defects are able to trap both electrons and holes that act as donors or acceptors and are called amphoteric defects. Furthermore, in the vacancies, the dangling orbitals could re-bond with other orbitals in order to relax the structure by distorting the existing bonds and creating new defects called negative U-defects. In the literature, many defects has been experimentally detected in SiC crystals using the EPR (Electron Paramagnetic Resonance) spectroscopy technique. EPR is also called ESR (Electron Spin Resonance) and is a spectroscopy technique used to study chemical species by analysing unpaired electrons by means of their magnetic properties. The identified defects are carbon vacancies ($V_C$) [159], silicon vacancies ($V_{Si}$) [160], divacancies ($V_CV_{Si}$) [161] and, as already mentioned, the carbon antisites ($C_{Si}$) [162], the antisite pairs ($Si_CC_{Si}$) [163], $C_{Si}$ coupled with a $V_C$ ($C_{Si}V_C$) [164]. In particular, $V_C$ defects have the lowest formation energy and can be found in abundance in the 4H-SiC crystal [165], [166]. These defects have energetic states within the bandgap, they can be found in different states of charge such as positive, $V_C^+$, and negative, $V_C^-$, and manifest paramagnetic behaviours. However, the dominant defect is that $V_C^+$ [167] and the final effect on the properties of the crystal depends on the fact that it is found in the k rather than in the h sites of the reticule. In fact, if the carbon vacancy is at the k site, distortions occur in the orbitals due to the JTE effect, Jahn-Teller-effect, and the symmetry of the defect changes. JTE's theorem states that any nonlinear molecule with a spatially degenerated electronic ground state shifts to a new distorted configuration that allows removing the degenerate energy states in order to have the lowest energy in the system. On the other hand, if the carbon vacancy is placed at the h site, the symmetry of the defect remains unchanged [168]. It is possible to identify whether the $V_C^+$ is located in a cubic or hexagonal site by the EPR resonance spectrum. In this technique, the carbon vacancies in the 4H-SiC crystal are called $Z_{1/2}$ defects and are those that drastically reduce the lifetime of the carriers in the substrate [169].

The silicon vacancies, $V_{Si}$, like those $V_C$, have different paramagnetic energy states within the bandgap of a 4H-SiC. They have a higher formation energy than $V_C$ and in these types of defects the JTE effect does not occurs because the dangling bonds simply point towards the inside of the molecular structure. Unlike carbon vacancies, in most $V_{Si}$ there are only small differences between vacancies placed in sites k and those placed in sites h sites at least if we consider the vacancies that behave as negative charge, $V_{Si}^-$ [170]. The carbon antisite vacancies pair, $C_{Si}V_C$, are defects identified both as states that behave as negative charges [171] and states that behave as positive charges [172]. Divacancy $V_CV_{Si}$ are a highly stable defects which can be formed by the migration of silicon and carbon vacancies and have a high formation energy [173]. Furthermore, they have been identified in the neutral state of charge $V_CV_{Si}^0$. Unlike the vacancies which can only be of two species in the 4H-SiC crystal, the configuration of the interstitial defects can be very numerous. In many cases, the interstitial defects are distinguished only by their geometries such as, for example, interstitial sites in the tetrahedral configuration of silicon atoms, $I_{TSi}$, or carbon atoms, $I_{TC}$. When the interstitial atom is in the center of a reticular hexagon it is in a hexagonal configuration, $I_{Hex}$, and if it is located along the connection between two neighbouring lattice sites it is in a bond-centered configurations, $I_{bc}$. Instead, split-interstitial defects lie at the edges of a cubic and or hexagonal bi-layer of the reticule. In the most cases, split-interstitial silicon defects behave like electric charges in $4^+$, $2^+$ or neutral states in SiC crystals. Instead, the interstitial defects of carbon atoms tend to form short bonds with the direct carbon atoms neighbours even if their arrangement in the reticule is quite similar to the interstitial defects of silicon atoms. Split-interstitial defects of carbon atoms can behave as $2^+$ to $1^-$ charges.

As already mentioned, another important type of defects is the antisites. $Si_C$ defects have been observed to behave as charges ranging from $4^+$ to neutral, 0. Unlike $Si_C$ defects, $C_{Si}$ defects are electrically inactive. Defect points, as described in this chapter, can move randomly through the crystal reticule. Every defect is created if at least the formation energy is supplied. Subsequently, the defects can move if the energy supplied exceeds a certain value such that can migrate passing from one position to another in the crystal. Defects move in different ways interstitially or thorough vacancies. Typically, the spread of defects is activated thermally. In the one-dimensional case, the defects diffusion equation can be written as (Fick's second law):

$$\frac{\partial G}{\partial t} = \overline{D}\frac{\partial^2 G}{\partial x^2} \tag{2.2.3.1}$$

G is the concentration of the specie and $\overline{D}$ is its diffusivity. The diffusivity coefficient can be expressed by the following Arrhenius-relationship as:

$$\overline{D} = \widehat{D}e^{-\frac{E_a}{KT}} \tag{2.2.3.2}$$

$\overline{D}$ is the diffusivity coefficient independent of temperature and $E_a$ is the activation energy. According to Fick's first law, the relationship between the flux of defects, **J**, and the concentration gradient is equal to:

$$\mathbf{J} = \overline{D}\frac{\partial G}{\partial x} \tag{2.2.3.3}$$

Sometime, during the migration process, the defects may react with other defects or a complex defect may dissociate into its individual constituents.

Other defects such such as dislocations and micropipes are also observed in SiC crystal. Dislocations are linear defects that evolve into one dimension. On the contrary, when defects evolve in two dimensions they are called planar defects and can also evolve into stacking faults. Stacking faults are SiC crystal segments in which bilayers deviate from the exact stacking sequence along the c-axis. Micropipes are widely observed in SiC wafers. They are defects of the hollow tubular type which penetrate the SiC crystals and have a radius between a few tens of nanometers and several tens of micrometers and their density can reach one hundred $cm^{-2}$ during the growth of the crystal [174].

The defects of the micropipes can cause a high reduction of the breakdown voltage and, thus, an increase of the leakage current in the device [175]. Conversely, stacking faults can cause a significant reduction in the lifetime of the carriers.

## 2.2.4 Silicon dioxide growth process in SiC power MOSFETs

Silicon carbide semiconductor is the only WBG semiconductor (Wide Band-Gap) in which the native oxide can be grown by means of a thermal oxidation process forming the silicon dioxide which is the most common dielectric used in microelectronics. Silicon dioxide grown in SiC substrates shows the same properties as that shown in silicon in terms of density, dielectric constant, refractive index, dielectric strength [180]. The thermal oxidation process in SiC is quite similar to that carried out in silicon wafers and can be described by the Deal-Grove model [181] by implementing some modification due to the fact that the CO and $CO_2$ molecules produced during the reaction must be removed [182]. In particular, $SiO_2$ has 9eV of bandgap and the offsets with respect to the 4H-SiC crystal of the conduction and valence bands are 2.70eV and 3.07eV respectively [183]. During dry oxidation the following chemical reactions occur [184].

$$SiC + \frac{3}{2}O_2 \leftrightarrow SiO_2 + CO \quad (2.2.4.1)$$

$$SiC + O_2 \leftrightarrow SiO_2 + C \quad (2.2.4.2)$$

$$2SiC + 3O_2 \leftrightarrow 2SiO_2 + 2CO \quad (2.2.4.3)$$

$$SiC + 2CO \leftrightarrow SiO_2 + 3C \quad (2.2.4.4)$$

$$2C + O_2 \leftrightarrow 2CO \quad (2.2.4.5)$$

$$2SiC + 4O_2 \leftrightarrow 2SiO_2 + 2CO_2 \quad (2.2.4.6)$$

In all these reactions silicon dioxide is grown on the surface of the SiC even though many carbon atoms react to form carbon oxide gaseous compounds that diffuse into the environment. Instead, some carbon atoms do not react and remain on the substrate surface creating carbon clusters and dangling bonds in the interface with the oxide. The oxidation process can be modeled through equations that consider the growth rate of the oxide thickness according to a linear-parabolic trend. When the oxidation process begins, the oxygen atoms break the chemical bonds of a SiC molecules by creating compounds of the Si-O-C types from which the CO molecule and silicon atoms with dangling bonds are formed. Silicon atoms react with oxygen that reaches the SiC surface to form silicon dioxide. From the Deal-Grove model, the thickness of the grown oxide can be obtained by:

$$X^2 + A^{\#}X = B^{\#}(t + \tau) \quad (2.2.4.7)$$

t is the oxidation time, τ is the time needed to grow an initial oxide and $A^{\#}$ and $B^{\#}$ are the constants that depend on the diffusion and the reaction coefficients of oxygen, the oxidation temperature and the partial pressure of oxygen [181]. The solution of Eq. (2.2.4.7) is given by:

$$X = \frac{A^{\#}}{2}\left(\sqrt{1 + 4B^{\#}\frac{t+\tau}{A^{*2}}} - 1\right) \quad (2.2.4.8)$$

To grow thin oxides very short oxidation processes are used, thus, Eq. (2.2.4.8) can be linearly approximated as:

$$X = \frac{B^{\#}}{A^{\#}}(t + \tau) \quad (2.2.4.9)$$

$B^{\#}/A^{\#}$ is defined as linear constant rate. For thicker oxides the oxidation times become longer and X grows according a parabolic function over time such as:

$$X = \sqrt{B^{\#}(t + \tau)} \quad (2.2.4.10)$$

$B^{\#}$is defined as parabolic constant rate. To include the diffusion process of the CO in the environment, the linear constant rate becomes equal to:

$$\frac{B^{\#}}{A^{\#}} \approx \frac{C^{\#}}{N^{\#}}K_f \quad (2.2.4.11)$$

$C^{\#}$ is the equilibrium concentration coefficient of oxygen in the oxide, $k_f$ is the forward reaction constant rate and $N^{\#}$ is the number of oxygen molecules incorporated in a unit volume in the oxide.

Depending on whether the process is in the phase in which the $O_2$ diffuses in the surface of the substrate or in the phase in which the CO diffuses in the environment, the parabolic constant rate can be expressed by:

$$B^{\#} \approx \frac{2C^{\#}}{1.5N^{\#}} D_{O_2} \quad (2.2.4.12)$$

$$B^{\#} \approx \frac{2C^{\#}K_f}{N^{\#}K_r} D_{CO} \quad (2.2.4.13)$$

$D_{O2}$ and $D_{CO}$ are respectively the diffusion coefficients of oxygen molecule and of CO and $K_r$ is the constant rate of reverse reaction. The oxidation rate in SiC strongly depends on the orientation of the crystal and, in particular, in the C face of the crystal is almost an order of magnitude higher than the Si face because the emission of silicon atoms is greater [177], [187]. However, it is preferred to grow the SiC crystal along the Si face of the crystal because it has been seen that a higher deep defects density is created along the C face in the interface region which degrades the electrical properties of the power MOSFETs in SiC [178], [188]. Furthermore, the conduction band offset when the oxide has grown along the C face of the SIC crystal is lower than when the oxide has grown along the Si face, 2.29eV compared to 2.70eV, and this phenomenon increases the leakage current of the gate of the device which decreases the reliability of the oxide [178]. Typically, silicon dioxide is grown in the SiC crystal in a suitable furnace where the temperature can reach values in the range of 1000°C-1400°C. Silicon dioxide can be grown in dry atmospheres, $O_2$, or in wet atmospheres, $H_2O$. Unlike silicon substrates, in SiC substrates the bonds between carbon and silicon atoms are very strong, thus, to break them during the oxidation process requires more time and higher temperatures.

An alternative method for making $SiO_2$ is by the CVD process. In this case, a gas containing $SiO_2$ precursor molecules is transported onto the wafer in SiC by decomposing and depositing on the surface of the wafer. Typically, the gas used in the CVD process is tetraethyl orthosilicate and its decomposition is obtained by a plasma ignition or by elevated temperatures [189]. However, a disadvantage of the CVD process is that the oxide deposited on the substrate does not stick well, thus, to overcome this problem, a short thermal oxidation is carried out after the deposition to make the oxide adhere better [190]. An advantage of the CVD process is that silicon dioxide can be deposited with a reduced thermal budget and is in a short time if compared with the standard growth process. This leads to greater mobility of the carriers in the channel [185].

## 2.2.5 Defects in the Interface in SiC power MOSFETs

After silicon dioxide has grown on the surface of the SiC wafer, many defects can be observed in the interface region, in particular, since the carbon atoms left unpaired during the oxidation process form clusters between them. These defects are localized within the SiC bandgap and, as already mentioned, influence the quality of the interface by decreasing the mobility of the carriers in the channel and degrading the electrical characteristics of the MOSFETs. In fact, the defects capture the charge carriers in the device channel and, thus, are no longer available for conduction and the $I_{DS}$ decreases. Furthermore, the electrically active defects interact with the carriers in the inversion layer by coulombic scattering mechanisms affecting the mobility of the carriers. These phenomena are more marked in WBG semiconductors, such as SiC, than silicon because they have a greater bandgap and, thus, could include a greater amount of defects. The defectiveness in SiC-$SiO_2$ interface was characterized by Afanasev [64] (see figure 2.2.5.1). The defects within the SiC bandgap can be classified into three different groups: defects near the valence band, defects near the conduction band and deep level defects in the middle of the bandgap. In the standard n-channel power MOSFETs, the defects located near the valence band do not influence the electrons that flow along the channel because they act by capturing holes. Instead, deep levels and defects near the conduction band greatly affect the performances of these transistors. The experimental data of Afanasev shows that the $D_{it}$ increases considerably approaching the edge of the conduction band exceeding the value of $10^{13}cm^{-2}eV^{-1}$ and, in particular, in the 4H-SiC polytype [167]. Part of these defects have been shown to respond slowly over time with a wide distribution of energy. Therefore, it can be assumed that these defects were not exactly positioned in the interface but in proximity and more within the oxide [64], [191]. These defects are called Near Interface States, NITs, or border traps and are supposed to be positioned about 1 or 2 nanometers from the interface and due to very small carbon clusters (carbon dimers). An important spectroscopic analysis performed by Rudenko [195] has shown that NIT are composed of a combination of two types of traps: fast traps and slow traps [212]. The fast traps respond quickly to an AC signal and are due to carbon atoms present at the interface and which are located at about 0.1eV below the edge of the conduction band. Instead, the slow traps are NITs that are in the range between 0.1eV and 0.7eV below the edge of the conduction band for the 4H-SiC polytype due to oxide defects not far from the interface. Both types of defects are activated thermally. Historically, it is known that silicon dangling bonds, called $P_b$ centers, and oxygen vacancies, called E' centers, are the most common defects observed in the interface region in the case of silicon power MOSFETs [167]. However, it has experimentally observed by the EPR analysis that these defects are not the main cause found at the interface of the SiC devices. In fact, by performing an annealing in the $H_2$ atmospheres there is no significant reduction in the defectiveness as in the case of silicon devices [64]. Furthermore, it has also been observed that there is a non-stoichiometric transition layer of the Si-O-C type, oxycarbide defects, at the interface which is formed during the growth of silicon dioxide on SiC substrates [192]. This transition region is of the order of few nanometers and its stoichiometry gradually changes from SiC to silicon dioxide [193], [194]. It is believed that the transition layer is formed so that the bonds lengths between the atoms that makes the SiC are too small compared to those of the $SiO_2$ [229] at that, thus, the slow traps are located right within this region. The mobility of the carriers in the inversion layer can be strongly influenced by the roughness of the interface and this is due, in particular, to the process of step bunching during the growth of the crystal [178].

Using the AFM and TEM instrumentations that analyse the interface morphology of the Si face of a 4H-SiC crystal, it has been observed that the average roughness value is about 0.3 nm [196]. Recently, a new kind of defect has been discovered in the interface region between SiC and $SiO_2$ and has been called carboxyl defect [197]. Carboxyl is a type of oxycarbide defect caused by a carbon interstitial defect. In practice, the carbon atom binds with two silicon atoms and one oxygen atom (Si-[C=O]-Si). In the case of 4H-SiC, carboxyl can be found in two different stable electrical states: $2^+$ and neutral. Carboxyl defects act as switching oxide border hole traps in the oxide and contribute to the phenomenon of the instability of the threshold voltage. In general, when a negative voltage is applied to the gate of a n-channel SiC power MOSFET, the carboxyl defects charge positively because the holes are captured. Instead, by applying a positive potential to the gate, the electrons in the channel enter in the oxide by tunnel effect and are captured by these traps which, thus, become electrically neutral. Historically, this type of behaviour has been related to the vacancies of oxygen atoms in silicon devices [198] and this has been experimentally observed by EPR analysis [199]. Carboxyl defects are created from Si-O-C structures present in the transition layer though an exothermic reaction with a release of energy equal to 2.0eV which indicates that the carboxyl has a stable configuration. The activation barrier of this type of defect is rather low and is equal to 0.5eV. The energy of formation of the carboxyl defects in different electrical configurations can be evaluated according to the Fermi level. In this case, the Charge Transition Level, CTL, is introduced as the Fermi level at which the defect passes between two different charge states that have the same formation energy. CTL was found to be at 1.4eV above the edge of the valence band in a 4H-SiC crystal. Beyond this energy value, the carboxyl switches from a $2^+$ configuration to a neutral state.

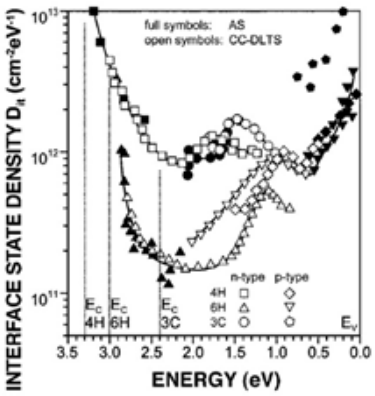



**Figure 2.2.5.1: $D_{it}$ distributions experimentally measured in the bandgap of various SiC polytypes and extrapolated from Afanasev's article of 1997 [64].**

## 2.2.6 Passivation Techniques of Defects in the Interface

In the semiconductor industry, passivation is a process used to eliminate or, better, reduce the number of defects in the interface region of power MOSFETs. There are many passivation techniques used to reduce the number of defects at the SiC-$SiO_2$ interface and most of them rely on post-oxidation annealing processes (POA). The annealing processes are based on high temperature thermal treatments of the substrate used to physically and sometime chemically alter the properties of the materials such as the SiC-$SiO_2$ interface. It is important to emphasize once again that in the SiC-$SiO_2$ interface the density of the defects is at least of two order of magnitude higher than the Si-$SiO_2$ interface, thus, it is necessary to introduce sophisticated passivation techniques to improve the performances of the transistors. One of the simple techniques used to reduce the number of defects in the interface is a re-oxidation or post-oxidation thermal treatment in an oxygen atmospheres [200]. However, this annealing process is not very effective because it has been shown that even if a significant decrease in $D_{it}$ is observed in the lower half of the bandgap, a slight increase in defect levels occur in the upper part of the bandgap. However, it has also been observed that high temperature oxidation performed up to about 1500°C can drastically reduce the defectiveness by one order of magnitude and increase the mobility of the carriers in the channel [223], [224]. One of the most used POA techniques in the silicon devices is the thermal treatment in a hydrogen atmospheres. The temperature in the oven has increased to 400°C as $H_2$ gas flows.
In silicon devices, this process passivates the $P_b$ centers efficiently and decreases defectiveness in the whole bandgap as stable Si-H bonds are formed at the interface, [203]. However, in SiC power MOSFETs, this POA technique does not lead to appreciable improvements because the dangling silicon bonds give only a small contribution to the defectiveness observed in the whole bandgap [64], [201]. Instead, it has been experimentally observed that one of the most widely used methods to reduce the density of traps at the interface of SiC-$SiO_2$ is a POA treatment with nitric oxide, NO, or with oxidations through nitrogen containing gas mixture [206], [208], [209], [210], [211], [212], [213]. Passivation with nitric oxide is the process that in many cases is currently used in the production of power MOSFETs in SiC even if, at times, $N_2O$ is preferred to NO for safety reasons. In particular, at very high temperatures, around 1200°C, the NO dissociates into individual atoms of oxygen and nitrogen and the latter create strong bonds with the silicon atoms at the interface allowing to strongly reduce the density of slow traps and increasing mobility of carriers in the device channel. It has been observed that nitrogen atoms form the following types of interface bonds in a SiC substrate for a depth of few atomic layers: N-$Si_3$, O-N-$Si_2$, $O_2$-N-Si, N-C [214]. Therefore, the POA treatment in NO also dissolves the carbon clusters and helps to remove the carbon atoms from the interface [205], [216]. Although the mechanism of how NO acts is not exactly well understood, it is believed that this gas diffuses through the oxide reaching the interface and decomposing. Some oxygen atoms oxidize the SiC surface by increasing the silicon dioxide layer while others form CO molecules that spreads out from the oxide. Instead, as already mentioned, the nitrogen atoms react with the silicon, oxygen and carbon atoms. Sometime NO passivation is carried out followed by $H_2$ passivation to improve the defectiveness in the whole SiC bandgap. This determine an increase in the mobility of the the carriers in the inversion layer of the power MOSFETs which reaches values close to 40$cm^2V^{-1}s^{-1}$ and is greater than about 15 $cm^2V^{-1}s^{-1}$ which are generally measured in the SiC power MOSFETs that perform only passivation in NO. Recently, it has also been observed that the width of the transition layer decreases by carrying out NO passivation and with increasing time of the same POA process [217]. Furthermore, nitric oxide has been observed to successfully passivates the carboxyl defects unlike the annealing treatment with $H_2$ [197]. Indeed, this process would create additional traps in the interface region similar to carboxyl defects.

POA treatment in $N_2O$ is often used for safety reasons although it has been observed that it is less effective than the NO process since there is an increase in slow interfacial states [209] while improving the quality of the interface [220]. However, it has been experimentally observed that oxides grown in the $N_2O$ atmosphere shows a better reliability of the device in conditions of high electrical stress compared to the treatment with NO thanks to the accumulation of nitrogen in the interface [226]. Another passivation technique that is used consists of nitrogen implantation before oxidation takes place. Subsequently, oxidation completely attacks the layer implanted with nitrogen. This process allow to reduce the density of the interface states near the edge of the conduction band even if a slight growth of the traps has been observed near the edge of the valence band [218], [219]. An alternative POA process to those already mentioned is obtained using phosphorous instead of NO gas. This annealing treatment can be carried out by reaching a mixture of $POCl_3$, $N_2$ and $O_2$ or $SiP_2O_7$ gases to obtain phosphosilicate glass (PSG), $P_2O_5$, at a temperature of about 1000°C. It has been observed that phosphorous annealing significantly reduces the defectiveness with respect to the NO process by increasing the mobility of the carriers in the channel [221]. However, annealing with phosphorous induces electric charges at the interface and the sign of these charges depends on the polarization of the gate, thus, this type of treatment is not practicable since it determines a marked increase in the instability of the threshold voltage [222].

Recently, a new POA process has been introduced which has given similar results to NO annealing. This treatment is based on an annealing process in an argon atmosphere carried out at very high temperatures (about 1500°C) [226]. The process of annealing with argon significantly reduces the density of the interface states near the conduction band without introducing any foreign element. Furthermore, unlike the NO process, annealing with argon does not introduce fast interfacial states [227] and hole traps in the oxide improving the quality and reliability of the device [228].

## 2.2.7 How POA treatments work in reducing defectiveness: simulations based on the DFT technique

Understanding where the different defects are energetically positioned within the bandgap and how the POA treatments passivate them is very complicated even if many deductions have been made thanks to the experiments carried out especially in the spectroscopic field. Therefore, in recent years, several studies have been carried out mainly through simulation techniques that use Density Functional Theory, DFT, to analyse the region of the $SiO_2$-SiC interface. DFT is a modeling method based on computational quantum mechanics used in physics, chemistry and materials sciences to study the atoms, molecules and electronic structures of a body system. Functional is a term used in mathematical sciences and it is related to the concept of function. A function is a rule that allows to get a number from another number. Instead, a functional is a rule that allows to get a number from a function. There are many software that allow to perform DFT analysis on semiconductor materials and, in particular, in the interface region between SiC and silicon dioxide. These commercial software simulate the behaviour of the crystal reticule and the relaxation of the structure subjected to mechanical stresses, the band-structure and the Density Of States, DOS, of the substrates in SiC and of SiC-$SiO_2$ interface. The calculations performed with the DFT are based on a reference system having plane waves as basic vectors to simulate the wave functions of each electron, the density of the same based on their position and the minimum energy of the system called the ground state. However, in this chapter, the basis of DFT theory have only been briefly mentioned for the sole purpose of obtaining the results that interest us because this is not the scope of this thesis. The theory of DFT is based on quantum mechanics which studies the microscopic behaviour of the particles that make up the material (electrons and nuclei). Each physical system tends to minimize its total energy and, thus, the interatomic distances between the atoms that make up the crystal reticule can be estimated even when defects are present inside the structure. The motion of electrons is completely described by Schrodinger's equation to calculate their positions and energies. However, in the case of a system consisting of many electrons interacting each other and with nuclei of the reticule, a very large number of Schrodinger equations must be solved, also taking into account that there is a system with 6 degrees of spatial freedom, 3 for the electron and 3 for nuclei, which is practically very complicated. Therefore, it is necessary to introduce some simplifications and approximations to obtain the solution of equations. Considering a time-invariant system, the Schrodinger equation associated with an electron can be written as:

$$\hat{\mathrm{H}}\Psi_{\mathrm{i}} = \mathbf{E}\Psi_{\mathrm{i}} \tag{2.2.7.1}$$

$\hat{\mathrm{H}}$ is the Hamiltonian associated with a particle. Therefore, considering all the particles involved, the ground state of the system can be obtained by minimizing the following functional as:

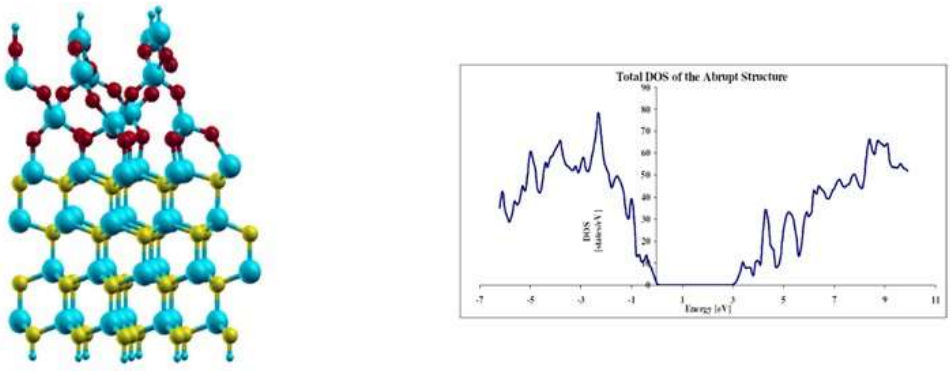
$$\mathrm{E} = \min_{\Psi}\langle\Psi|\hat{\mathrm{H}}|\Psi\rangle \tag{2.2.7.2}$$

It is important to underline that the Hamiltonian operator allows to obtain the total energy of the system as the sum of different types of energies such as the kinetic energies of electrons, the potential energy due to the Coulombic attraction between nuclei and electrons, the potential energy due to the repulsion between electrons, the kinetic energy of the nuclei and the potential energy due to the repulsion between the nuclei. The Hamiltonian operator could also include additional energy components if external electric and/or magnetic fields are applied. Therefore, DFT is based on the solution of a particular set of Schrodinger equations in which many approximations and simplifications are introduced that allow to solve a new system of equations called Kohn-Sham [230].

In the formulation of Kohn and Sham the kinetic energy of the interacting electrons in a system is replaced with an equivalent reference system in which the electrons do not interact and have the same ground state. A simplification used to solve the Kohn-Sham equation is based on the Born-Oppenheimer approximation which energetically separates the electrons from the nuclei even if the state functions of the former depend on the location of the latter. In practice, electrons remain in a given state even if the nuclei move. Therefore, the total energy of the system is given by the sum of the part due to the nuclei and that due to the electrons. Another simplification is due to Hartree's approximation. In practice, each electron interacts with the others, thus, for each interaction it should be considered a Schrodinger equation. Instead, through the Hartree approximation we consider a single Schrodinger equation or each electron since an electron interacts with the centroid of the rest of the electrons that move driven by an effective potential. In particular, the wave function trough Hartree's approximation can simply be written as the product of the individual wave functions associated with each electron. Instead, the energy equation based on the Hartree approximation considers the sum of the kinetic energy of the electrons, the interaction of the single electron with the Coulomb distribution of nuclei and the interaction of an electron with the centroid of the rest of the remaining electrons. So, we have to solve a number of equations equal to the number of electrons. Unfortunately, Hartree's approximation does not include the Pauli exclusion principle, thus, a new simplification must be considered as in the model proposed by Hartree-Fock which introduces the electron functions defined as spin orbitals. Each spin orbitals is given by the product between a spatial orbital and one of the two spin functions. Spin functions are orthonormal functions that minimize electron energy. In the Hartree-Fock model, the equivalent electron wave function is approximated by the product of a number of antisymmetric functions equal to the total number of electrons in the system, each of them associated with each electron (Slater determinant).

In Kohn-Sham's equations the interaction between electrons is divided into two parts. The first part is the exchange correlation takes into account the Pauli exclusion principle. The second part is defined as correlation interaction and takes into account Coulomb's repulsive interactions between electrons. The Kohn-Sham equations are based on the two Hohenberg-Kohn theorems. The first stated that the potential of the nuclei depends only on the DOS. The second states that the ground state of the system can be obtained by varying the DOS and using the Lagrange multiplicator method to minimize the entire energy of the system. In summary, Kohn-Sham equations are a set of pseudo Schrodinger equations of independent electrons that interact with an effective potential. Finally, the Kohn-Sham equations take into account the sum of four energetic terms: the kinetic energy of system which the elements do not interact, the potential energy of the nuclei, the Hartree potential energy deriving from the classic Coulomb repulsion between electrons that have a certain DOS and the potential energy to exchange correlation. The first three energy components can be easily calculated while the exchange correlation component is more complicated to estimate. The latter component also includes the phenomena of quantum mechanics. A more precise estimate of the exchange correlation component can be obtained by suitably choosing the functional. One of the most used functional is the local density functional, LDA, which depends exclusively on the DOS and on the generalized gradient approximation functional, GGA [231]. However, when considering the entire reticule, there exist an infinite number of nuclei and electrons that move due to the effect of an effective potential. Therefore, to simplify the study, it is possible to assume that the reticule is composed of single supercells that repeat in the space in which suitable boundary conditions are considered. The regularity of the calculation is guaranteed by the Bloch's theorem applied to the functions of the electronic wave.

If defects are introduced in the interface region between SiC and silicon dioxide, it is necessary to take into account the Hellman-Feynman theory that simulates how atoms and molecules are arranged in the reticule to reduce mechanical stress and, thus, achieve equilibrium in which the entire energy of the system is minimized. An interesting work that simulate the behaviour of the defects in the interface and how POA techniques act to reduce defectiveness, thanks to the estimation of DOS within the SiC bandgap, was made by Salemi in his PhD thesis [232] using an open source software called Quantum Espresso DFT along the Si face of the substrate [233]. First of all, Salemi simulated DOS at the 4H-SiC interface with the oxide without introducing any defects (see figure 2.2.7.1). From figure 2.2.7.1b it is noted that the estimated bandgap is equal to 3.26eV as experimentally obtained. Subsequently, Salemi showed that introducing a silicon vacancy creates interfacial states within the SiC bandgap just above the valence band ($E_v$ + 0.8eV) which can be easily passivated with hydrogen atoms (see figure 2.2.7.2). Salemi also simulated the effect produced by an interstitial carbon atom in the interface region. This defect introduces traps close to both the conduction band and the valence band (see figure 2.2.7.3). From the simulation made by Salemi, it has been shown that passivation with nitrogen eliminates the interfacial states within the bandgap unlike the treatment with hydrogen only. In a further example, Salemi demonstrates that an oxygen vacancy in the interface creates interface states within the bandgap close to the conduction band that can be passivated by annealing in the atmosphere with nitrogen (see figure 2.2.7.4). Finally, Salemi shows how the introduction of an oxycarbide defect at the interface region creates a transition layer which introduces traps within the bandgap close to both the valence band and the conduction band which can be passivated by annealing in the atmosphere with nitrogen (see figure 2.2.7.5).




a) b)

**Figure 2.2.7.1: Simulation of the interface region between 4H-SiC and $SiO_2$ without defects. DFT analysis extracted from Salemi's PhD thesis [232]: a) elementary reticular structure; b) DOS analysis.**

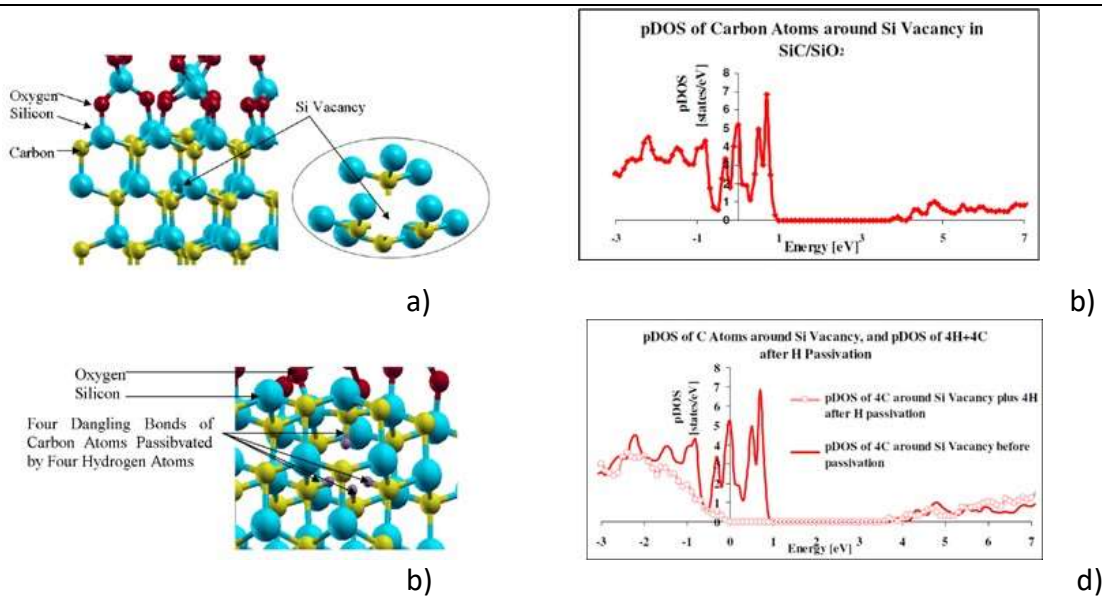



**Figure 2.2.7.2: Interface region between 4H-SiC and $SiO_2$. DFT analysis extracted from Salemi's PhD thesis [232]: a) elementary reticular structure with a silicon vacancy; b) DOS analysis with silicon vacancy; c) elementary reticular structure in which the hydrogen atoms passivate the silicon vacancy; d) DOS analysis with silicon vacancy passivated by hydrogen atoms.**

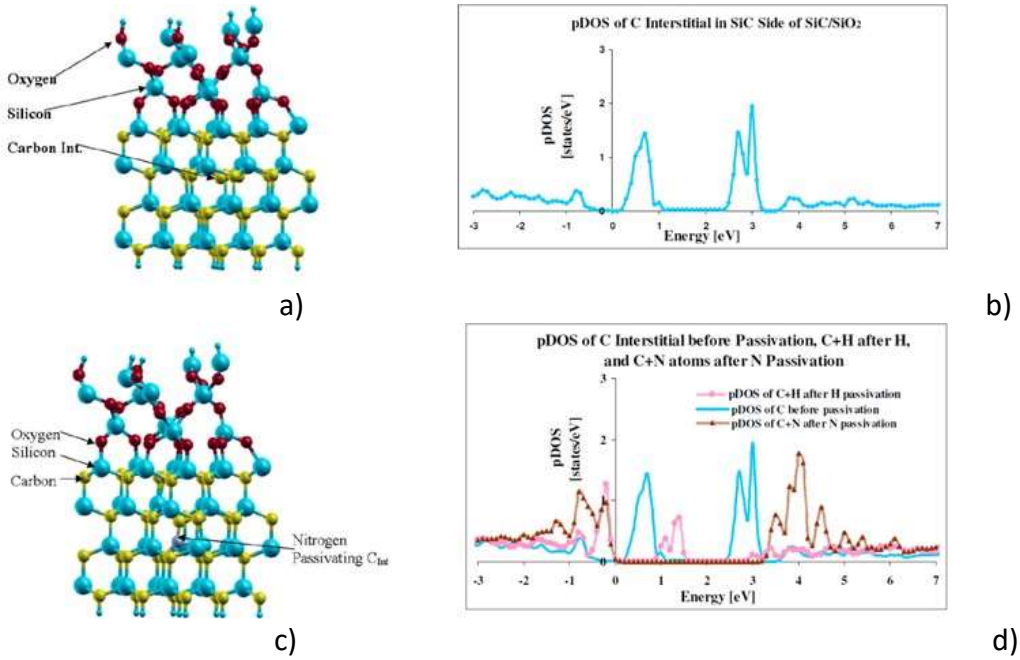
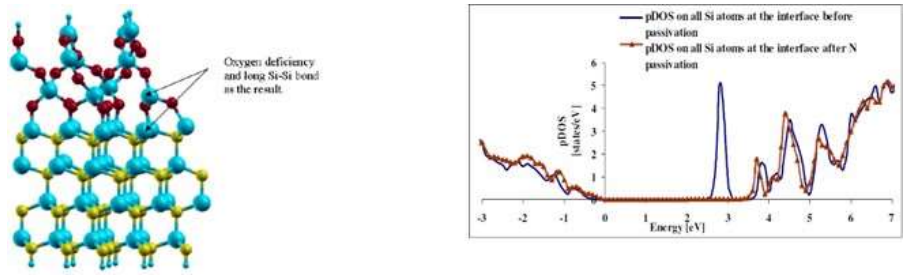
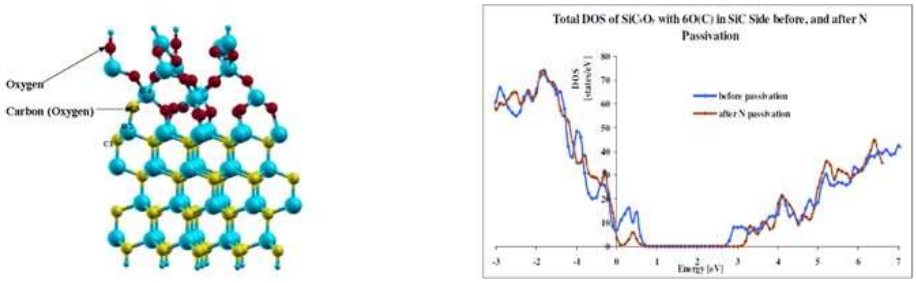



**Figure 2.2.7.3: Interface region between 4H-SiC and $SiO_2$. DFT analysis extracted from the Salemi's PhD thesis in which an interstitial carbon defect is present [232]: a) elementary reticular structure in which the interstitial carbon defect is present; b) DOS analysis with interstitial carbon defect; c) elementary reticular structure showing how the interstitial defect of carbon is passivated by nitrogen atom; d) DOS analysis showing how the interstitial defect of carbon is passivated by both nitrogen and hydrogen.**




a) b)

**Figure 3.9.4: Interface between 4H-SiC and $SiO_2$. DFT analysis extracted by Salemi's PhD thesis which considers an oxygen vacancy [232]: a) elementary reticular structure with the oxygen vacancy; b) DOS analysis with and without nitrogen annealing of the oxygen vacancy.**




a) b)

**Figure 2.2.7.5: Interface region between 4H-SiC and $SiO_2$. DFT analysis extracted from Salemi's PhD thesis which considers an oxycarbide defect [232]: a) elementary reticular structure with an oxycarbide defect; b) DOS analysis with and without nitrogen annealing of the oxycarbide defect.**

# 3 Low frequency Noise in power MOSFETs

## 3.1 Fundamentals of noises analysis in electronics

Any stochastic fluctuation related to an observable physical variable that superimpose the original deterministic signal is called noise. In electronics we speak of noise every time stochastic fluctuations affect voltages or currents. Noise is a fundamental aspect of all electronic circuits. Generally, when you add any electronic component to a circuit, the noise increases. In this context, noises can be represented through the chaotic movement of carriers within an electronic devices. Noises can be generated both from external sources and internal sources to the component and circuit. External noises are due to electromagnetic fields present in the environment and coming from other electronic components and circuits that are nearby. This type of noise can be attenuated by placing the electronic component or the entire circuit inside a metal box that acts as a Faraday cage. The electromagnetic signal from the electrical network that feeds the circuit is also a source of noise. In this case, the signal will appear at the 50Hz frequency. Instead, in the case of internal sources of noise, it is possible to distinguish between different causes. The sources of noise from electronic components, as in the case of power MOSFETs, are thermal noise, shot noise, GR noise, RTS noise and flicker noise. Typically, noise can be characterized by its statistical properties such as the distribution of the signal amplitude or the average power of the same signal. The distribution of the amplitude of the noise provides information on the frequency with which the different amplitudes of the signal over time are detected. This information allows to obtain the Probability Density Function, PDF, f(X), of the signal. Therefore, having fixed an instant of time and given a stochastic variable X, the probability associated with the occurrence of the event, described by the variable in the interval of X+dX, is obtained as [235]:

$$dP = f(X)dX \tag{3.1.1}$$

If the event is confined in the interval [a, b], it is possible to obtain:

$$\int_a^b f(X)dX = 1 \tag{3.1.2}$$

The average value associated with the X through its distribution is obtained as:

$$\overline{X} = \int_a^b Xf(X)dX \tag{3.1.3}$$

and the associated variance it is equal to:

$$\sigma^2(X) = \int_a^b (X - \overline{X})^2 f(X)dX \tag{3.1.4}$$

Typically, the distribution of the amplitude associated with voltage and current fluctuations take the Gaussian shape as:

$$f(X) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(X-\overline{X})^2}{2\sigma^2}} \tag{3.1.5}$$

When the average value and variance are constant over time, the stochastic process is called stationary. It is important to underline that in a stochastic process the event observed in an certain instant of time is often influenced by the events that occurred previously. This phenomenon is called persistence. A stochastic process has an accentuated persistence when the observed event is related to events very distant in time. A persistent stochastic process is called ergodic. In the case of an electrical resistance, R, the average power associated with the variable X is written as:

$$P = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \frac{V^2(t)}{R} dt = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} R\, I^2(t)\, dt \quad (3.1.6)$$

In order to simplify the study, the average power associated with noise is normalized to 1Ω, thus, it is expressed in $V^2$ or $A^2$ instead of W. Many times information on noise is obtained by moving from the time domain to the frequency domain by carrying out the Fourier transform of the signal and studying its Power Spectral Density, PSD, also called spectrum [234]. In the case of a stochastic process, the PSD in the frequency domain, S(f), can be expressed in $V^2Hz^{-1}$ or $A^2Hz^{-1}$ and it is often normalized to 1Ω. The one-side spectrum is obtained by applying the Wiener-Khintchine theorem as:

$$S(f) = 2\int_{-\infty}^{+\infty} \overline{X(t)X(t+s)} e^{-j\omega s} ds \quad (3.1.7)$$

with:

$$\overline{X(t)X(t+s)} = \lim_{T\to\infty} \int_0^T X(t)X(t+s)e^{-j\omega s} dt \quad (3.1.8)$$

The part of the spectrum at negative frequencies is evaluated in the positive part of the same spectrum. If s is equal to 0, it is possible to obtain:

$$P = \overline{X^2(t)} = \int_0^{+\infty} S(f) df \quad (3.1.9)$$

If PSD is constant across the entire frequency domain, the stochastic process is called white noise. In the electronic components such as power MOSFETs, it is usually observed that the PSD depends on the same f at low frequencies and becomes a white noise for higher frequencies.

For electronic components, the current flowing along a layer of length L, as in the case of the channel of a power MOSFET, can be obtained as:

$$I(t) = \frac{q}{L} \sum_{i=1}^{N^*(t)} v_i(t) \quad (3.1.10)$$

N* is the number of free carriers and $v_i$ is the drift velocity of each of them. These two parameters can change over time and can be derived by:

$$N^*(t) = \overline{N^*} + \Delta N^*(t) \quad (3.1.11)$$

$$v_i(t) = \bar{v} + \Delta v_i(t) \quad (3.1.12)$$

Therefore, the fluctuation of the current can be obtained by:

$$\Delta I(t) = \frac{q}{L} \bar{v} \Delta N^*(t) + \frac{q}{L} \sum_{i=1}^{\overline{N^*}} \Delta v_i(t) \quad (3.1.13)$$

Given that the velocity of the carriers depends on their mobility such as:

$$v = \mu E^* \quad (3.1.14)$$

The Eq.(3.1.13) can be rewritten as:

$$\Delta I(t) = \frac{q}{L} \mu E^* \Delta N^*(t) + \frac{q}{L} E^* \sum_{i=1}^{\overline{N^*}} \Delta \mu_i(t) \quad (3.1.15)$$

Therefore, there are two possible causes that generate noise in the current and voltage signals in power devices. The first cause is due to the fluctuation in the number of carriers in the device channel. The second cause is due to the fluctuation of the mobility of the carriers in the device channel. Low frequency noise, also called flicker noise or pink noise, was first discovered by Johnson in 1925 during an experiment designed to study shot noise in vacuum tubes [236]. Subsequently, Schottky theoretically modeled the noise signal observed by Johnson [237]. At the beginning of the process, it is possible to assume that there are $N_{t0}$ traps available to be occupied by electrons. The free electrons available to occupy the traps are several orders of magnitude greater than $N_{t0}$. By applying an electric field on the gate of the device, some electrons begins to occupy the traps, thus, after a time interval equal to Δt, the free traps decrease down to $N_t(t+\Delta t) < N_{t0}$. The number of traps occupied during the time interval Δt is equal to $-\Delta N_t(t) = N_t(t) - N_t(t-1)$ and the rate with which the electrons remain trapped is achieved by:

$$\frac{\Delta N_t(t)}{\Delta t} = -\alpha^* N_t(t) \quad (3.1.16)$$

$\alpha^*$ is the inverse of the time constant relative to the captured electrons. In an infinitesimal time interval, dt, integrating Eq. (3.1.16), it is possible to achieve the number of traps available over time as obtained by Schottky as:

$$N_t(t) = N_{t0}e^{-\alpha^* t} \tag{3.1.17}$$

Similarly, during the electron release phase, it is possible to obtain the number of traps available over time such as:

$$N_t(t) = N_{t0}\left(1 - e^{-\beta^* t}\right) \tag{3.1.18}$$

$\beta^*$ is the inverse of the constant of time to the released electrons. Typically, $\alpha^*$ and $\beta^*$ have different values.

### 3.1.1 Thermal noise

Thermal noise is also called Nyquist or Johnson noise. It is due to the chaotic thermal movement of the electrons inside the material that determine the fluctuation of the current. Since the movement of electrons is purely random, the average value of the noise signal over time is always 0. The PSD associated with thermal noise expressed in terms of both current and voltage is equal to:

$$S_I = \frac{4KT}{R} \tag{3.1.1.1}$$

$$S_V = 4KTR \tag{3.1.1.2}$$

The thermal noise was discovered by Johnson [238] and then theoretically explained by Nyquist [239]. The thermal noise exists in every material that has an electrical resistance and is usually the one that sets a minimum value to the power of noise in an electric circuit. The thermal noise behaves like a white noise even if, for physical reasons, it should not considered such since the PSD cannot extend up to infinite frequencies.

## 3.1.2 Shot noise

Shot noise occurs as a result of the discrete movement of charges that pass through a barrier potential randomly as an np junction. The PSD associated with the shot noise can be obtained as:

$$S_I = 2qI \tag{3.1.2.1}$$

In the case of an np junction, the current of the ideal diode can be obtained as:

$$I = I_0\left(e^{\frac{qV}{KT}} - 1\right) \tag{3.1.2.2}$$

It is obtained from the sum of forward and backward currents and the PSD is obtained from:

$$S_I = 2qI_0\left(e^{\frac{qV}{KT}} + 1\right) \tag{3.1.2.3}$$

From the Eq. (3.1.2.2), the dynamic resistance of the junction is obtained as:

$$R = \left(\frac{dI}{dV}\right)^{-1} = \frac{KT}{qI_0 e^{\frac{qV}{KT}}} \tag{3.1.2.4}$$

By reordering the terms of Eq. (3.1.2.4) and replacing it in Eq. (3.1.2.3), for V equal to 0, it is possible to obtain:

$$S_I = \frac{4KT}{R} \tag{3.1.2.5}$$

Therefore, the latter equation shows as shot noise and thermal noise are closely related because Eq. (3.1.2.5) is equal to Eq. (3.1.1.1). However, Eq. (3.1.2.1) is valid for frequencies lower than a value set by the transition time of the charges through the potential barrier.

## 3.1.3 Generation-Recombination noise

Generation and recombination processes are SRH phenomena, Shockley-Read-Hall, that occur in indirect bandgap of semiconductors such as SiC and silicon. In electronic components, such as power MOSFETs, the physical origin of the LF noise can be attributed to changes in the density of the carriers in the channel due to the fluctuations of the states of the G-R centers in the channel of the devices and with particular reference to the states within the bandgap [240]. The first experimental observations of LF noise in MOSFET devices have been reported by Ralls et al. [241] and Uren et al. [242] since 1984. The PSD associated with the fluctuation in the number of carriers is obtained from [235]:

$$S_{N^*} = 4\overline{\Delta N^{*2}} \frac{\tau}{1+(2\pi f)^2\tau^2} \tag{3.1.3.1}$$

$\overline{\Delta N^*}$ is the variation in the number of electrons and $\tau$ the time constant. It is possible to affirm that the G-R processes become significative only when the $E_F$ Fermi level is close enough, and in the range of a few KT, to the energy levels of the traps and the case where $\tau_c$, capture time constant, and $\tau_e$, emission time constant, are almost equal. In fact, when $E_F$ is greater than the energy levels of the traps, these will be filled. However, if $E_F$ is lower than the energy levels of the traps, they will be almost completely empty. Considering that $N^*>>N_t$, and that $\overline{\Delta N^{*2}}$ can be approximated to $N_t/4$, it is possible to obtain the PSD in terms of current such as [235]:

$$S_I = I^2 \frac{N_t}{N^{*2}} \frac{\tau_c}{1+(2\pi f)^2\tau^2} \tag{3.1.3.2}$$

From this equation, it is possible to observe that the PSD depends linearly on the number of traps. The spectrum associated with Eq. (3.1.3.2) is called Lorentzian and can be represented in log-log scales as in figure 3.1.3.1.

### 3.1.3.1 RTS noise

RTS stands for Random Telegraph Signal noise and is a special case of G-R noise. In fact, RTS is due to the transition of the current and voltage signals between two different established levels called high and low. This noise is composed of random impulses with variable length and fixed height and can be attributed to the presence of a single trap or few traps. RTS is also called burst or popcorn noise. This noise is a stochastic process which has a Poisson distribution. The PSD of an RTS noise is equal to [235]:

$$S_I = \frac{4\Delta I^2}{(\tau_c+\tau_h)+\left[(2\pi f)^2+\left(\frac{1}{\tau_c}+\frac{1}{\tau_e}\right)^2\right]} \quad (3.1.3.1.1)$$

where the term $\frac{1}{\tau_c}+\frac{1}{\tau_e}$ is the average trapping time [243]. The PSD of an RTS noise shows the same Lorentzian shape as the G-R noise. Furthermore, RTS noises, like G-R noises, depend heavily on temperature [244]. Typically, RTS can be observed in MOSFETs with small areas or in large devices in which only a small part of the area is involved in the phenomenon.

## 3.1.4 Flicker noise

As mentioned in chapter 3.1, flicker noises were first discovered by Johnson in 1925 during an experiment to study shot noise in vacuum tubes. Flicker noises are low frequency noises and their peculiarity is that the spectrum is proportional to $1/f^{\gamma^*}$ with $\gamma^*$ in the range of 0.7-1.3. Typically, $\gamma^*$ approaches 1. In this case the noise signal is also called pink noise. The PSD of a flicker noise is given by:

$$S_I = K^{\#} \frac{I^{\beta^{\#}}}{f^{\gamma^*}} \tag{3.1.4.1}$$

$K^{\#}$ is a constant that depends on the device and $\beta^{\#}$ has a value in the range of 0.5-2.

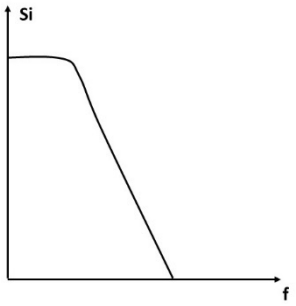



**Figure 3.1.3.1: Lorentzian shape of the spectrum of a noise signal due to SRH processes.**

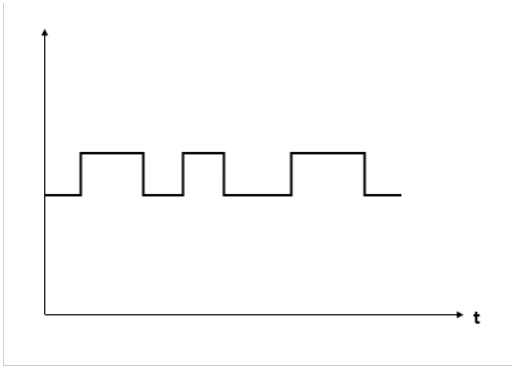



**Figure 3.1.3.1.1: Example of RTS noise in the time domain.**

According to Eq. (3.1.17) proposed by Schottky, flicker noise can be modeled with a Poisson process. Furthermore, it is possible to hypothesize that the stochastic process is composed of many G-R events with different $\alpha_i^*$. Therefore, Eq. (3.1.17) can be rewritten as:

$$N_t(t) = \sum_i N_{t0i} e^{-\alpha_i^* t} \tag{3.1.4.2}$$

According to the study conducted by Bernamont, from the superposition of many stochastic processes with different trapping times, a flicker noise is obtained for a reasonable range of frequencies [245]. When $\alpha_i^*$ are uniformly distributed between two different values, $\alpha_1^*$ and $\alpha_2^*$, the expression of the PSD can obtained as:

$$S_{N^*} = \begin{cases} n^* N_{t0} & 0 \ll f \ll \alpha_1^* \ll \alpha_2^* \\ \frac{n^* \pi N_{t0}}{2f(\alpha_2^* - \alpha_1^*)} & 0 \ll \alpha_1^* \ll f \ll \alpha_2^* \\ \frac{n^* N_{t0}}{f^2} & 0 \ll \alpha_1^* \ll \alpha_2^* \ll f \end{cases} \tag{3.1.4.3}$$

Therefore, the PSD associated with Eq. (3.1.4.2) represents a pink noise only in the frequency range between $\alpha_1^*$ and $\alpha_2^*$. On the other hand, for frequencies lower than $\alpha_1^*$, the stochastic process behaves like a white noise, and for frequencies higher than $\alpha_2^*$, the PSD takes the shape of a Lorentzian function which is generally used to describe the Brownian movement of particles in a medium. A flicker noise can also be generated when the time constants of the G-R events are distributed over time as [246]:

$$g(\tau) = \begin{cases} \frac{1}{\tau \ln\left(\frac{\alpha_1^*}{\alpha_2^*}\right)} & 0 \ll \alpha_1^* \ll \frac{1}{\tau} \ll \alpha_2^* \\ 0 & 0 \ll \frac{1}{\tau} \ll \alpha_1^* \text{ and } \alpha_2^* \ll \frac{1}{\tau} \end{cases} \quad (3.1.4.4)$$

where the term $\ln\left(\frac{\alpha_1^*}{\alpha_2^*}\right)$ is used to normalize the probability function. Therefore, from Eq. (3.1.3.1), the PSD of noise can be obtained as:

$$S(f) = \int_0^{+\infty} g(\tau) S_{N^*}(\tau)\, d\tau \quad (3.1.4.5)$$

By solving Eq. (3.1.4.5), it is possible to obtain:

$$S_{N^*} = \begin{cases} \frac{2\overline{\Delta N^*}}{\pi \alpha_1^* \ln\left(\frac{\alpha_1^*}{\alpha_2^*}\right)} & 0 \ll f \ll \alpha_1^* \ll \alpha_2^* \\ \frac{\overline{\Delta N^{*2}}}{f \ln\left(\frac{\alpha_1^*}{\alpha_2^*}\right)} & 0 \ll \alpha_1^* \ll f \ll \alpha_2^* \\ \frac{\overline{\Delta N^{*2}}}{\pi^2 f^2 \ln\left(\frac{\alpha_1^*}{\alpha_2^*}\right)} & 0 \ll \alpha_1^* \ll \alpha_2^* \ll f \end{cases} \quad (3.1.4.6)$$

These results are quite similar to Bernamont's results. When the noise signal takes a power law expression, the process is called fractal shot noise and the spectrum is obtained as:

$$S(f) \propto \frac{1}{f^{2(1-\alpha^{\#})}} \quad (3.1.4.7)$$

$\alpha^{\#}$ is a coefficient related to the fractal shot noise. When $\alpha^{\#}$ is equal to 0.5, the stochastic process becomes a pink noise. It is worth noting that the PSD graph obtained from Eq. (3.1.4.1) in log-log scales it is linearly dependent of the frequency because the spectrum can be written as (see figure 3.1.3.1):

$$\ln(S_I) = \ln\left(K^{\#} \frac{I^{\beta^{\#}}}{f^{\gamma^*}}\right) = -\gamma^* \ln(f) + \ln\left(K^{\#} I^{\beta^{\#}}\right) \quad (3.1.4.8)$$

## 3.2 McWhorter model

In 1957, McWhorter developed a sophisticated model in which noise was attributed to trapping and emission processes of electrons from the energetic states of traps within the bandgap [248]. In fact, from Eq. (3.1.15), the noise in the current of the power MOSFETs can be due to several factors. The first factor is related to the fluctuation of the number of carriers while the second factor concerns the fluctuation of the mobility of the carriers. The McWhorter model, also called Number Fluctuation Model, is related to the first factor. McWhorter's model is based on several assumption:

a) The phenomenon of the charges trapped in the interface region affects only the density of the charges in the device channel and not the mobility.
b) The Power MOSFETs work in the strong inverse regime, thus, the carriers move from the semiconductor conduction band into the traps placed in the dielectric through a tunneling mechanism.
c) Power MOSFETs work in linear region, thus, the bending of the bands along the source- drain direction, the charge present in the inversion layer, the mobility of the carriers and the electric field near the interface are constants.
d) When tunneling towards the interface traps, the electrons must cross a rectangular barrier potential given by the difference between the conduction band of the dielectric and that of semiconductor.
e) The centroid of the charge trapped inside the dielectric layer induces a charge in the channel which depends on its distance from the interface region. Generally, this distance is very small compared to the $t_{OX}$, and it is possible to assume that both charges are equal.

Taking in account these assumptions, for a n-channel device, the drain current can be written as:

$$I_{DS} = \frac{\mu_n \mathbf{W}}{\mathbf{L}} |Q_c| V_{DS} \tag{3.2.1}$$

Therefore, a variation in current is only due to a change in the charge in the channel such as:

$$\Delta I_{ds} = \mu \frac{W}{L} V_{ds} \Delta |Q_c| = I_{ds} \frac{\Delta |Q_c|}{|Q_c|} \tag{3.2.2}$$

The PSD associated with the $I_{ds}$ becomes equal to:

$$S_I = \frac{{I_{ds}}^2}{|Q_c|^2} \Delta |Q_c|^2 = \frac{q^2 {I_{ds}}^2}{|Q_c|^2} S_{N^*} \tag{3.2.3}$$

and, again, it is possible to obtain:

$$S_I = \frac{q^2 {I_{ds}}^2}{[C_{OX}(V_{GS} - V_{th})]^2} S_{N^*} = \left(\frac{q}{\mathbf{WL}}\right)^2 \frac{{I_{ds}}^2}{{C_{ox}}^2 (V_{GS} - V_{th})^2} S_{N^*} \tag{3.2.4}$$

$S_{N^*}$ is the PSD obtained from Eq. (3.1.3.1) for G-R noise. Whereas $\overline{\Delta N^{*2}}$ can also be approximated as [249]:

$$\overline{\Delta N^{*2}} = N_t f(E)[1 - f(E)] \tag{3.2.5}$$

and that:

$$N_t f(E)[1 - f(E)] = N_t(E_F) KT \tag{3.2.6}$$

f(E) is the Fermi-Dirac distribution. Since the distribution is rather concentrated in the quasi-Fermi level, Eq. (3.1.3.1) can be rewritten as:

$$S_{N^*} = 4 N_t f(E)[1 - f(E)] \frac{\tau}{1 + (2\pi f)^2 \tau^2} \approx 4 N_t KT \frac{\tau}{1 + (2\pi f)^2 \tau^2} \tag{3.2.7}$$

In fact, only the traps that have energy in a short range of the $E_F$ contribute to the fluctuation of the current because for states that have lower or higher energies the traps are always filled or empty.

By integrating Eq. (3.2.7), it is possible to obtain the contribution of all the traps in the generation of noise as:

$$S_{N^*} = 4KT \int_{E_v}^{E_c} \int_0^{\mathbf{W}} \int_0^{\mathbf{L}} \int_0^{t_{ox}} N_t \frac{\tau}{1+(2\pi f)^2\tau^2} \, dx dy dz dE \tag{3.2.8}$$

Previously it was assumed that the electrons were trapped in the oxide via a FN tunneling process. The tunneling probability can be obtained by means of the attenuation length parameter, $\lambda^*$, as foreseen by the theory of WKB [250]. In the McWhorter model, for each interfacial states, trapping events are assumed to occur considering a time constant that varies as a function of the distance from the interface such as:

$$\tau = \tau_0(E)e^{-\frac{x}{\lambda^*}} \tag{3.2.9}$$

Based on what has been observed in silicon, $\tau_0$ is equal to about $10^{-10}$s and $\lambda^*$ is equal to about $10^{-10}$m. Therefore, the depth x can is between 0.7nm and 2.6nm for frequencies between 0.01-$10^6$Hz. In practice, traps located very close to the interface region are very fast to generate flicker noises while those located 3nm away are too slow to be observed [235]. Therefore, in the case of traps evenly distributed within the oxide, taking into account Eq. (3.2.4), given the Eq. (3.2.9) and solving Eq. (3.2.8), it is possible to obtain:

$$S_I = \frac{q^2\lambda^* KTN_t(E_F)}{\mathbf{WL}{C_{ox}}^2} \frac{1}{f} \frac{{I_{ds}}^2}{(V_{GS}-V_{th})^2} \tag{3.2.10}$$

In practice, the spectrum of the current is a pink noise that depends on the number of traps placed in a given energy level within the bandgap and which depends on the inverse of the square of the difference between the applied $V_{GS}$ and the $V_{th}$. If the traps are not evenly distributed near the oxide interface, Eq. (3.2.10) can be rewritten as [235]:

$$S_I = \frac{q^2\lambda^* KTN_t(E_F)}{\mathbf{WL}{C_{ox}}^2} \frac{1}{f^{\gamma^*}} \frac{{I_{ds}}^2}{(V_{GS}-V_{th})^2} \tag{3.2.11}$$

In the case where $\gamma^*<1$, the trap density is higher near the interface region. Instead, when $\gamma^*>1$, the trap density is higher as you move away from the interface. Many times, current spectrum normalizes to be able to compare the defectiveness between different devices. Therefore, Eq. (3.2.11) becomes [251]:

$$\frac{S_I}{{I_{ds}}^2} = \frac{q^2\lambda^* KTN_t(E_F)}{\mathbf{WL}{C_{ox}}^2} \frac{1}{f^{\gamma^*}} \frac{1}{(V_{GS}-V_{th})^2} \tag{3.2.12}$$

The power spectrum can be also defined in terms of gate voltage instead of current. Considering that the drain current can be written as:

$$I_{DS} = g_{fs}(V_{GS} - V_{th}) \tag{3.2.13}$$

Therefore, from Eq. (3.2.13), it is possible to obtain the square of $g_{fs}$ as:

$${g_{fs}}^2 = \frac{{I_{ds}}^2}{(V_{GS}-V_{th})^2} \tag{3.2.14}$$

By replacing Eq. (3.2.14) in Eq. (3.2.11), the power spectrum referred to gate voltage become equal to:

$$S_V = \frac{S_I}{{g_{fs}}^2} = \frac{q^2\lambda^* KTN_t(E_F)}{\mathbf{WL}{C_{ox}}^2} \frac{1}{f^{\gamma^*}} \tag{3.2.15}$$

Finally, it is important to highlight that traps can also be thermally activated. The time constant associated with this process assumes an exponential trend according to the energy of the interfacial states as [252]:

$$\tau = \tau_0(E)e^{\frac{E}{KT}} \tag{3.2.16}$$

## 3.3 Mobility fluctuation model

In chapter 3.1 and, in particular, from Eq. (3.1.15), it has been observed that the fluctuation of the current can also be due to the fluctuation of the in the mobility and not only to the variation in the number of the carriers. This second mechanism was first studied by Hooge in 1969 [253], [254]. The mobility fluctuation model proposed by Hooge is based on an empirical expression that considers a generic conductor that has an electrical resistance, R. The normalized spectrum associated with the mobility fluctuation is equal to:

$$\frac{S_R}{R^2} = \frac{\alpha_H}{f\,\overline{N^*}} \tag{3.3.1}$$

$\alpha_H$ is a dimensionless parameter defined as a Hooge parameter that has a value between $10^{-6}$ and $10^{-3}$. In particular, Eq. (3.3.1) can be derived from Eq. (3.1.15) as:

$$\Delta I(t) = \frac{q}{L} E^* \sum_{i=1}^{\overline{N^*}} \Delta\mu_i(t) \tag{3.3.2}$$

In the event that the fluctuation of each carrier does not affect the others, Eq. (3.3.2) can be written as:

$$\Delta I(t) = \frac{q}{L}\overline{N^*}E^*\Delta\mu_i(t) = \frac{\Delta\mu_i(t)}{\mu_i\,\boldsymbol{\rho}}E^* \tag{3.3.3}$$

By reordering Eq. (3.3.3), it is possible to obtain:

$$\frac{\Delta\mu_i(t)}{\mu_i} = \boldsymbol{\rho}\frac{\Delta I(t)}{E^*} = \frac{\Delta I(t)}{I(t)} \tag{3.3.4}$$

Therefore, even taking into account Eq. (3.3.1), the normalized power spectrum can be written as:

$$\frac{S_I}{{I_{ds}}^2} = \frac{S_{\mu_i}}{{\mu_i}^2} = \frac{S_R}{R^2} = \frac{\alpha_H}{f\,\overline{N^*}} \tag{3.3.5}$$

In practice, the spectrum represents a pink noise as observed by Hooge. The number of carriers in the inversion layer of the power MOSFETs working in linear regime can be obtained by:

$$\overline{N^*} = \frac{\boldsymbol{WL}}{q}|Q_c| = \frac{\boldsymbol{WL}}{q}C_{ox}(V_{GS} - V_{th}) \tag{3.3.6}$$

and, thus, the normalized power spectrum is equal to:

$$\frac{S_I}{{I_{ds}}^2} = \frac{q\,\alpha_H}{f\,\boldsymbol{WL}\,C_{ox}(V_{GS}-V_{th})} \tag{3.3.7}$$

Therefore, the power spectrum in the mobility fluctuation regime depends on the inverse of the difference between the applied $V_{GS}$ and the $V_{th}$ rather than on the inverse of the square as obtained in the number fluctuation model.

## 3.4 Correlated number-mobility fluctuation model

In McWhorter model it was assumed that the noise was due only to the fluctuation of the number of carriers and, thus, the mobility of each of them is not influenced by the others. However, this scenario is unrealistic because the trapping and releasing charge processes from the interface region affect the density of the charge in the inversion layer and, thus, also on the mobility of the carriers. This phenomenon is called correlated number-mobility fluctuation process [256]. In practice, a fluctuation of the charge stored in the oxide causes a fluctuation in the $V_{FB}$ such as:

$$\delta V_{FB} = -\frac{\delta Q_{OX}}{C_{OX}} \tag{3.4.1}$$

Therefore, the change in the $I_{DS}$ is due to the sum of the change in the current obtained from the change in the $V_{FB}$ and that due to the change in mobility, $\mu_{eff}$, such as:

$$\delta I_{DS} = \frac{\partial I_{DS}}{\partial V_{FB}} \delta V_{FB} + \frac{I_{DS}}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{OX}} \delta Q_{OX} \tag{3.4.2}$$

Considering that:

$$\frac{\partial I_{DS}}{\partial V_{FB}} = \frac{\partial I_{DS}}{\partial V_{GS}} = -g_{fs} \tag{3.4.3}$$

and:

$$\alpha^{+} = \frac{1}{\mu_{eff}^{2}} \frac{\partial \mu_{eff}}{\partial Q_{OX}} \tag{3.4.4}$$

$\alpha^{+}$ is the scattering parameter related to the number-mobility fluctuation model, from Eq. (3.4.1), Eq. (3.4.2) can be rewritten as:

$$\delta I_{DS} = (-g_{fs} + \alpha^{+} \mu_{eff} I_{DS} C_{OX}) \delta V_{FB} \tag{3.4.5}$$

The spectrum associated with Eq. (3.4.5) becomes equal to:

$$S_I = \frac{q^2 \lambda^* K T N_t(E_F)}{WLC_{ox}^{\ 2}} \frac{1}{f^{\gamma^*}} g_{fs}^{\ 2} \left(1 + \frac{\alpha^{+} \mu_{eff} I_{DS} C_{OX}}{g_{fs}}\right)^2 \tag{3.4.6}$$

## 3.5 Unified model for flicker noise

The unified model was proposed in 1990 by Hung et al. in order to combine both the McWhorter's model and the mobility fluctuation models [256]. Given a channel section of a power MOSFET of length Δx and perimeter **W**, the $I_{DS}$ can be written as:

$$I_{DS} = q\mu \mathbf{W} \overline{N^*} E^* \tag{3.5.1}$$

As already mentioned, the fluctuation of the current can be due both to the fluctuation of the number of carriers and to the fluctuation of the mobility and, in this case, it can be obtained as:

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{\overline{\Delta N^*}} \frac{\delta \overline{\Delta N^*}}{\delta \Delta N_t} \pm \frac{1}{\mu} \frac{\delta \mu}{\delta \Delta N_t}\right) \delta \Delta N_t \tag{3.5.2}$$

Considering that:

$$\overline{\Delta N^*} = N^* \mathbf{W} \Delta \mathbf{x} \tag{3.5.3}$$

and that:

$$\Delta N_t = N_t \mathbf{W} \Delta \mathbf{x} \tag{3.5.4}$$

Taking into account that the sign inside the round brackets in Eq. (3.5.2) depends on the charge of defects (neutral or charged traps), that $\frac{\delta \overline{\Delta N^*}}{\delta \Delta N_t}$ is equal to about 1 in a strong inversion regime [257], the $\frac{\delta \mu}{\delta \Delta N_t}$ can be obtained as [258]:

$$\frac{\delta \mu}{\delta \Delta N_t} = -\frac{\alpha^\circ \mu^2}{\mathbf{W} \Delta \mathbf{x}} \tag{3.5.5}$$

$\alpha^\circ$ is the scattering coefficient related to the unified model, Eq. (3.5.2) becomes:

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{N^*} \pm \alpha^\circ \mu\right) \frac{\delta \Delta N_t}{\mathbf{W} \Delta \mathbf{x}} \tag{3.5.6}$$

From Eq. (3.2.8), the associated normalized current spectrum becomes equal to:

$$\frac{S_I}{{I_{ds}}^2} = \frac{\lambda^* KT}{q f} \left(\frac{1 \pm \alpha^\circ \mu N^*}{\overline{\Delta N^*}}\right) N_t(E_F) \tag{3.5.7}$$

## 3.6 Modeling of flicker noise with stochastic processes AR and MA

In the previous chapters, it has been explained that the currents and voltages in the power MOSFETs can be subjected to flicker noises from two main sources. Flicker noises can be mathematically modeled in different ways. In particular, Granger in 1980 was the first to demonstrate that flicker noises are stochastic processes that have a long memory and can be obtained by aggregating an infinite number of autoregressive stochastic processes, AR [259]. Subsequently, the same Granger et al. in 1996 demonstrated that this can happen by adding a finite number of AR processes [260]. First, it is necessary to define exactly a stochastic process. A stochastic process, also called random process, can be described as a series of random events that cannot be assessed exactly at the beginning. Each event can be estimated with statistical methods based on a certain margin of error. For example, a random vector of indefinite length is a stochastic process. This random vector could describe a physical phenomenon through the values assumed by each experimental observation over time. Every observation of the experiment can be characterized as a random variable that takes values contained in a continuous or discrete interval. Typically, a physical phenomenon is studied in a predetermined period of time, thus, the results achieved from the observations represent a sample of the whole set of observable values. Therefore, we speak of statistical inference when it is possible to obtain information on the moments of the entire population from a sample. In a time series, each observation is obtained experimentally from an ordered time sequence of events where each of them could also depends on the immediately preceding events. As mentioned above, this behaviour is called persistence. Therefore, the noises observed in the currents or voltages of power MOSFETs sampled in a discrete number of time periods can be also considered a time series. So, given a time sequence of events characterized by a sequence of random variables, $x_{t-1}$, $x_t$, $x_{t+1}$,…, for each of them it is possible to associate a PDF, $f(x_{t-1})$, $f(x_t)$, $f(x_{t+1})$,….Then, given two different time instants, t and t-1, the function $f(x_t, x_{t-1})$ is called marginal probability. In general, the marginal probability associated with many random variables, f(…, $x_{t-1}$, $x_t$, $x_{t+1}$,…), is different from the product of the individual PDFs, … $f(x_{t-1})$ $f(x_t)$ $f(x_{t+1})$… if the stochastic process has a persistence. However, for each random variable, $x_t$, it is possible to derive the expected value or the average value, $E(x_t)$, the variance, $V(x_t)$, and the autocovariance, Cov ($x_t$, $x_{t-p}$) (in this case the autocovariance is of order p). These parameters are called moments of the random variable. When a stochastic process shows a persistence, the autocovariances are nonzero. A stochastic process is called stationary when the moments associated with the process are independent of time. However, a stochastic process can be strong stationary or weak stationary. In a strong stationary stochastic process, each subset process of the main process containing any number of events is independent of time. Instead, in a weak stationary stochastic process only the subset processes of the main process containing at most two events are independent of time. In weak stationary stochastic processes, the first and second moments, in practice, the average value, the variance and the autocovariances of different order are invariant over time. When a weak stationary stochastic process has a Gaussian shape it is also a strong stationary process. When a stochastic process has a weak persistence it is called ergodic. In fact, it is possible to obtain:

$$\lim_{n\to\infty} \frac{1}{n} \sum_{k=1}^{n} \mathrm{Cov}(x_t, x_{t-k}) = 0 \tag{3.6.1}$$

Given a long time series which describes a stationary and ergodic stochastic process, all the moments of the process can be estimated because this series is equivalent to a statistical inference carried out on many different samples. White noise is a stationary stochastic process but it is not ergodic because it does not manifest persistence.

In a white noise the expected value and the autocorrelations are equal to zero while the variance remains constant over time. The autocorrelations are derived from the ratio between the autocovariances and the variance of a stochastic process. A correlogram is a bar chart of the autocorrelation values of the process sorted according to the delay over time (see figure 3.6.1 in which an example of a correlogram of an ergodic stochastic process is shown). An ergodic stochastic process, $x_t$, can be estimated as:

$$x_t = x_t'\beta^+ + \varepsilon_t \tag{3.6.2}$$

$\beta^+$ is a vector of linear coefficients, $x_t'$ is the transposed vector of the random variables ordered over time and $\varepsilon_t$ is the random error. The random error is a stochastic process similar to a white noise. The linear coefficients are not known and can be estimated using the Ordinary Least Squares technique, OLS, by means of the autocorrelation values such as (Yule-Walker equations):

$$\begin{bmatrix}\beta_1\\ \vdots\\ \beta_n\end{bmatrix} = \begin{bmatrix}1 & \cdots & \rho_n\\ \vdots & \ddots & \dots\\ \rho_n & \dots & 1\end{bmatrix}^{-1}\begin{bmatrix}\rho_1\\ \vdots\\ \rho_n\end{bmatrix} \tag{3.6.3}$$

ρ are the autocorrelation values. Stochastic processes that have variance that varies over time are called heteroskedastic.

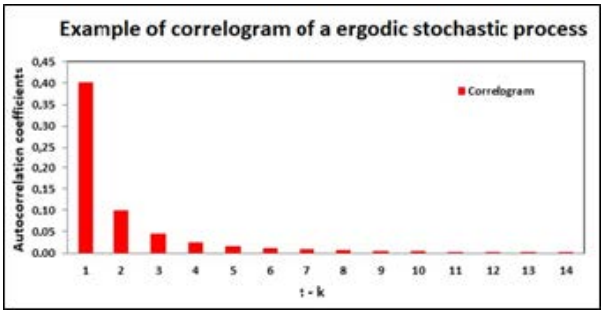



**Figure 3.6.1: Example of correlogram of an ergodic stochastic process.**

## 3.6.1 MA stochastic processes

A stochastic process of the MA type, or stochastic process with moving average, is obtained from a linear combination of stochastic processes of the white noise type such as:

$$x_t = \sum_{i=0}^{q} \theta_i \varepsilon_{t-i} \quad (3.6.1.1)$$

$\vartheta_i$ are the linear coefficients related to the stochastic process MA. The expected value of stochastic processes MA is equal to zero:

$$E(x_t) = E\left(\sum_{i=0}^{q} \theta_i \varepsilon_{t-i}\right) = \sum_{i=0}^{q} \theta_i E(\varepsilon_{t-i}) = 0 \quad (3.6.1.2)$$

Therefore, it is possible to assume that this mathematical model has limited applications. However, any stochastic process can be transformed into an average zero stochastic process such as:

$$x_t = x_t - E(x_t) \quad (3.6.1.3)$$

Furthermore, the Word theorem states that any stationary and zero-mean stochastic process can be derived from Eq. (3.6.1.1). The MA stochastic process variance is equal to:

$$E({x_t}^2) = E\left[\left(\sum_{i=0}^{q} \theta_i \varepsilon_{t-i}\right)^2\right] = E\left(\sum_{i=0}^{q} {\theta_i}^2 {\varepsilon_{t-i}}^2\right) + E\left(\sum_{i=0}^{q} \sum_{i \neq j} \theta_i \theta_j \varepsilon_{t-i} \varepsilon_{t-j}\right) = \boldsymbol{\sigma}^2 \sum_{i=0}^{q} {\theta_i}^2 \quad (3.6.1.4)$$

$\boldsymbol{\sigma^2}$ is the variance of the stochastic process. Instead, the autocovariances can be obtained as:

$$\mathrm{Cov}(x_t x_{t+k}) = E\left[\left(\sum_{i=0}^{q} \theta_i \varepsilon_{t-i}\right)\left(\sum_{j=0}^{q} \theta_i \varepsilon_{t-j+k}\right)\right] = \boldsymbol{\sigma}^2 \sum_{i=0}^{q} \theta_i \theta_{i+k} \quad (3.6.1.5)$$

taking into account that for $j \neq i + k$, $E\left(\varepsilon_{t-j+k} \varepsilon_{t-i}\right) = 0$ and $\theta_i = 0$ for $i > q$, thus, the persistence of a MA stochastic process becomes more marked by increasing its order.

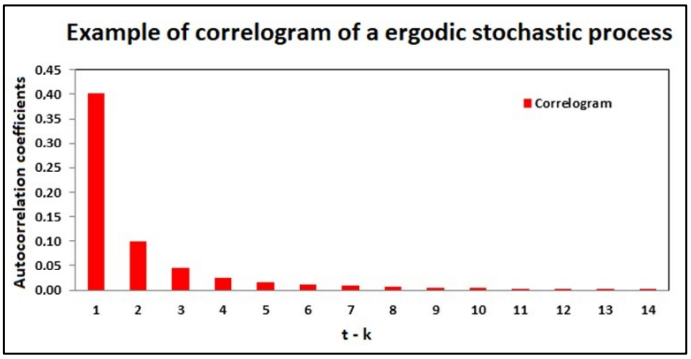



**Figure 3.6.1: Example of correlogram of an ergodic stochastic process.**

## 3.6.2 AR stochastic processes

The autoregressive processes, AR, have already been introduced in a compact form in Eq. (3.6.2). They can also be written as:

$$x_t + \beta_1^+ x_{t-1} + \cdots + \beta_n^+ x_{t-n} = \varepsilon_t \qquad (3.6.2.1)$$

Introducing the lag operator L equal

to: $$L^n x_t = x_{t-n} \qquad (3.6.2.2)$$

Eq. (3.6.2.1) becomes:

$$x_t(1 + \beta_1^+ L + \cdots + \beta_n^+ L^n) = x_t(1 + \beta^+ \mathbf{L}) = A(\mathbf{L}) x_t = \varepsilon_t \qquad (3.6.2.3)$$

**L** is the vector $[L^1 \ldots L^n]$ and A(**L**) is the characteristic polynomial. In the case of $|\beta^+|<1$, it is possible to obtain:

$$x_t = [1 + \alpha \mathbf{L}]^{-1} \varepsilon_t = [1 + \alpha L + \cdots \alpha^n L^n] \varepsilon_t = \sum_{i=0}^{n} \alpha^i L^i \varepsilon_t = A(\mathbf{L})^{-1} \varepsilon_t \qquad (3.6.2.4)$$

Therefore, AR processes can be derived from the linear combination of white noise processes as in the case of MA processes. For the process to be stationary, the root of A(**L**) must be greater than 1 in absolute values. Given a AR process of first order, AR(1), it is possible to obtain:

$$x_t = \beta^+ x_{t-1} + \varepsilon_t \qquad (3.6.2.5)$$

The expected value of Eq. (3.6.2.5) is equal to:

and: $$E(x_t) = \beta^+ E(x_{t-1}) \qquad (3.6.2.6)$$

The Eq. (3.6.2.6) is true in the case of a zero-mean stationary stochastic process or if $\beta^+$ is equal to 1. However, as already mentioned for MA stochastic processes, any stochastic process can be transformed into a stochastic process with zero-mean as seen in Eq. (3.6.1.3). The variance of a stochastic process AR(1) can be obtained as:

$$V = E(x_t^2) = E(\beta^+ x_{t-1} + \varepsilon_t)^2 = \beta^{+2} E(x_{t-1}) + 2E(\beta^+ x_{t-1} \varepsilon_t) + E(\varepsilon_t^2) = \beta^{+2} V + \boldsymbol{\sigma}^2 \qquad (3.6.2.7)$$

$$V = \frac{\boldsymbol{\sigma}^2}{1-\beta^+} \qquad (3.6.2.8)$$

As can be seen in Eq. (3.6.2.8), when $\beta^+$ approaches 1, the variance becomes infinitely big. The autocovariance of a AR(1) process can be achieved by:

$$Cov(x_t x_{t-1}) = E(x_t x_{t-1}) = E[(\beta^+ x_{t-1} + \varepsilon_t)\, x_{t-1}] = \beta^+ E(x_{t-1}^2) + E(\varepsilon_t\, x_{t-1}) = \beta^+ V \qquad (3.6.2.9)$$

## 3.7 Entropy and approximate entropy of stochastic processes

In the previous chapter it was said that the noises observed in the currents and voltages of power MOSFETs are stochastic processes and can be studied both using PSD (in the frequency domain) and through the MA and AR processes (linear stochastic processes obtained by sum of white noises) in the domain of time. In the last chapter it was also said that, in time domain, noises can be described by discrete data time series in which each ordered event represents a sample of the random variable that describes the phenomenon. However, sometime it is necessary to make a summary of the information contained in the stochastic process in a few parameters that contain the relevant characteristics of the phenomenon under investigation. A stochastic process can be studied by carrying out two different types of measures on the parameters: linear and nonlinear. Typical linear measures are the expected value and variance of a stochastic process. The latter do not depend on the ordering of the data, thus, they do not provide information on the time evolution of the phenomenon. As already mentioned, it is possible to obtain information on the time evolution of stochastic processes by studying the autocorrelations of the time series. In the case of non-linear parameters, noises are classified according to their complexity and irregularity. An example of non-linear parameter is the approximate entropy introduced by Pincus in 1991 [261]. In particular, non-linear parameters are used to characterize a stochastic process when it is assumed that the signal is influenced by a deterministic chaotic dynamic that cannot be effectively quantified by traditional linear parameters. A deterministic chaotic system is a particular deterministic system in which the two trajectories of a point in the space, position and velocity, depend strongly on the initial conditions. Indeed, deterministic chaotic systems are not purely stochastic processes because they can be modeled by non-linear mathematical equations even if their behaviour appears unpredictable. Therefore, given a time series of a noise signal, it is possible to obtain the entropy of the process by knowing the PDF of each random variable and the probability of transition between two adjacent variables [262]. The term entropy is associated with the concept of disorder. In fact, entropy measures the randomness of the signal and its value increases by increasing the disorder of the system. In the deterministic processes the trajectories are exactly described by mathematical equations, thus, entropy is zero. Instead, in a deterministic chaotic system entropy increases assuming finite positive values. In purely stochastic processes, entropy takes on very high values. In a stochastic process supposed as a source that emits symbols from an alphabet to form strings from a certain length, $s_i$, Shannon defined entropy as:

$$H = -\sum_{i=1}^{b} P(s_i) \ln[P(s_i)] \tag{3.7.1}$$

$P(s_i)$ is the probability associated with the string $s_i$. Entropy has three basic properties [8]. The first states that H is equal to zero if and only if the probability associated with an element of the alphabet is equal to 1 and the others are equal to zero assuming that $h(s_i) = P(s_i)\ln[P(s_i)]$ is equal to zero when $P(s_i)$ is equal to zero. The second states that $h(s_i)$ is a continuous, non-negative and concave function in the range of (0,1]. The maximum value of entropy H is reached when each element of the alphabet has the same probability of being emitted:

$$H = \ln(b) \tag{3.7.2}$$

Finally, the third property states that if an event associated with the string is independent of the others then it is obtained that:

$$\ln[P(s_1, s_2, \dots, s_n)] = \ln[\prod_{i=1}^{n} P(s_i)] = \sum_{i=1}^{n} \ln[P(s_i)] \tag{3.7.3}$$

Given a string of elements, it is possible that the signal shows a persistence, thus, in this case, it is appropriate to consider the conjunct entropy associated with the ordered sequence of symbols such as:

$$H_n = -\sum_{S:|S|=n} P(s)\ln[P(s)] \tag{3.7.4}$$

If the length of the string is equal to 2, the conjunct entropy becomes:

$$H_2 = H(E_1) + H(E_2|E_1) \tag{3.7.5}$$

$H(E_1)$ is the entropy of the first event and $H(E_2|E_1)$ is the conditional entropy or entropy of the second event known the result of the first event. However, $H(E_2|E_1)$ is always not greater than $H(E_2)$, thus:

$$H_2 \leq H(E_1) + H(E_2) \tag{3.7.6}$$

and extending the result obtained in Eq.(3.7.6) to an indefinite string of n elements, it is possible to obtain:

$$H_n \leq H(E_1) + \ldots + H(E_n) \tag{3.7.7}$$

Therefore, if the stochastic process is persistent, its entropy is less than that of a purely random process. Kolmogorov introduced the concept of metric entropy for a stochastic process with strings of length n [8]:

$$K_1 = \lim_{n\to\infty} \frac{H_n}{n} \tag{3.7.8}$$

Given Eq.(3.7.2) and Eq.(3.7.6), in the case of a stationary source, it is possible to obtain that:

$$0 \leq K_1 \leq \ln(b) \tag{3.7.9}$$

and:

$$K_1 = \lim_{n\to\infty} (H_n - H_{n-1}) \tag{3.7.10}$$

The metric entropy proposed by Kolmogorov can be easily applied when the conjunct probabilities associated with the string of symbols are known, otherwise, the metric entropy must be estimated on the basis on the results obtained from the experiments. Eckmann and Ruelle proposed an algorithm to estimate the metric entropy of a stochastic process given by a time series [78] based on a previous algorithm introduced by Grassberger and Procaccia in 1983 [179]. The Eckmann and Ruelle algorithm, E-R, considers a time series of events, {u(1),…,u(n)}, acquired in a constant time interval, Δt. Given the numbers $m^{\#}$, an integer, and r, a real, we construct the vectors z(1),…,z(N-$m^{\#}$+1) in the set $R^m$ as described below:

$$z(i) = [u(i), \ldots, u(i + m^{\#} - 1)\ ] \tag{3.7.11}$$

with 1 ≤ i ≤ N-m+1. It is now possible to introduce the Takens distance defined as [185]:

$$d[z(i), z(j)] = \max_{k=1,\ldots,m} |u(i + k - 1) - u(j + k - 1)| \tag{3.7.12}$$

Given the number, ϑ, of vectors z defined as d[z(i),z(j)] ≤ r, it is possible to introduce a new number:

$$C_i^{m^{\#}}(r) = \frac{\vartheta}{n-m+1} \tag{3.7.13}$$

This number measures how many times similar vectors of m elements have been observed with respect to a given vector in an interval r. By introducing a new parameter:

$$\Phi^{m^{\#}}(r) = \frac{\sum_{i=1}^{n-m^{\#}+1} \ln\left[C_i^{m^{\#}}(r)\right]}{n-m^{\#}+1} \tag{3.7.14}$$

The metric entropy of E-R becomes equal to:

$$K_{E-R} = \lim_{r\to 0} \lim_{m^{\#}\to+\infty} \lim_{n\to+\infty} \left[\Phi^{m^{\#}}(r) - \Phi^{m^{\#}+1}(r)\right] \tag{3.7.15}$$

However, the entropy of E-R is calculated for a very large number of elements, thus, Pincus has introduced a new metric entropy called approximated entropy of the time series defined as:

$$ApEn(m^{\#}, r, n) = \Phi^{m^{\#}}(r) - \Phi^{m^{\#}+1}(r) \tag{3.7.16}$$

with n which can also be quite small. In stochastic deterministic processes, the approximated entropy is close to zero while, for the most complicated and unpredictable systems, the approximated entropy grows up to high values. However, approximated entropy can be considered as a measure of regularity of time series rather than an approximation of E-R entropy. In any case, for a very large number of elements n, a fairly large $m^{\#}$, and an optimize value of r, the two parameters tend to approach.

# 4 Defectiveness characterization of the oxide-substrate interface in SiC power MOSFETs

## 4.1 Description of the experimental analyses performed on some SiC power MOSFETs samples to characterize the oxide-substrate interface

In this chapter the analysis techniques will be described and all the experimental results performed on some samples of two different families of the standard VDMOS 4H-SiC power MOSFETs (see the topology in figure 2.1.4) will be shown in order to characterize exactly the interface region between the oxide and the substrate to evaluate the reliability of the devices. Both families of SiC power MOSFETs under test (type A family and type B family) belong to the same manufacturer and the difference between them consists only in the die size (type A devices should be approximately 10% larger than type B devices) because all the other design parameters have remained unchanged. The critical dimensions of the devices under test provided by the manufacturer's design rules are not known but, in any case, purely by way of example, it is possible to assume that they are approximately the same as those which can usually be obtained, typically, from the literature. In fact, it is possible to assume that the thickness of the gate oxide could be equal to about 80nm and, thus, the oxide capacitance per unit area could be equal to about $1.32x10^{-3}$ $Fm^{-2}$. For example purposes only, It is also possible to assume that the length of each cell in the periodic arrangement of the VDMOS structure (defined as cell pitch) could be equal to about 5µm and that the channel length could be equal to about 0.5µm. Therefore, the channel region could be equal to about 20% of the entire cell pitch. It is also possible assume that the edge region of the high voltage power MOSFETs should be approximately 30% of the entire die surface. This region should definitely contain special metal plates and other design solutions and is designed to prevent the crowding of the electric field lines to withstand high drain-source voltages (see chapter 2.1). Therefore, the active area of the device should be approximately 30% smaller than the die surface. The effective surface of the die involved in the conduction process is equal to the product between the length of the channel and the perimeter of the device. Therefore, considering that the channel region should be equal to about 20% of the cell pitch, the perimeter of the device can be estimated by dividing 20% of the active area by the length of the channel. The main electrical characteristics obtained by the manufacturer's datasheets are summarize in Tab. 5.1 for both families of SiC power MOSFETs under test. Furthermore, purely as an example, although this may not be true, considering information that can usually be obtained from the literature, it is possible to assume that type A devices have a die size of about 16 $mm^2$ while type B devices have a die size of about 14.5 $mm^2$. The maximum guaranteed temperature for both types of devices is fixed at 200°C.

Tab. 4.1: Main electrical characteristics of type A and type B devices.

| Family | type | $BV_{ds}$[KV] | $I_{Dsmax@25°C}$[A] | $R_{DSON@20A,25°C}$[mΩ] | $V_{th@1mA,25°C}$[V] | $C_{ISS@50mV,25°C}$[nC] | Package | technology | Qt. |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
| Type A | n-ch | 1.2 | 65 | 52 | 3 | 3.5 | HiP247 | Planar | 8 |
| Type B | n-ch | 1.2 | 45 | 80 | 3.5 | 2.5 | HiP247 | Planar | 4 |

The analyses that were performed on the these devices to characterize the defectiveness of the interface region and, thus, their reliability level were the threshold-voltage instability measurements, the PBTI and the Low frequency noise analysis. With reference to the threshold-voltage instability measurements and the PBTI analyses, the behaviour of the devices under test was simulated with suitable TCAD tool in order to extrapolate the $D_{it}$ profile as a function of the energy within the SiC bandgap. To complete the characterisation study, further experimental analyses on the physical nature of the interface performed on devices of the same families mentioned above were extrapolated from the works of P. Fiorenza et al. These analyses concerns both the characterization of the transition layer in the interface region implemented with the EELS (Electron Energy Loss Spectroscopy) technique and the characterization of the gate current to understand the conduction mechanism within the dielectric. These analyses were carried out in the framework of European project WInSiC4AP (Wide Band Gap Innovative SiC for Advanced Power). Before introducing the chapters of the experimental analyses, it is important to underline again that, according to the Deal Committee formulation for silicon MOSFETs [263], charges to the interface and within the gate oxide can be categorized as interface traps, oxide traps, fixed charges and mobile ions (see figure 4.1.1). This same convention can be also successfully applied to SiC power MOSFETs. In silicon MOSFETs, fixed charges are found in the first 25 Å inside the dielectric away from the interface [263]. These charges are not electrically connected with the substrate. Fixed charges also exist in SiC power MOSFETs, but their physical nature is different as explained in chapter 2.2.5. It is possible to define extrinsic threshold voltage instability when this phenomenon depends on the mobile charges due to ionic contaminations such as sodium or potassium which could enter the gate oxide during the manufacture of the device. Neglecting for our purpose the oxide charges and the mobile charges, both the threshold-voltage instability and the PBTI depend on the interface and the oxide traps and, thus, it is possible to define this phenomenon as an intrinsic threshold voltage instability. As will be better shown later, the threshold-voltage instability phenomenon is mainly due to the interface traps even if it also depends on the oxide traps which are close enough to the interface so that they can exchange charges with the inversion layer present in the device channel. In particular, as will be shown later, the relaxion time constants of the oxide traps are larger than those relating to the interface traps, thus, this could cause a permanent drift of the threshold voltage of the device during normal operation in application. Therefore, the short-term effects of the threshold voltage instability can be mainly due to interface traps while the long-term effects can be mainly due to oxide traps. These defects can be separated from each other mainly by the response time as function of the voltage applied to the gate. However, sometime, the distinction between interface traps and oxide traps is not that sharp. In fact, oxide traps with very shallow energy barriers behave like the interface traps. It is important to underline that, interface traps can be described as point defects in the interface that are located energetically within the semiconductor bandgap and that can exchange carriers with the substrate according to the Shockley-Read-Hall (SRH) theory (see figure 4.1.2). Instead, the oxide traps exchange charges with the substrate with an inelastic tunneling process, see figure 4.1.3, triggered not only by the position of the Fermi level in the semiconductor but also by a thermodynamic energy barrier (see chapter 3.2). Typically, interface traps cause fully reversible threshold voltage variations while oxide traps are most likely responsible for more permanent drift.

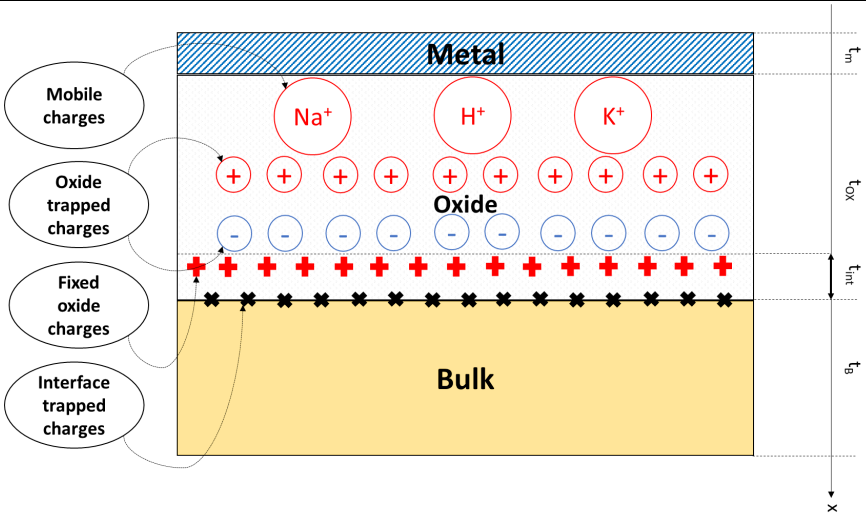



**Figure 4.1.1: Representation and localization of the traps onside the oxide in the MOS structure.**

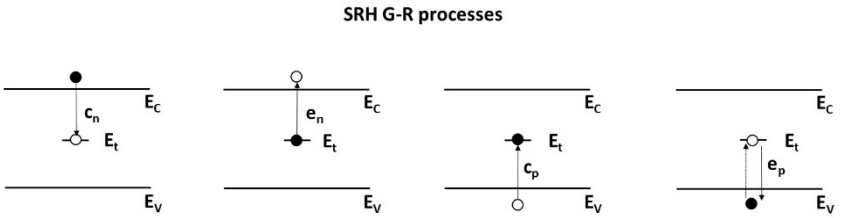



**Figure 4.1.2: SRH processes for deep-level traps: a) electron capture process; b)electron release process; c) hole capture process; d) hole release process.**

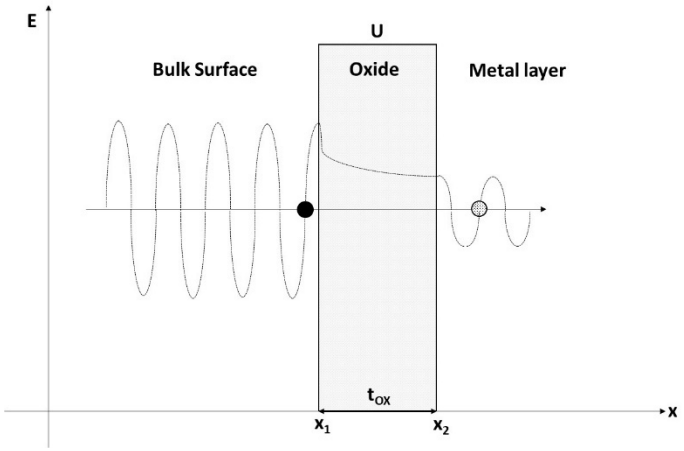



**Figure 4.1.3: Electron tunnelling effect through a rectangular energy barrier.**

Fully reversible threshold voltage variations occur when the number of carriers trapped and emitted during one gate voltage switching period remains constant even after billions of consecutive switching events [270]. When studying PBTI over time in SiC power MOSFETs, it is possible to assume that the phenomenon is strongly correlated to oxide traps. However, it is necessary better define the concept of oxide traps.

The oxide traps involved in the instability process in SiC power MOSFETs are those close to the interface region and are generally defined as compensated holes (not permanently annealed), thus, they are positively charged [198]. Over time, these oxide traps are called in many different ways such as, for example, slow states, Anomalous Positive Charge (APC) and, in particular, border traps. In the past, two different models of oxide defects attributed to permanent annealing and charge switching phenomena have been classified even if this distinction is not clear [265]. Permanent annealing phenomenon is due to the traditional hole traps which anneal but do not switch while the charge switching behaviour is due to traps which switch but do not anneal and are associated with APC defects. Traps with a permanent annealing phenomenon can be interpreted as defects in which it is possible to reform the broken bonds between the atoms of the reticule. Hole traps can be annealed on an approximately logarithmic time scale even at room temperature due to a tunneling mechanism. The shape of the response curve depends on the specific spatial and energetic distribution of trapped holes within the oxide [266]. In fact, electron tunneling into the oxide from the substrate can eliminate the positive charge. However, if a hole is only compensated by an electron, the process is reversible and the defect behaves like a switching oxide trap. First, electrons have to tunnel into the oxide before they can tunnel back out. Therefore, the charges move towards and from the oxide traps according to the voltage variation applied in the gate terminal. These switching behaviour of the traps are attributed to APC defects [267], [268]. Therefore, APC defects have been described simply as positive charge centers near the interface that exchanges charges with the substrate and often they are called border traps as proposed by Fleetwood [269]. This is the typical phenomenon observed in the experimental results that will be shown in the next chapters. However, a switching oxide trap can be defined as border trap if it responds to the applied signal. Indeed, for example, if the signal transient is too fast it could be that the trap does not respond and, thus, it will be called only as a switching oxide trap instead of border trap. The low frequency noise analysis is a suitable characterisation tool that allow us to understand if the interface traps and, in particular, the border traps affect the noise observed in the currents and voltages of power MOSFETs due to the variation in the number of carriers involved in the flow of current in the channel, thus, it can be explained by the McWhorter model, or because of the fluctuation of the mobility of the carriers explained by the Hooge model or if both phenomena explain the noise (Unified model for flicker noise).

## 4.2 Threshold-Voltage Instability Measurements in SiC power MOSFETs

The Threshold-Voltage Instability Measurements carried out on both families of SiC power MOSFET devices were focused on the experimental study of the $I_{DS}$-$V_{GS}$ transfer characteristic hysteresis. All tests were carried out at ambient temperature set at around to 20˚C. The electrical characterization has been performed by means of the Keithley 4200 Semiconductor Characterization System (4200-SCS), equipped with a high power source-measure-units (SMUs), the ultra-fast I–V module of pulse-measure-unit (PMU) and the text fixture for packaged devices. The 4200-SCS is a fully automated system that performs I-V, pulsed I-V and C-V characterization of semiconductor devices. Tests can be easily and quickly configured and executed from the Keithley Interactive Test Environment (KITE). KITE is an application program designed and developed specifically for the characterization of semiconductor devices. The instrumentation is equipped with eight outputs to connect measurement units (SMU). The source of pulse and measurement signals is performed by the ultrafast IV card 4225-PMU. The 4200-SCS Interactive KTE software includes six tools to operate the machine. The Keithley Interactive Test Environment (KITE) is the main application for characterizing devices. The Keithley User Library Tool (KULT) allows test engineers to integrate custom algorithms (user modules) into KITE. KULT is used to create and manage user module libraries. All the components of the 4200-SCS can be controlled by user modules written in the C programming language. Keithley CONfiguration (KCON) allows test engineers to configure external modules to the machine via the GPIB interface, switch matrices and probes connected to the 4200-SCS. The KXCI interface allows to connect an external computer to control SMUs and cards to generate pulses remote control of the machine via the GPIB interface (IEEE-488) or Ethernet network. KPulse is the application of the virtual front panel of Keithley instruments that allows direct access to the functionality of the cards for generating the pulses. KScope is the Keithley Instruments virtual front panel application that allows direct access to the features of the 4200-SCP2 and 4200-SCP2HR modules. The basic units of the 4200-SCS are the SMU that measure currents after imposing voltages or, conversely, measure voltages after imposing currents. The SMUs used in the experiments conducted in this work are the 4200 which can manage a power up to 2W, withstand voltages up to 200V and carry currents up to 100mA.

The standard threshold-voltage instability measurements performed in these experiments is shown as in figure 4.2.1. Initially, the gate voltage was set to -5 V to reset device characteristics by removing the charges trapped in the interface. Subsequently, the gate voltage was increased from negative polarization to positive polarization in 50 mV increments and setting the $V_{DS}$ at 50 mV. Immediately afterwards, the gate voltage was decreased starting from the maximum positive value reached during the first phase down to -5 V in 50 mV decrements to determine the shift of the trans-characteristic (the readout is quasi-instantaneous after each increment that occurs about every 60 ms). Figure 4.2.2 shows the electric circuit used to perform the threshold voltage instability tests on the devices under test set the working temperature. The hysteresis measurements were obtained considering three different conditions by sweeping the $V_{GS}$ from -5 V up to the maximum voltages of 5 V, 10 V and 15 V. At first, the measurements were performed in DC quasi-static mode. Unless mobile ions are involved, applying a positive voltage to the gate will result in a positive shift in $V_{th}$. Conversely, applying a negative voltage to the gate will result in a negative shift in $V_{th}$. These effects can be explained by filling or emptying the near-interface oxide traps with electrons in response to the electric field.

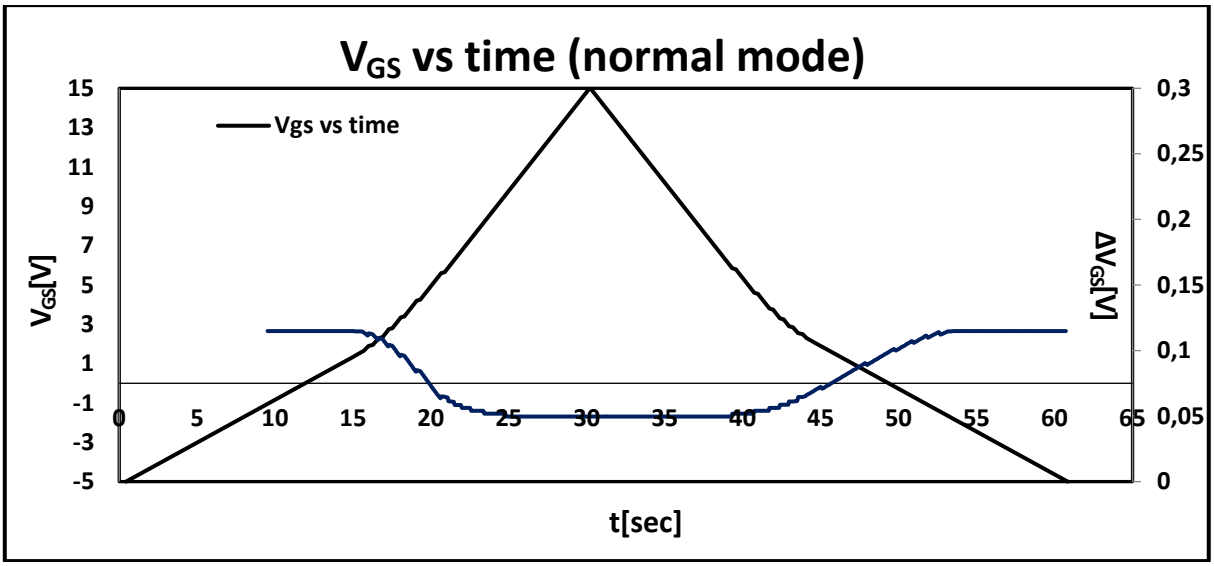



**Figure 4.2.1: $V_{GS}$ over time applied on the devices under test during the Threshold-Voltage Instability Measurements in quasi-static normal mode.**

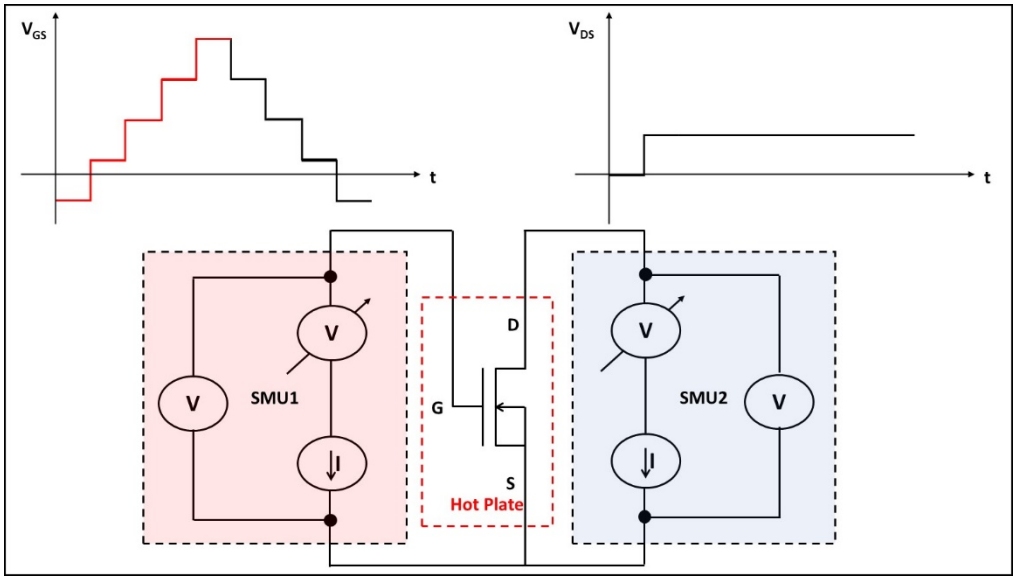



**Figure 4.2.2: Temperature dependent $V_{th}$ hysteresis measurement setup.**

The shift in the $V_{th}$ is particularly visible in the subthreshold regime, thus, it can be easily estimated by choosing a certain level of current in this condition. Above the value of $V_{th}$, the hysteresis slowly disappears and the drain current aligns with its typical value [271]. Therefore, the shift of the $V_{th}$ is obtained as the difference between the values of the $V_{th}$ estimated during the descending phase, $V_{th}^{down}$, and the ascending phase of the trans-characteristic, $V_{th}^{up}$. In this first work, the current value used to estimate the $V_{th}$ has been set to 100 µA. However, another method to accurately evaluate $V_{th}$ in power MOSFETs and which will be used later in the analysis of low frequency noise has been proposed by Williams [123]. In particular, in the Williams' method, $V_{th}$ is estimated from the graph of $g_{fs}$ as a function of $V_{GS}$. When the $g_{fs}$ starts to grow exponentially with the growth of the $V_{GS}$ then this point on the x axis is taken as $V_{th}$. By way of example, in figure 4.2.3, the typical instabilities that are observed in the $I_{DS}$–$V_{GS}$ characteristics measured in the piece number 1 of the type A power MOSFET are shown.

The transfer-characteristics for both the upward sweep and downward sweep of the three different working conditions are included in this graph: up to 5V, up to 10V and up to 15V. It is important to underline that the behaviour observed in the piece 1 of the type A power MOSFET tested is similar to the rest of the samples analysed. Figure 4.2.3 shows that the three characteristics of the $I_{DS}$-$V_{GS}$ overlap during the upward sweep, thus, confirming that the initial polarization of -5 V applied to the gate of the power MOSFET allows to release the charges previously trapped in the oxide. In figure 4.2.4, figure 4.2.5 and figure 4.2.6 are highlighted the trans-characteristics of the device which shows the phenomenon of hysteresis for $V_{GS}$ which reaches respectively up to 5V, 10V and 15V. In red are traced the trans-characteristics with the upwards sweep of the $V_{GS}$ while in black are traced those with the downwards sweep of the $V_{GS}$. Figure 4.2.7 shows the same graph as figure 4.2.3 but with the $I_{DS}$ plotted in a logarithmic scale. Figure 4.2.8, figure 4.2.9 and figure 4.2.10 show the phenomenon of hysteresis in the trans-characteristics of piece 1 of the type A of the power MOSFET under test with $I_{DS}$ in a logarithmic scale to highlight the $V_{th}$ shift between the upward sweep and the downward sweep of the $V_{GS}$ for the working conditions up to 5V, up to 10V and up to 15V. It is worth noting that applying gate voltages up to 15V the electric field of the oxide can reach up to about 2 $MVcm^{-1}$. As expected and explained in chapter 4.1, the application of a positive voltage in the gate terminal causes a positive shift of the threshold voltage in all operating conditions. Furthermore, it has been found that the $V_{th}$ instability increases by increasing the gate voltage. In fact, the higher the gate voltage, the more effectively the tunneling process occurs inside the oxide. Furthermore, the higher the gate voltage, the greater the number of interface traps swept within the SiC bandgap. In our example, the shift of the $V_{th}$ is 400 mV for testing up to 15 V of $V_{GS}$, 300 mV for testing up to 10 V of $V_{GS}$ and 150 mV for testing up to 5 V of $V_{GS}$. In a first approximation, the total number of traps per unit of area involved in the instability process of the threshold voltage can be calculated as:

$$N_t = \frac{C_{ox}}{q}\Delta V_{th} \tag{4.2.1}$$

Therefore, taking into account that the $C_{ox}$ is approximately equal to $1.32x10^{-3}$ $Fm^{-2}$, the number of traps involved in the $V_{th}$ instability process per unit of area is approximately equal to $3.3x10^{11}$ $cm^{-2}$ in case the $V_{GS}$ reaches 15 V, $2.5x10^{11}$ $cm^{-2}$ in case the $V_{GS}$ reaches 10 V and $1.2x10^{11}$ $cm^{-2}$ in case the $V_{GS}$ reaches 5V. By way of example, the same analysis performed on the piece 1 of the type A power MOSFET has been also performed on the piece 1 of the type B power MOSFET. The experimental results are shown from figure 4.2.11 to figure 4.2.18. Again, the behaviour observed in the piece 1 of the type B power MOSFET tested is similar to piece 1 of the type A power MOSFET and of the rest of the samples analysed of type B devices. In this new example, the shift of the $V_{th}$ is 500 mV for testing up to 15 V of $V_{GS}$, 350 mV for testing up to 10 V of $V_{GS}$ and 100 mV for testing up to 5 V of $V_{GS}$. Therefore, the number of traps involved in the $V_{th}$ instability process per unit of area is approximately equal to $4.1x10^{11}$ $cm^{-2}$ in case the $V_{GS}$ reaches 15 V, $2.9x10^{11}$ $cm^{-2}$ in case the $V_{GS}$ reaches 10 V and $0.8x10^{11}$ $cm^{-2}$ in case the $V_{GS}$ reaches 5V. In the comparison between piece 1 of type A device and piece 1 of type B device, it is important to highlight that the second shows a slightly higher level of defectiveness level than the first even if the value of the threshold voltage instability is lower considering the characteristic of $V_{GS}$ up to 5 V. The latter event occurs because the real value of the $V_{th}$ estimated by the Williams' method of the type B device is greater than of the type A device, as shown in figure 4.2.19 and figure 4.2.20 where is also highlighted the $g_{fs}$. From these last graphs it is possible to see that the $V_{th}$ measured during the ascending phase is equal to 2.7 V for the piece 1 of the type A device and 3.0 V for the piece 1 of the type B device to confirm the previous hypothesis. In these graphs, the $g_{fs}$ is obtained by dividing the increment in $I_{DS}$ by the increment in $V_{GS}$ and setting a certain current value.

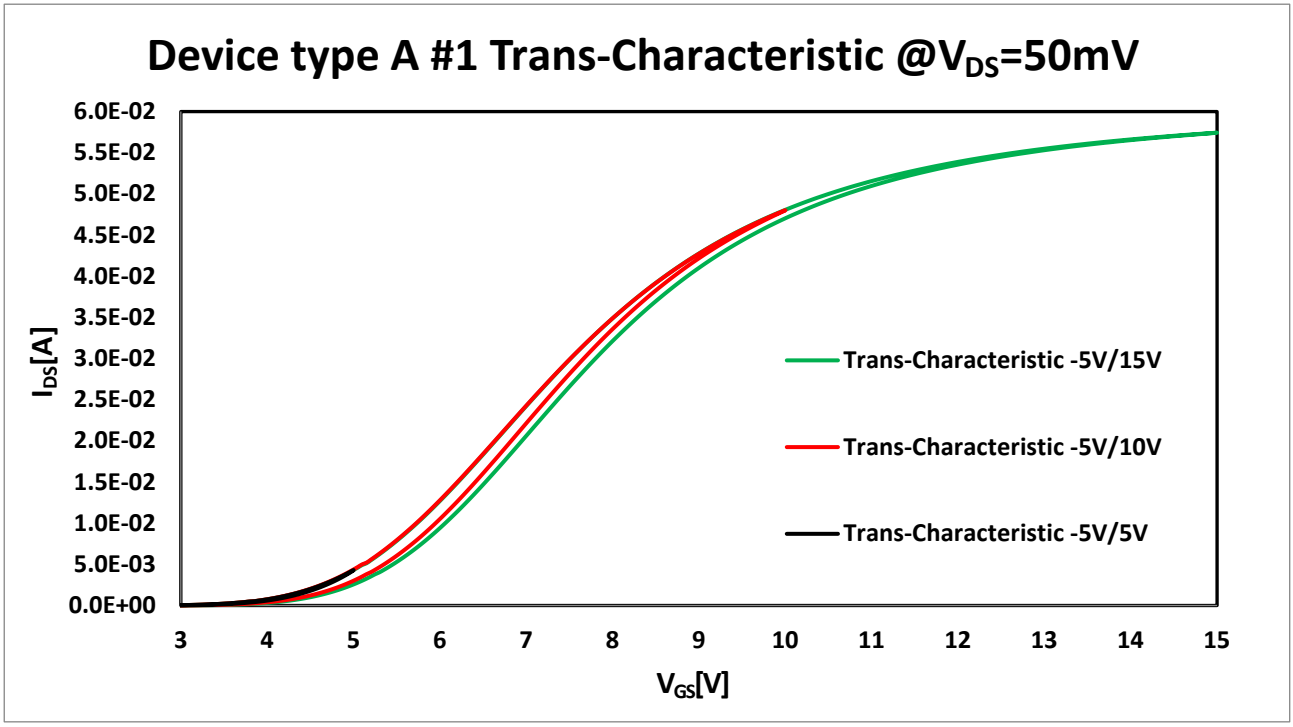



**Figure 4.2.3: Trans-characteristics of piece 1 of the type A power MOSFET which show the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V, 10V and 15V.**

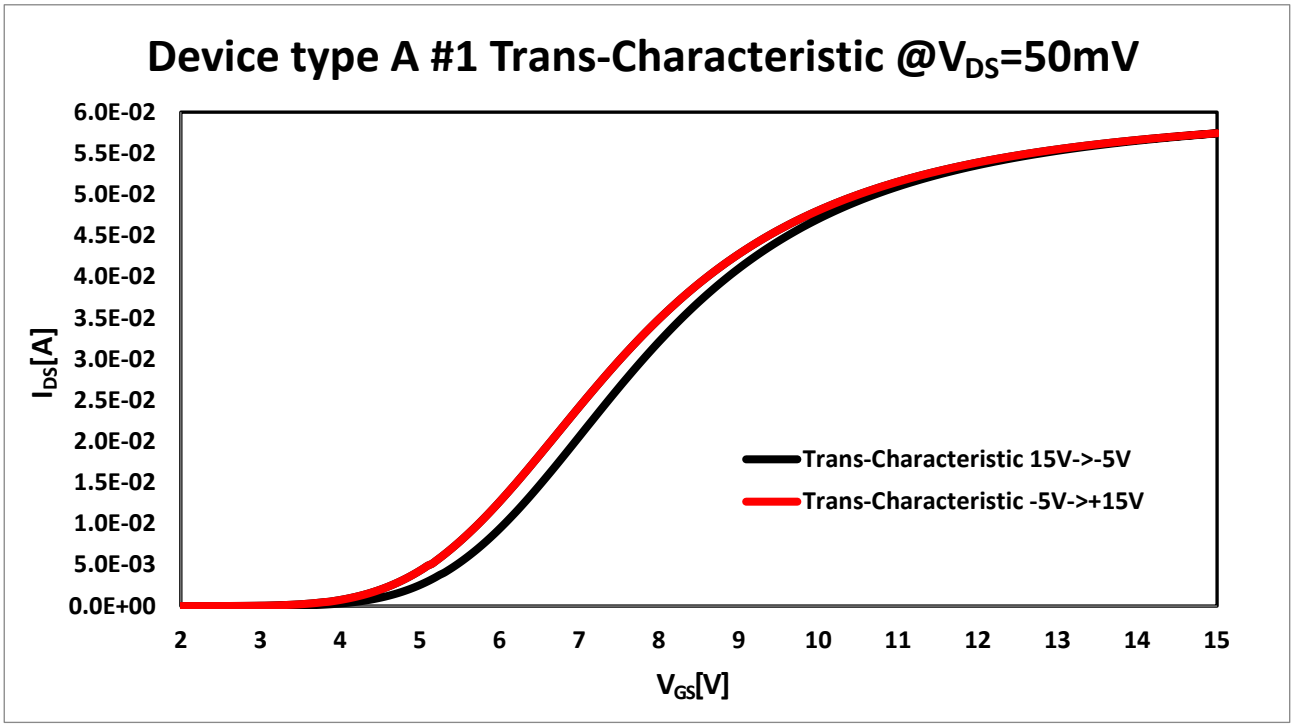



**Figure 4.2.4: Trans-characteristic of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 15V.**

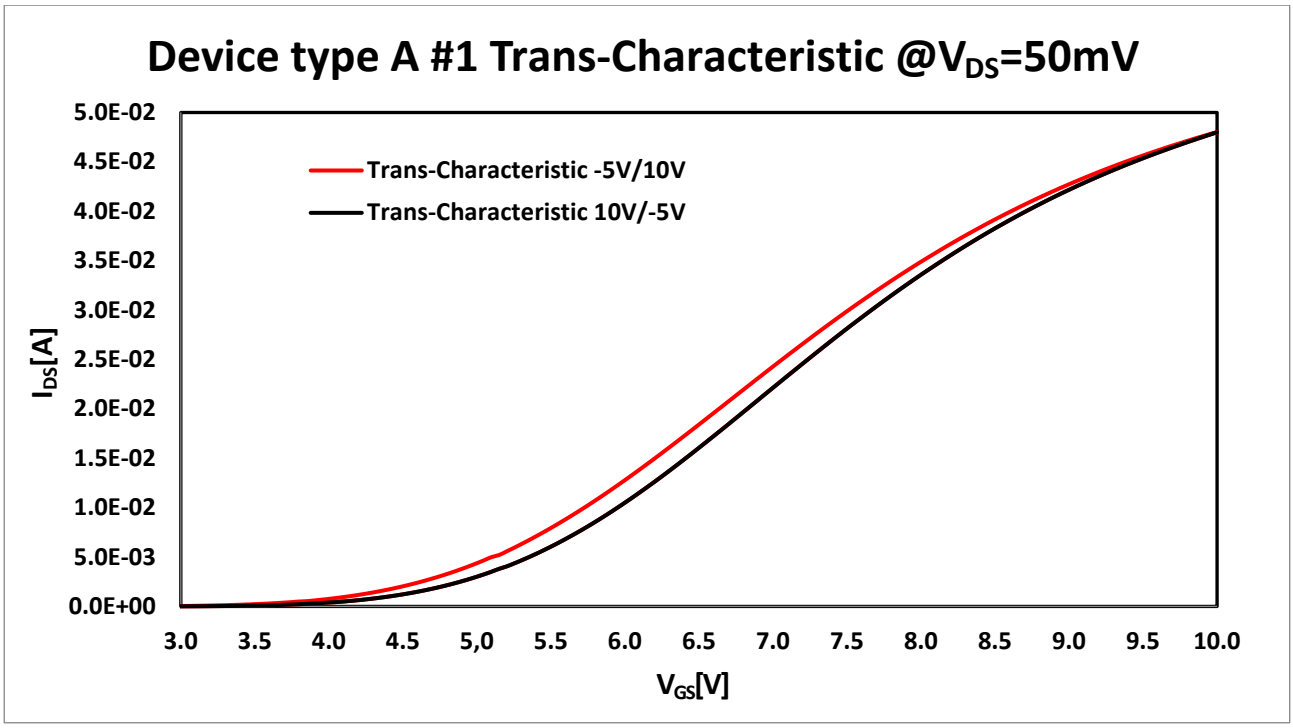



**Figure 4.2.5: Trans-characteristic of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 10V.**

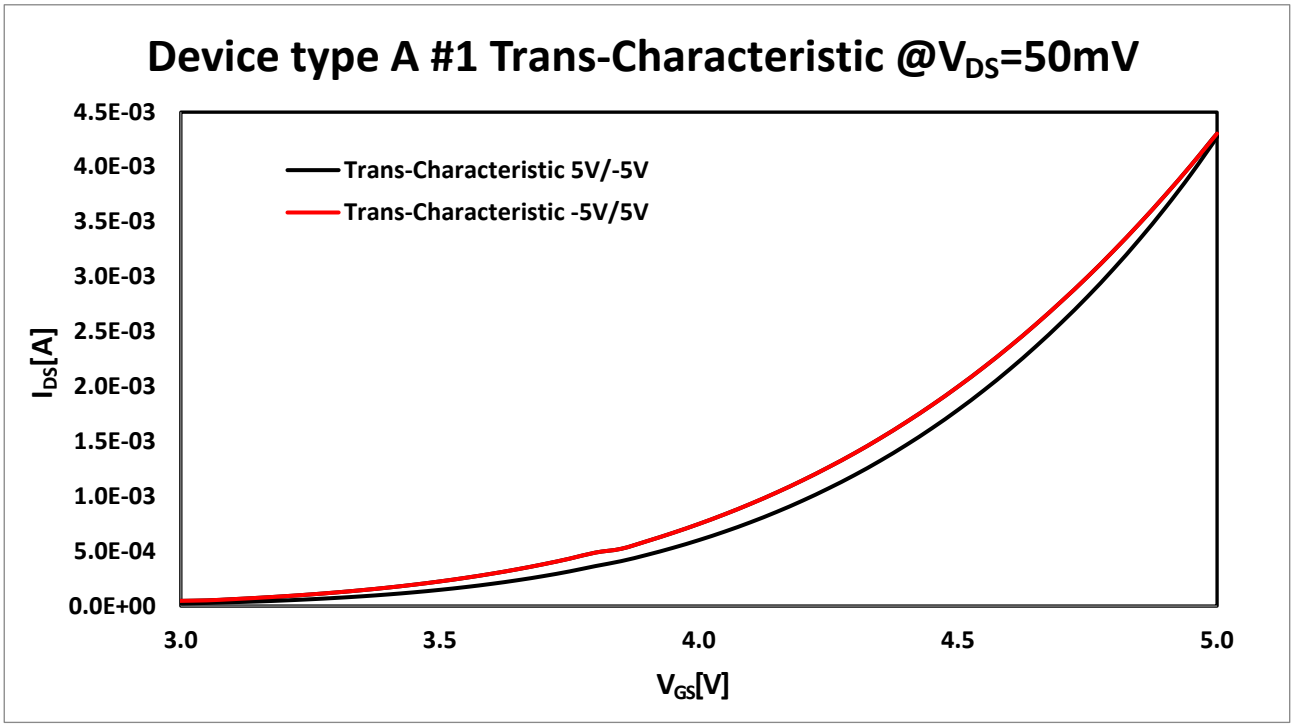



**Figure 4.2.6: Trans-characteristic of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V.**

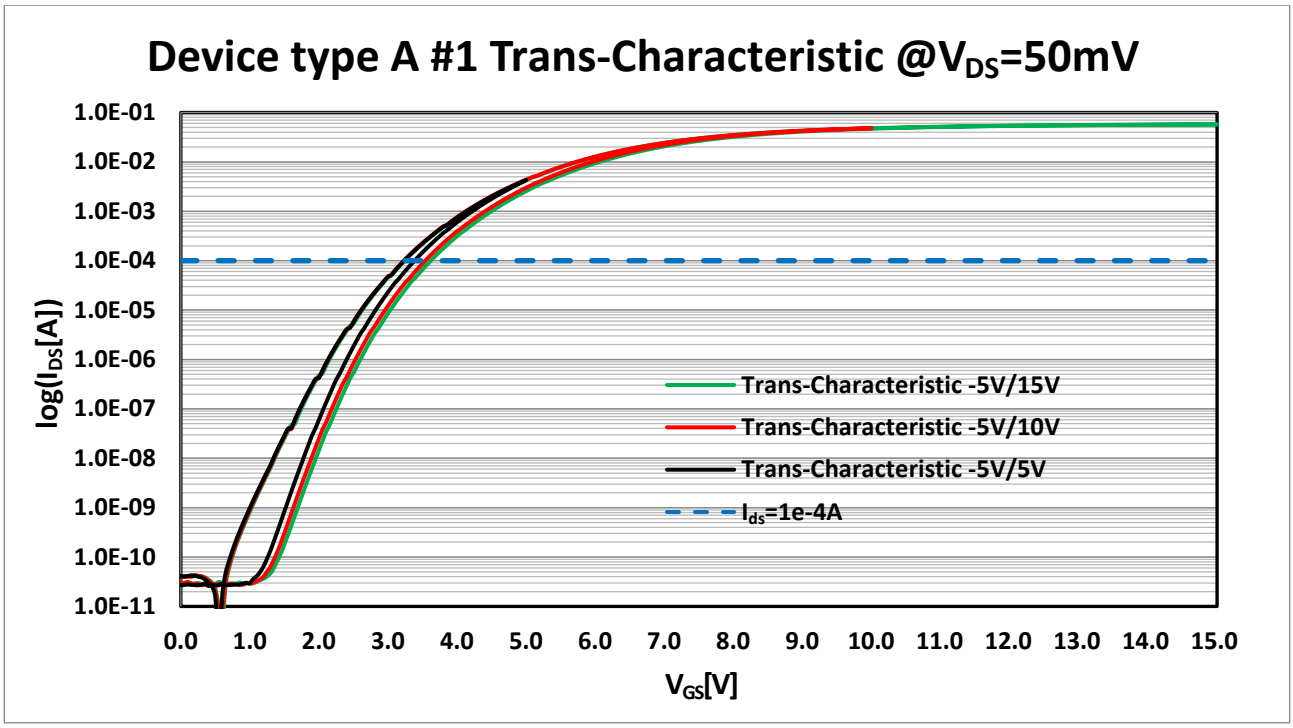



**Figure 4.2.7: Trans-characteristic in a logarithmic scale of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V, 10V and 15V.**

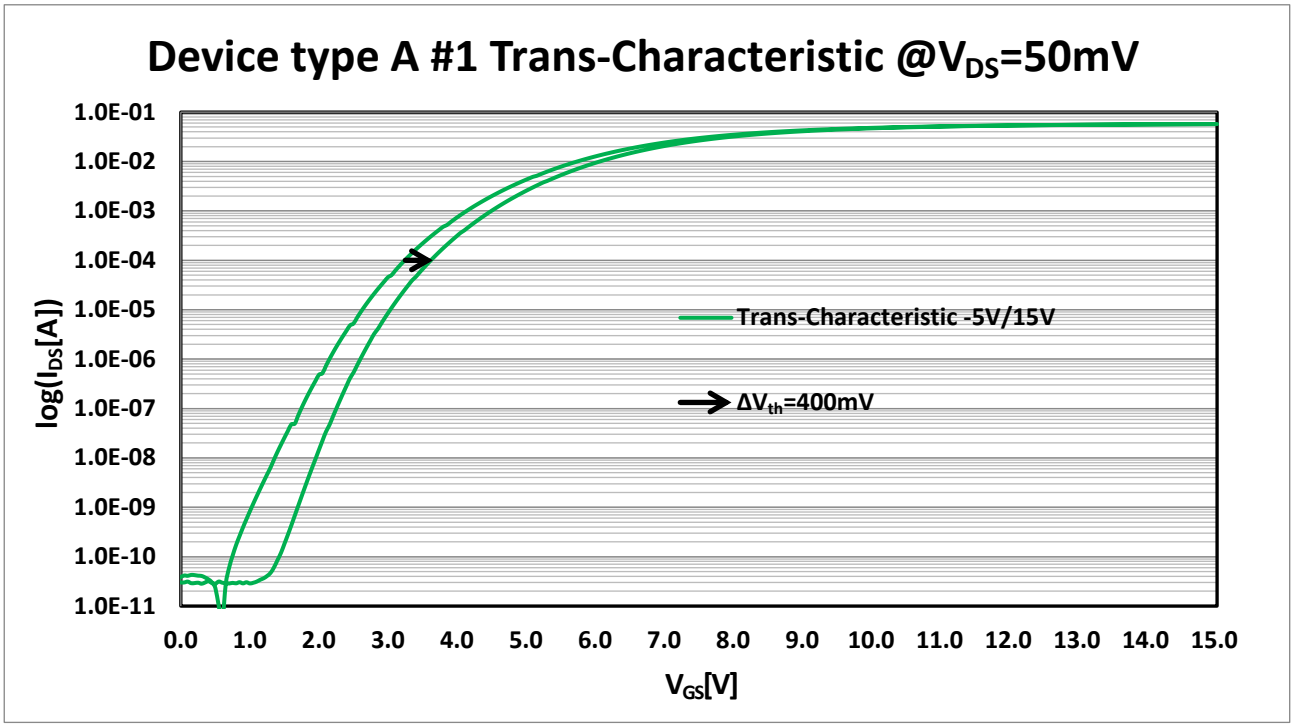



**Figure 4.2.8: Trans-characteristic in a logarithmic scale of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 15V.**

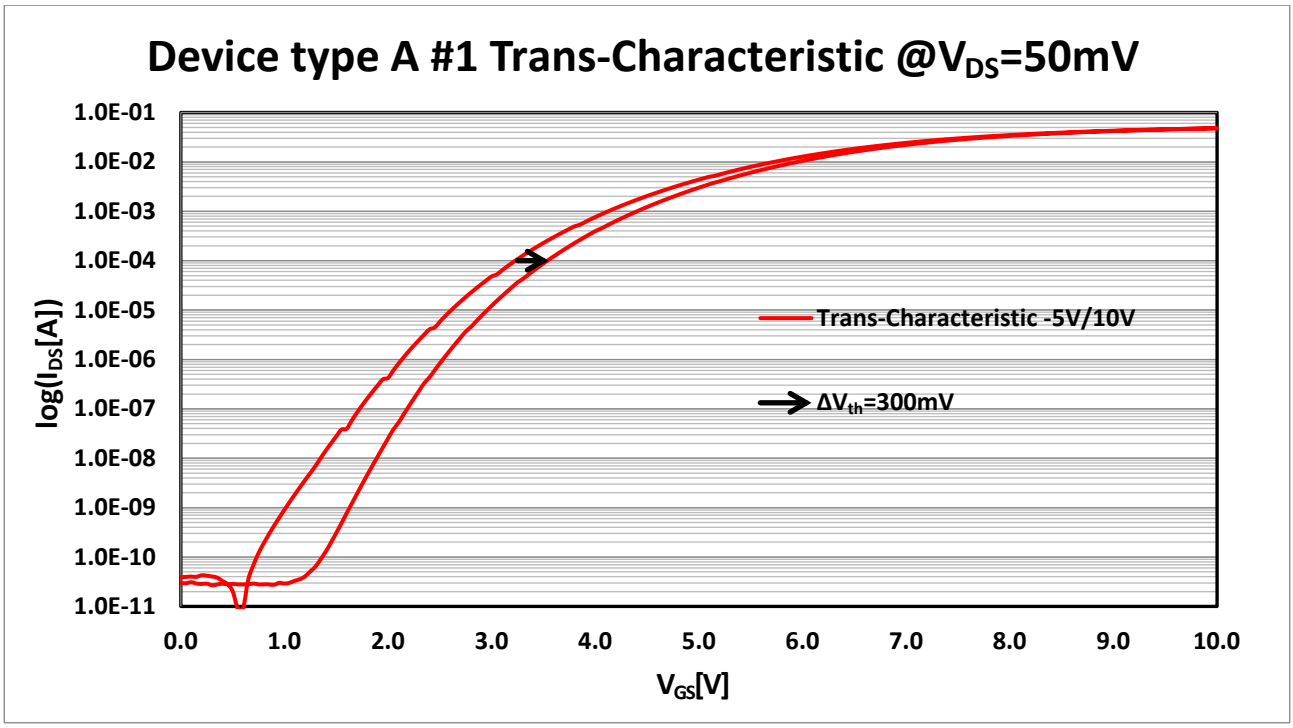



**Figure 4.2.9: Trans-characteristic in a logarithmic scale of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 10V.**

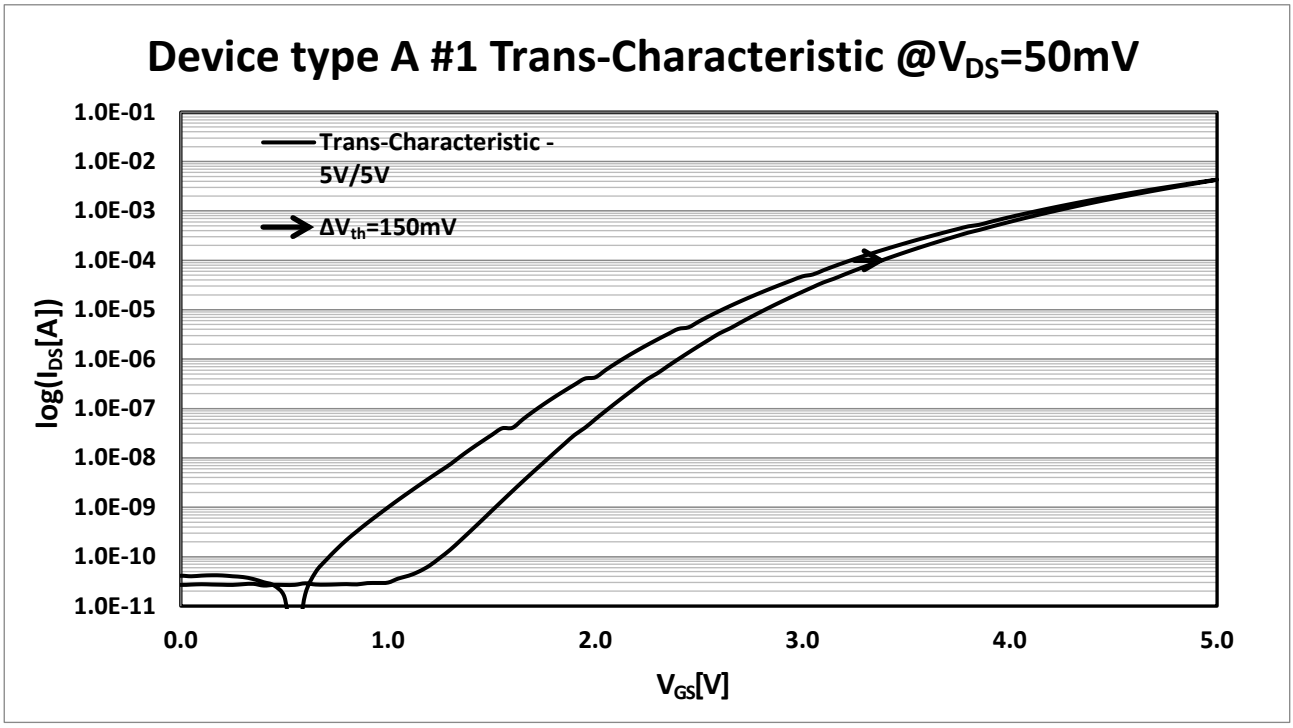



**Figure 4.2.10: Trans-characteristic in a logarithmic scale of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V.**

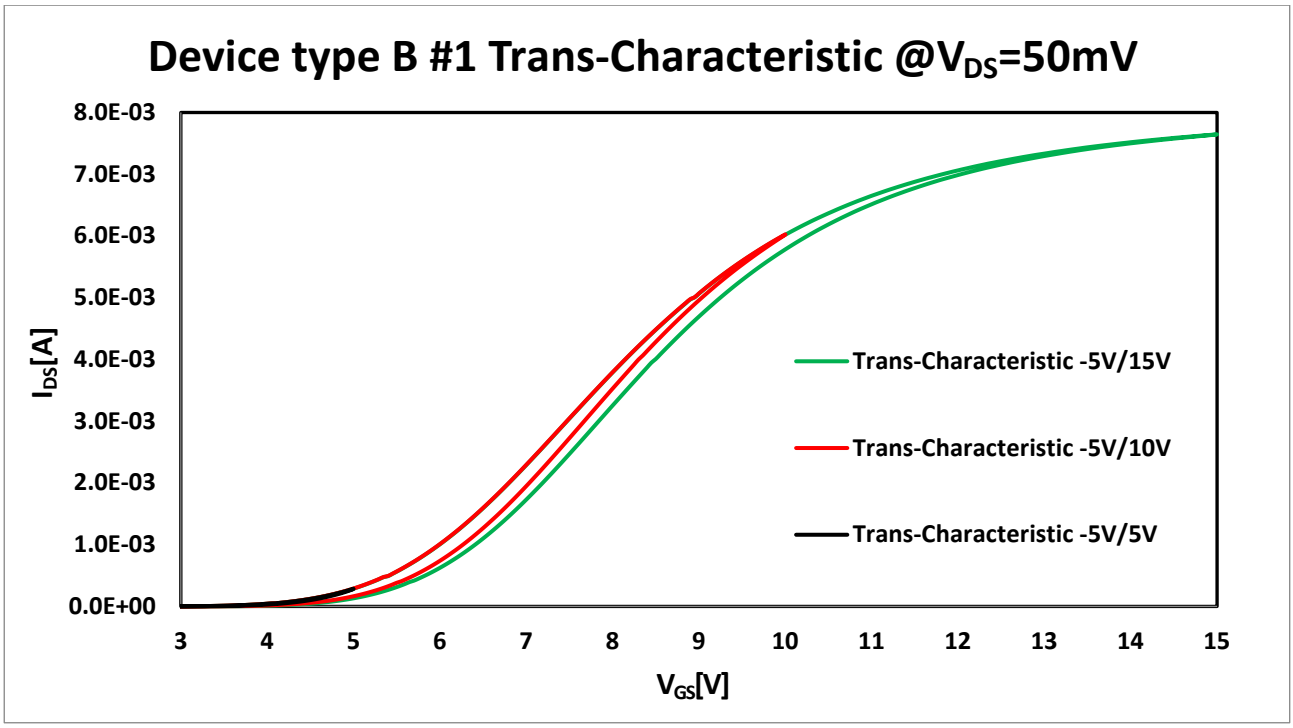



**Figure 4.2.11: Trans-characteristic of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V, 10V and 15V.**

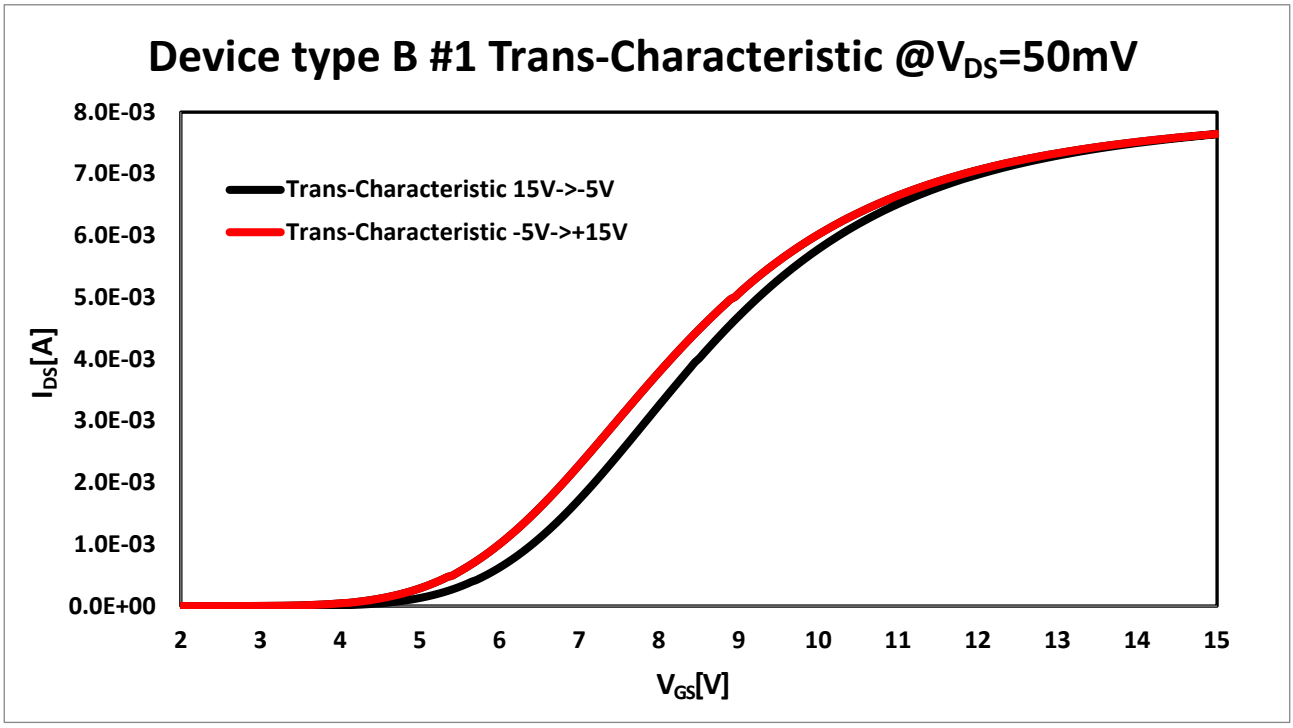



**Figure 4.2.12: Trans-characteristic of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 15V.**

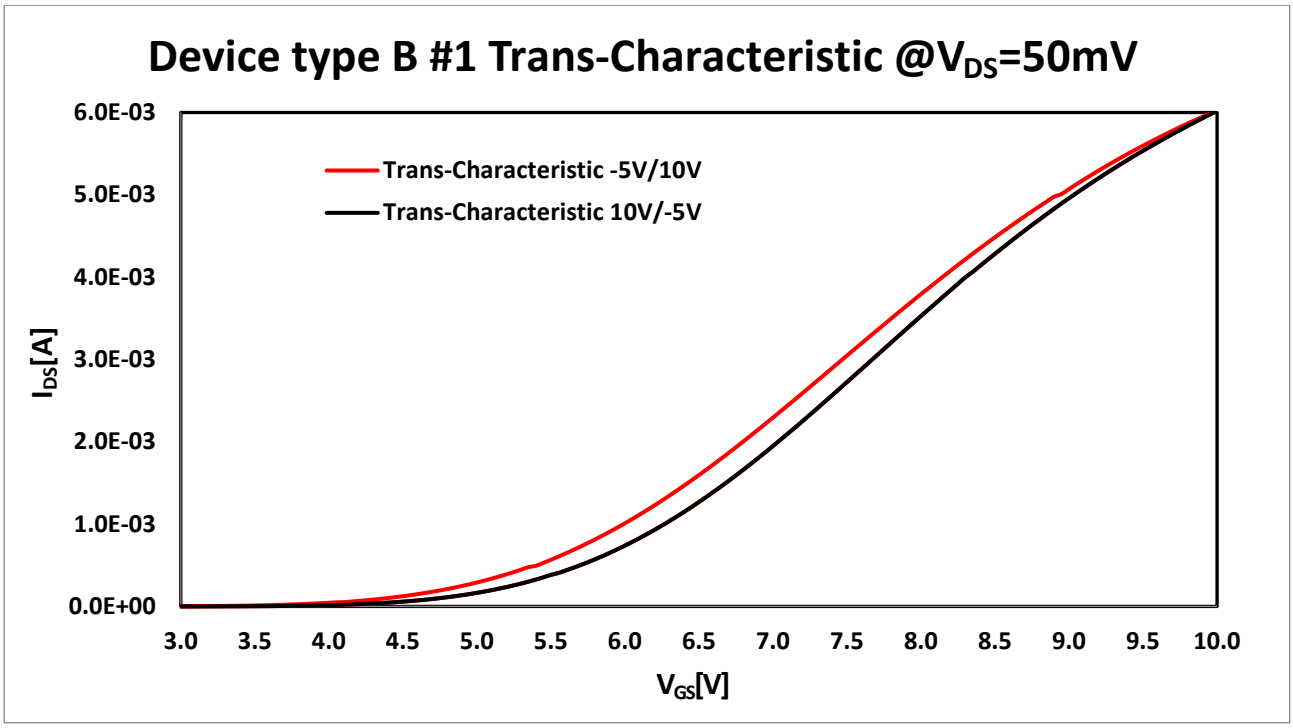



**Figure 4.2.13: Trans-characteristic of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 10V.**

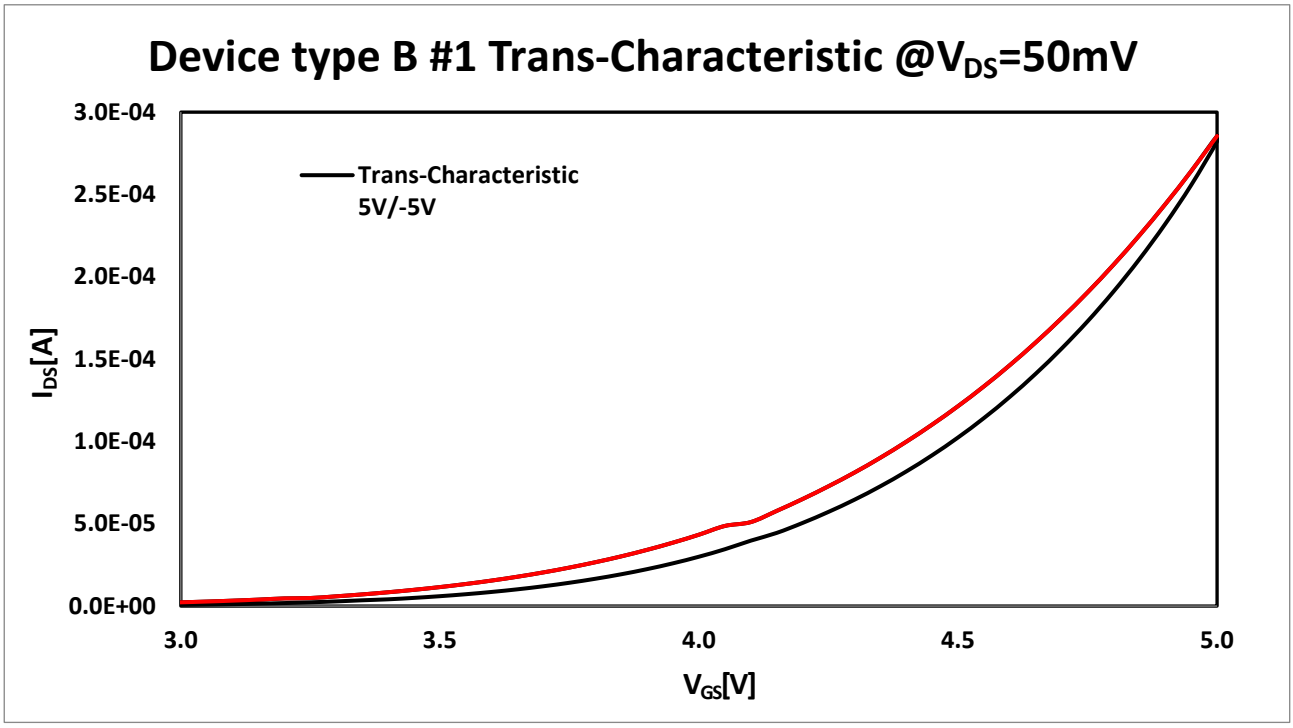



**Figure 4.2.14: Trans-characteristic of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V.**

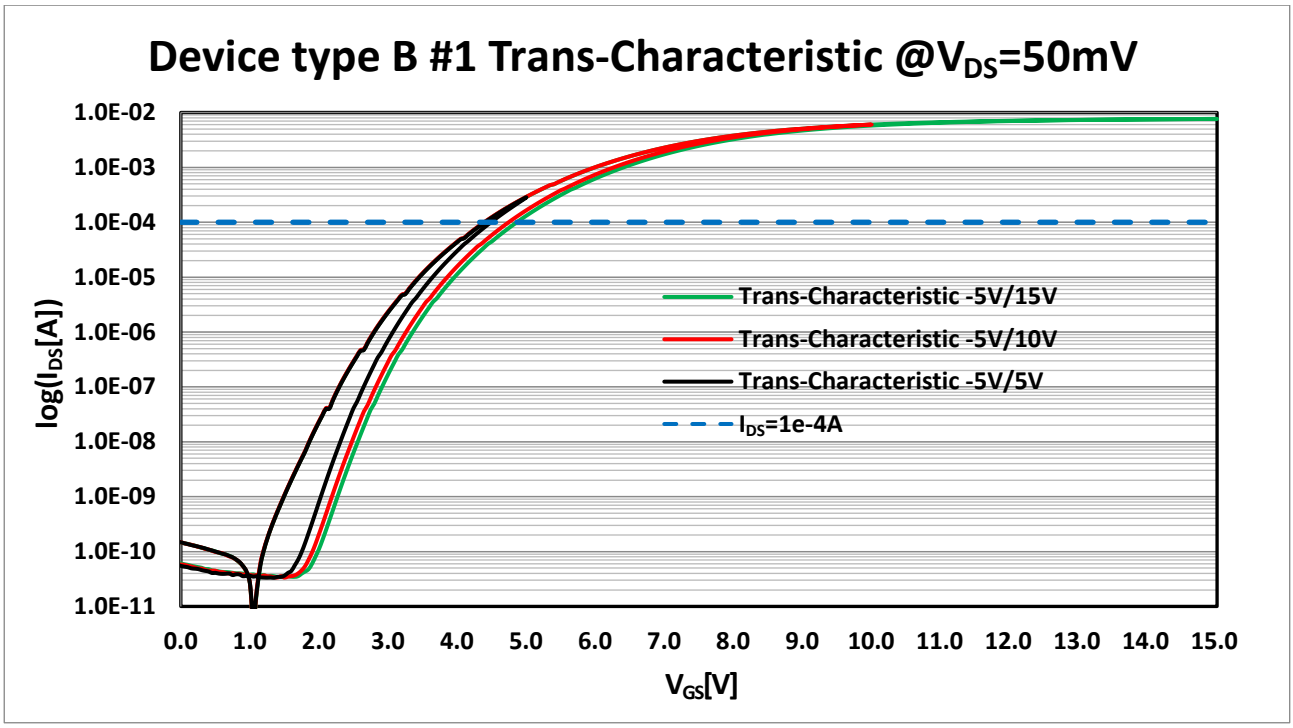



**Figure 4.2.15: Trans-characteristic in a logarithmic scale of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V, 10V and 15V.**

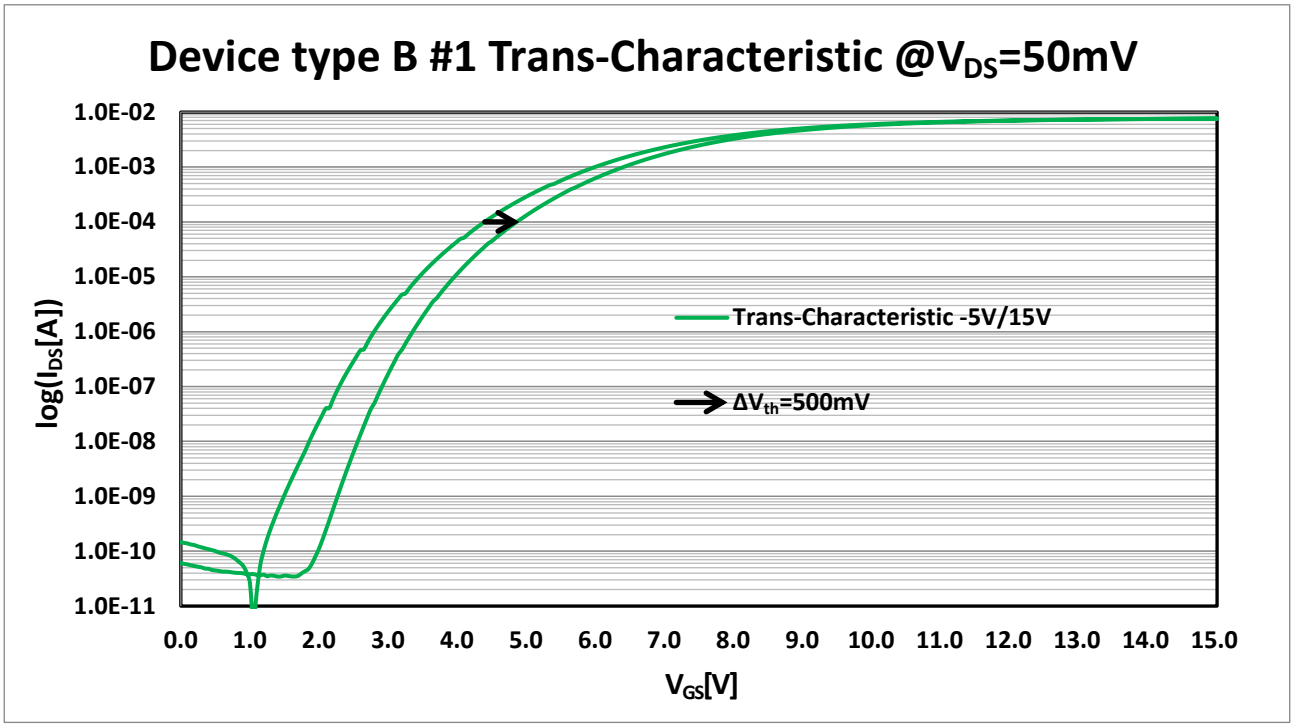



**Figure 4.2.16: Trans-characteristic in a logarithmic scale of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 15V.**

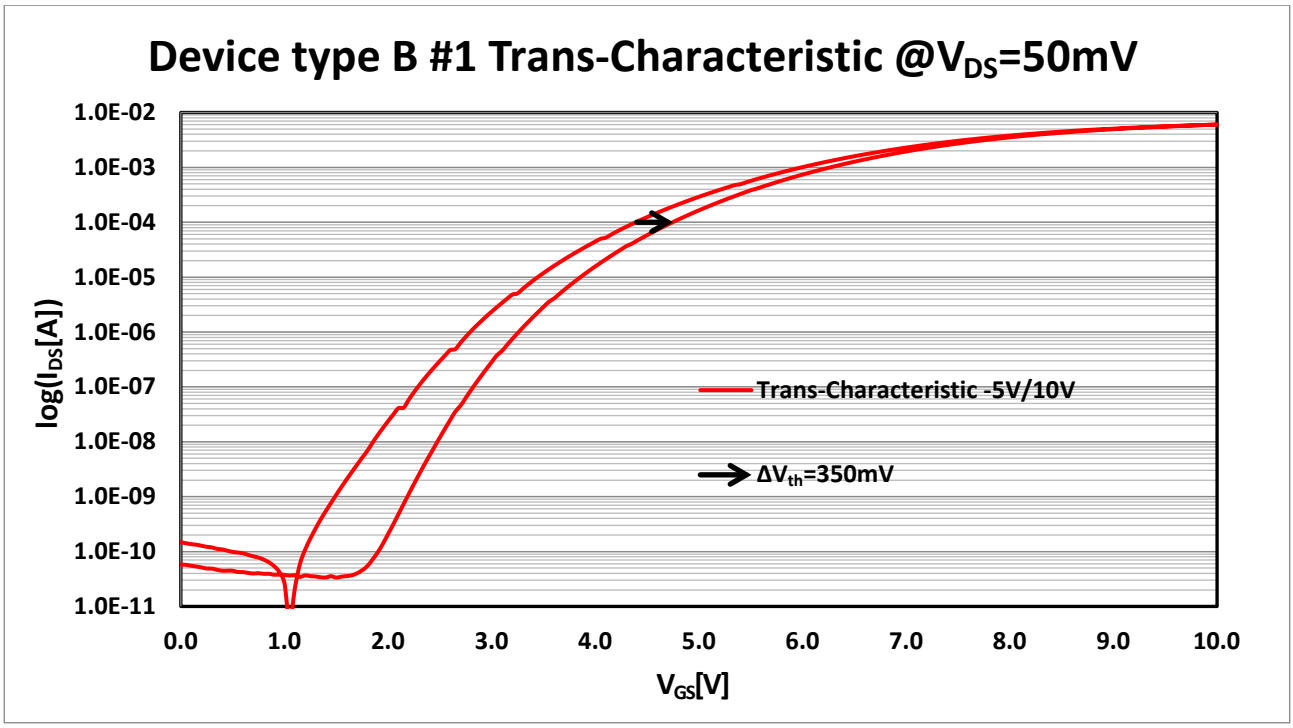



**Figure 4.2.17: Trans-characteristic in a logarithmic scale of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 10V.**

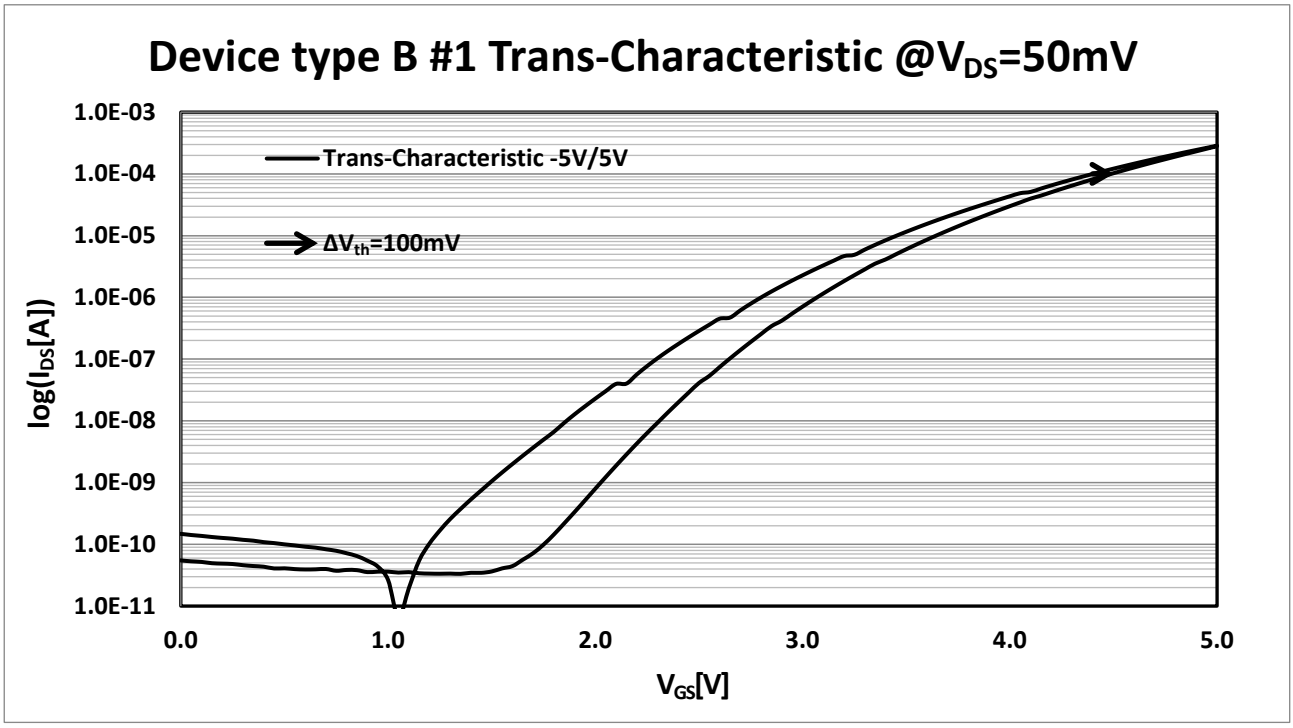



**Figure 4.2.18: Trans-characteristic in a logarithmic scale of piece 1 of the type B power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 5V.**

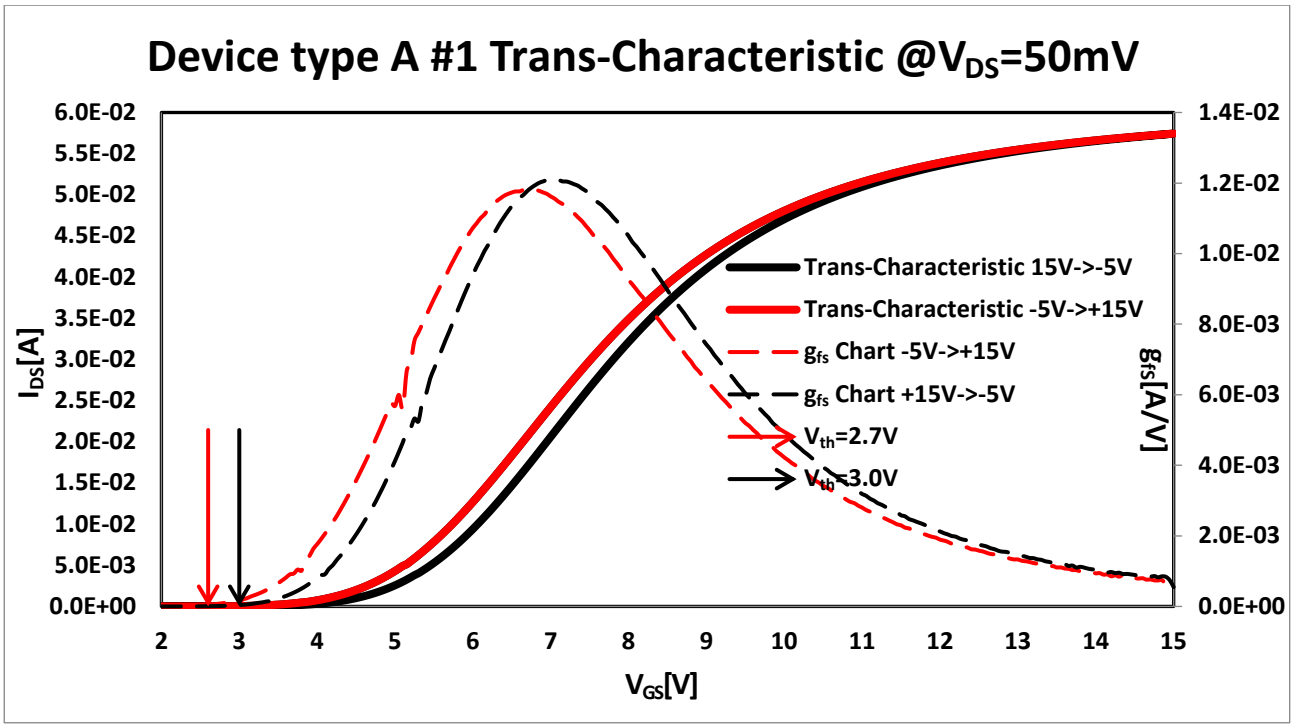



**Figure 4.2.19: Trans-characteristic of piece 1 of the type A device which shows the $g_{fs}$ and highlights the $V_{th}$.**

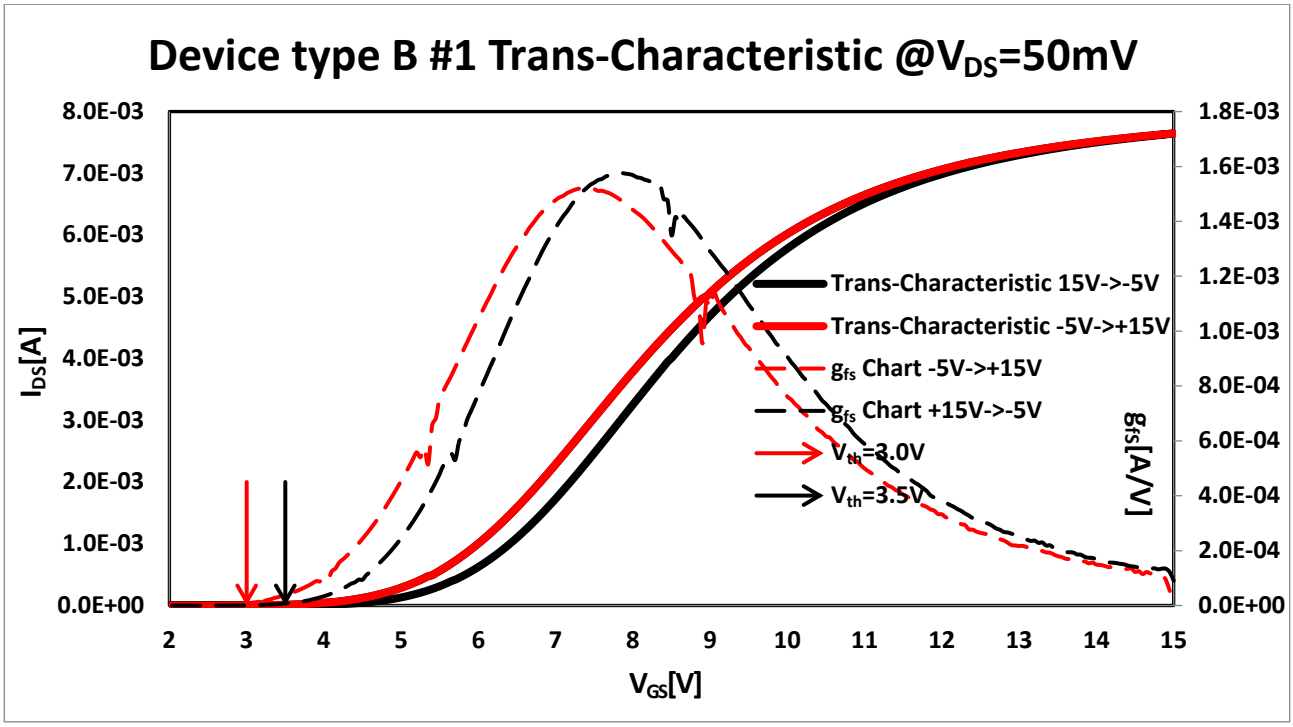



**Figure 4.2.20: Trans-characteristic of piece 1 of the type B device which shows the $g_{fs}$ and highlights the $V_{th}$.**

It was pointed in chapter 4.1 that the hysteresis phenomenon observed in the trans-characteristics of the SiC power MOSFETs (it is important to emphatize again that all the devices tested in our experiments are n-channel transistors) are due to two different trapping mechanisms. In fact, the short-term effects of the threshold voltage instability can be mainly attributed to the interface traps while the long-term effects can be mainly attributed to the oxide traps. Now, both trapping mechanisms are described in detail to better understand the results obtained in our experiments [272]. First, the short-term effects attributed to the interface traps will be analysed. Initially, the gate voltage is set to -5 V and the device is in deep accumulation. In this condition, the Fermi level is in the valance band, the interface traps are positively charged and the system is in thermal equilibrium. When the gate voltage is swept from the accumulation condition to the inversion condition, the Fermi level moves rapidly from the valence band almost to the conduction band of the SiC and, depending on the signal transient, the interface traps for a certain time could be in non-steady state condition. In practice, the system slowly goes toward thermal equilibrium by capturing electrons from the conduction band as well and emitting holes into the valence band (see figure 4.2.21). In figure 4.2.21, positively charged interface states are indicated as full circles, neutral interface states are illustrated as open circles. Therefore, the $V_{TH}^{UP}$ increases over time until the state of the interface traps approaches thermal equilibrium. The process of capturing electrons from the conduction band is characterized by the emission coefficient $e_n$. Instead, the process of emitting holes towards the valence band is characterized by the emission coefficient $e_p$. In the trapping processes only one of the two bands is mainly involved depending on the energy position of the traps. In fact, the traps located near the $E_C$ mainly exchange charges with the conduction band because the electron capture and emission coefficients are higher than the same as the holes in the valence band. Conversely, the traps located near the $E_V$ mainly exchange charges with the valence band because the holes capture and emission coefficients are higher than the same as the electrons in the conduction band. Instead, impurities positioned in the middle of the bandgap move in both the conduction band and valence band. Therefore, during the ascending phase of the trans-characteristic, until approaching the $V_{th}$, the main trapping mechanism is due to the holes emitted towards the valence band while only few electrons from the conduction band are captured. The holes emitted towards the valence band allow to determine the $E_{VTH,ep}$ value which allow to calculate the $V_{TH}$ hysteresis. The time constant for the emission of holes in the valence band can be estimated as [272]:

$$\tau_h = \frac{1}{N_V \sigma_p v_{th}} e^{\frac{E_t - E_V}{KT}} \tag{4.2.2}$$

Therefore, considering the delay time, Δt, between the gate polarization and the $V_{th}$ measurement, the $E_{VTH,ep}$ can be estimated by:

$$E_{Vth,ep} = E_V + KT \ln\left( N_V \sigma_p v_{th} \Delta t \right) \tag{4.2.3}$$

The longer Δt, the more the $E_{VTH,ep}$ approaches the middle of the bandgap and the measured $V_{th}$ hysteresis decreases. The time constant for electron capture can be obtained as:

$$\tau_c = \frac{1}{c_n n} \tag{4.2.4}$$

$c_n$ is the electron capture coefficient which measures the probability that this event occurs and it is measured in $cm^3\ s^{-1}$. It represents the electron density in the unit of time that moves from the conduction band towards the states of impurities. Furthermore, $c_n$ can be obtained as [4]:

$$c_n = \sigma_n v_{th} \tag{4.2.5}$$

$\sigma_n$ is the cross section of the traps and $v_{th}$ is the thermal velocity of the electrons. From Eq. 4.2.4) it is possible to observe that the larger the density of the charge in the inversion layer, the less time it takes to reach the thermal equilibrium.

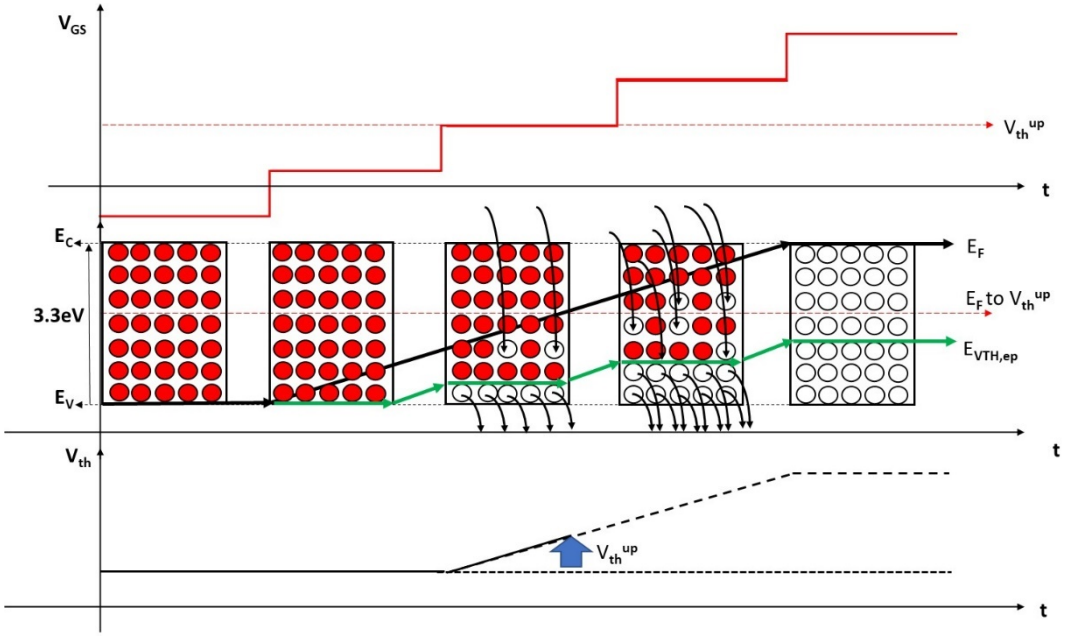



**Figure 4.2.21: Dynamics of the electron capture mechanism of the interface traps during the ascending phase of the trans-characteristic.**

Now, considering that the drain current in the triode regime can also be written as:

$$I_{DS} = \frac{qn\mu_n \mathbf{W}\delta}{\mathbf{L}} V_{DS} \tag{4.2.6}$$

since the value of the $I_{DS}$ directly depends on the density of the charge in the inversion layer and, thus, on the $V_{GS}$, the higher the drain current, the lower the $V_{th}$ shift and for this reason it is better to evaluate the hysteresis phenomenon close the subthreshold regime as can be seen in the previous figures.

Now, attention will be placed in the descending phase of the trans-characteristic as shown in figure 4.2.22. At the end of the ascending phase of the trans-characteristic the $E_F$ is in the conduction band and the device works in strong inversion regime. In the downward phase, the $V_{GS}$ decreases down to -5 V and the device switches from the strong inversion regime to the accumulation regime. During this transition, the $V_{th}^{down}$ is measured. In the meantime, the thermal equilibrium is obtained through the only emission of electrons from the interface traps in the conduction band. In fact, no holes are captured by the valence band because the device channel is in the inversion regime. When decreasing the $V_{GS}$ below the $V_{th}^{down}$, the main mechanism becomes the capture of holes from the valence band. The time constant for electron emission is equal to:

$$\tau_e = \frac{1}{N_C \sigma_p v_{th}} e^{-\frac{E_t - E_C}{KT}} \tag{4.2.7}$$

Unlike the upward sweep, in the downward sweep the thermal equilibrium in the emission of electrons is restored almost immediately because the interface trap positioned above $E_F$ are very close to $E_C$, thus, $V_{th}^{down}$ does not depends on the drain current level. Finally, from Eq. (4.2.1), the $\Delta V_{th}$ can be obtained as [272]:

$$\Delta V_{th} = \Delta V_{th}^{down} - \Delta V_{th}^{up} = \frac{qD_{it}(E_F - E_{Vth,ep})}{C_{ox}} \tag{4.2.8}$$

where $E_F$ is the Fermi level measured when reaching the $V_{th}^{down}$. Now, if the energy interval in Eq. (4.2.8) is equal to 3.3 eV as the SiC bandgap, in case of $C_{ox}$ is equal to $1.32 \times 10^{-3}$ $Fm^{-2}$, assuming $D_{it}$ in a range of $10^{11}$-$10^{12}$ defects $eV^{-1}cm^{-2}$, $\Delta V_{th}$ will be in the range of 0.4-4 V according to the results achieved in our experiments which measures $V_{th}$ shift in the order of 400-500 mV when the $V_{GS}$ reaches 15 V.

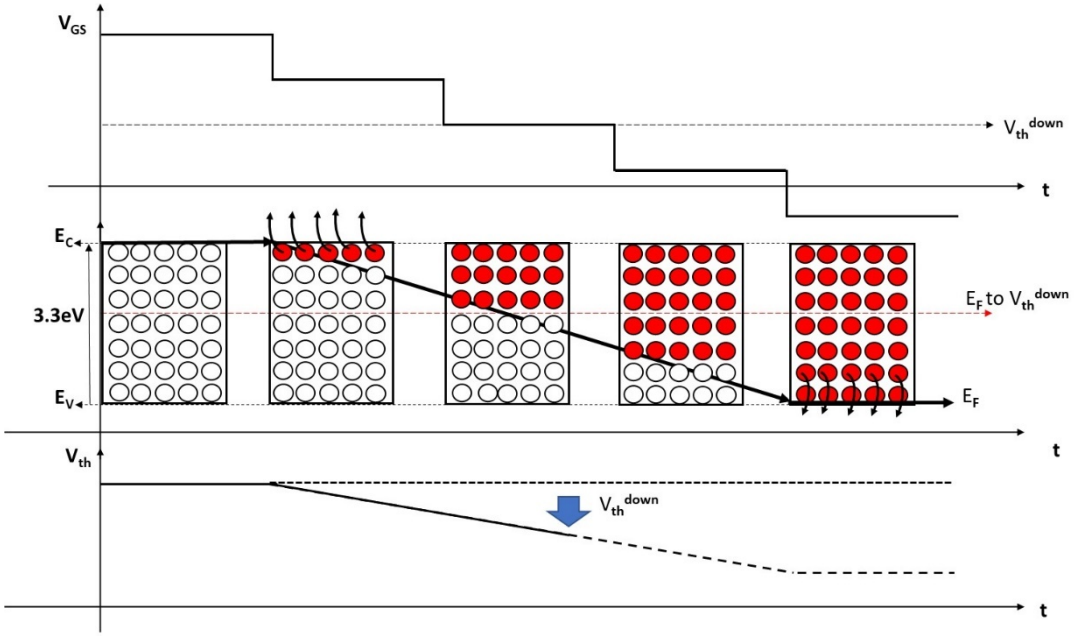



**Figure 4.2.22: Dynamics of the mechanism of emission of electrons from the interface traps during the descending phase of the trans-characteristic.**

However, it is important to underline once again that the hysteresis of $V_{th}$ due to interface traps is not classic BTI phenomenon, thus, it is typically a fully reversible.

Prevuolsly it has been stated that $V_{th}^{up}$ depends on the transient of $V_{GS}$ while $V_{th}^{down}$ does not. This phenomenon has been observed in our experiments. In fact, by a way of example, the trans-characteristics of the piece 2 of the type A device were obtained by considering three different transients of the $V_{GS}$: the normal mode as shown in figure 4.2.1, the fast mode, as shown in figure 4.2.23 and the slow mode as shown in figure 4.2.24. In the fast mode, the $V_{GS}$ was increased in 5 mV increments and the ascending and descending phase of the trans-characteristic was completed in 18 sec (the readout is quasi-instantaneous after each increment that occurs about every 2 ms). In the slow mode, the $V_{GS}$ was increased in 200 mV increments and the ascending and descending phase of the trans-characteristic was completed in 340 sec (the readout is quasi-instantaneous after each increment that occurs about every 1.7 s). The normal mode was completed in 60sec in steps of 50 mV. The comparison between the trans-characteristics obtained in these three working conditions is shown in figure 4.2.25 while in figure 4.2.26 the details of the comparison on a logarithmic scale are shown in a current range around 100 µA. As can be seen in these last graphs, the threshold-voltage instability increases slightly for a faster variation of the $V_{GS}$ and, in particular, while the $V_{th}^{down}$ remains fixed in the three different measurements, the $V_{thup}$ decreases. The $V_{th}$ shifts measured in this example are 400 mV, 405 mV and 415 mV respectively for the fast, normal and slow modes.

As already mentioned in chapter 4.1, border traps are defects within the oxide near the interface that exchange carriers with the substrate and behave like switching oxide traps. Unlike interface traps, long-term effects are attributed to border traps. The carrier exchange mechanism involved in this process is FN tunneling. The time constants associated to the trapping events depend on the distance of the traps from the interface. They can also be obtained for capture and emission events as in Eq. (3.2.16) and can be written as:

$$\tau_{cn} = \tau_{cn0}(E)e^{\frac{E_{cn}}{KT}} \quad (4.2.9)$$

$$\tau_{en} = \tau_{en0}(E)e^{\frac{E_{en}}{KT}} \quad (4.2.10)$$

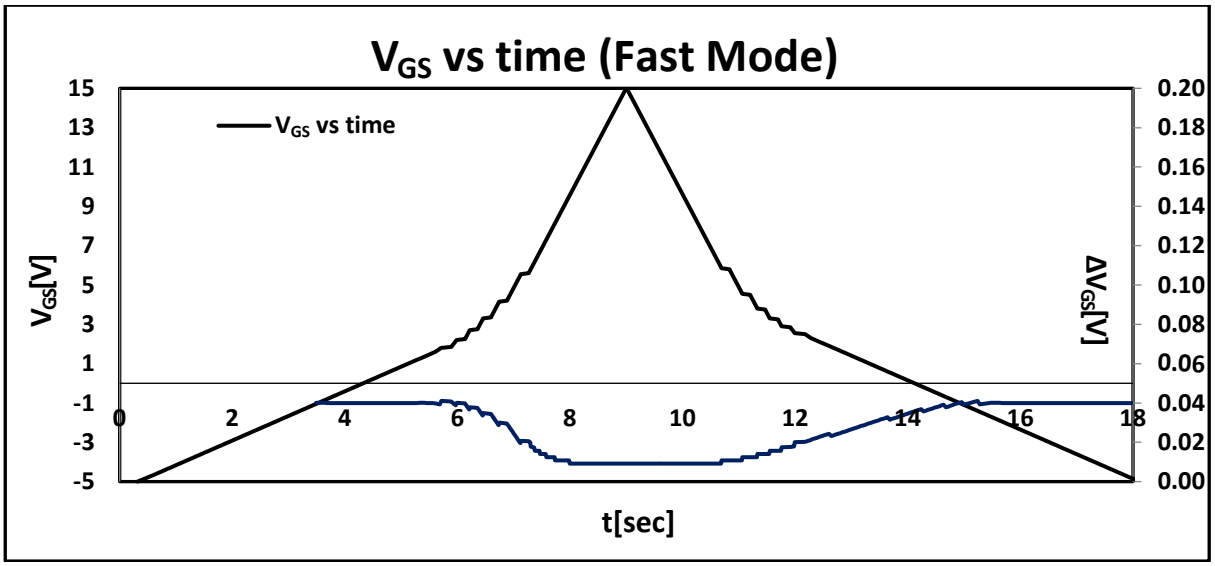



**Figure 4.2.23: $V_{GS}$ over time applied on the devices under test during the Threshold-Voltage Instability Measurements in quasi-static fast mode.**

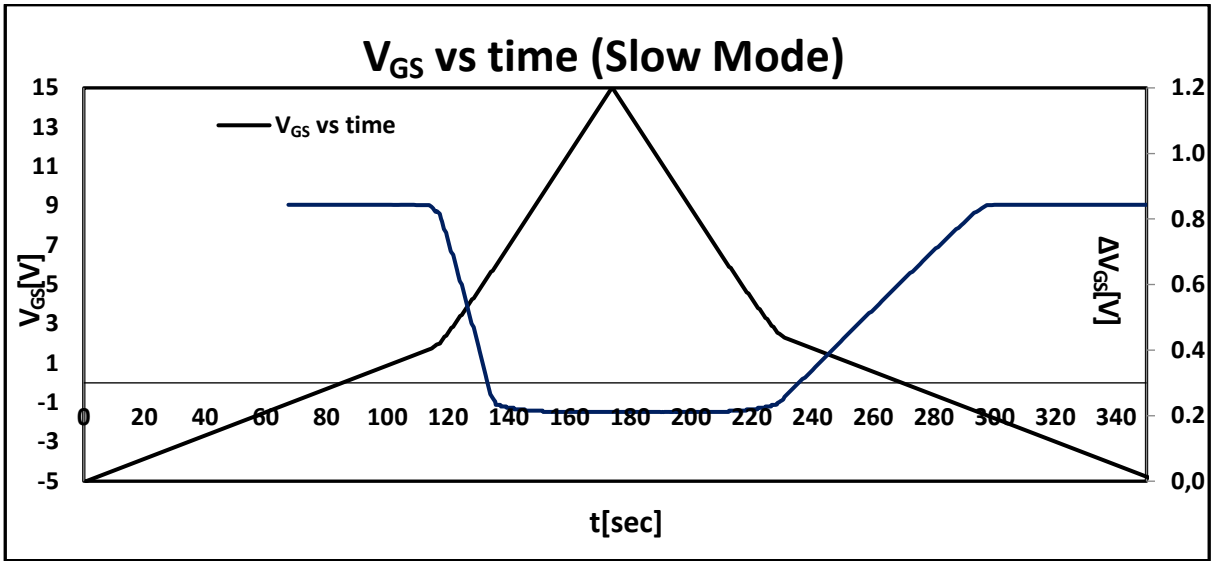



**Figure 4.2.24: $V_{GS}$ over time applied on the devices under test during the Threshold-Voltage Instability Measurements in quasi-static slow mode.**

where $E_{cn}$ and $E_{en}$ are the energy barriers for the capture and emission processes by the border traps. Therefore, the higher the energy barriers, the higher the time constants. Border traps may be better characterized from BTI tests rather than threshold-voltage instability measurements. As will be better explained later, a wide distribution of the energy barrier explains the power-law dependence of $\Delta V_{TH}$ in BTI tests as well as the logarithmic transients in BTI recovery process [273], [274]. Unlike interface states that fully charge and discharge after each switch, the border traps could be charged more than they are discharged during long-term operation and this can lead to a gradual drift of the $V_{TH}^{UP}$ and $V_{TH}^{DOWN}$ over time as shown in figure 4.2.27. The amplitude of the BTI drift, $\Delta V_{TH}^{BTI}$, during the switching process depends on the dynamic balance between the trapping and detrapping phase described by the capture-emission-time (CET) maps [274], [275].

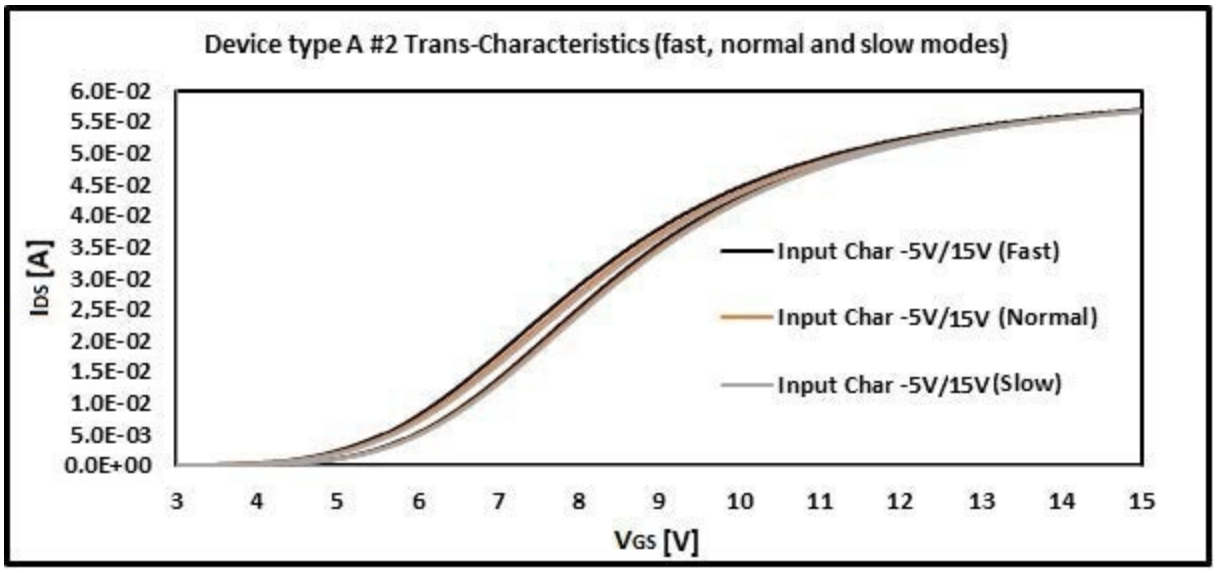



**Figure 4.2.25: Comparison between the trans-characteristics obtained with fast, normal and slow modes of piece 2 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ which reaches a value of 15V.**

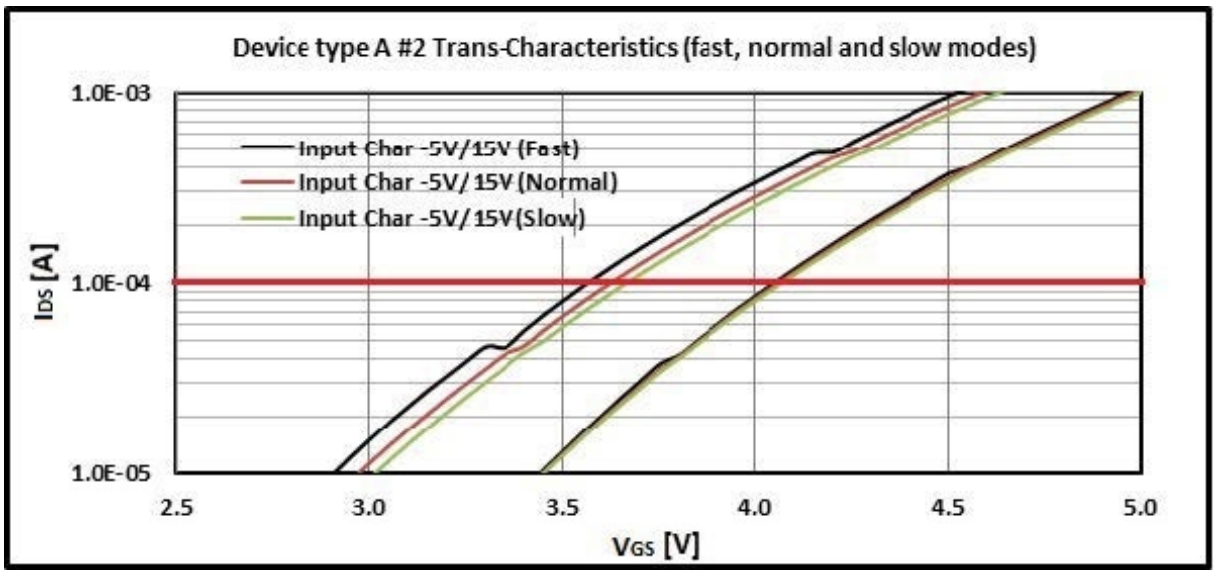



**Figure 4.2.26: Details of the comparison between the trans-characteristics on a logarithm scale obtained with the fast, normal and slow modes of piece 2 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ which reaches a value of 15V.**

The threshold-voltage instability analysis performed in quasi-static conditions on the same devices under test was also implemented in pulsed conditions according to the schematic shown in figure 4.2.2 using the ultra-fast I–V module of the pulse-measure-unit (PMU). Pulsed $I_{DS}$-$V_{GS}$ curves were obtained by applying a train of pulses with a period of 300 µs and a width of 30 µs at the gate terminal (see figure 4.2.28). The analyses were performed to compare the results obtained in quasi-static regime with those obtained with very fast transient applied on the $V_{GS}$. The trans-characteristics obtained in the pulsed regime in each tested device shows the same hysteresis phenomenon observed in the quasi-static conditions. As an example, figure 4.2.29 shows the details obtained in the $I_{DS}$-$V_{GS}$ curves in logarithmic scale for the $V_{GS}$ which reaches 5 V, 10 V and 15 V in the 100 µA range for the piece 1 of the type B device.

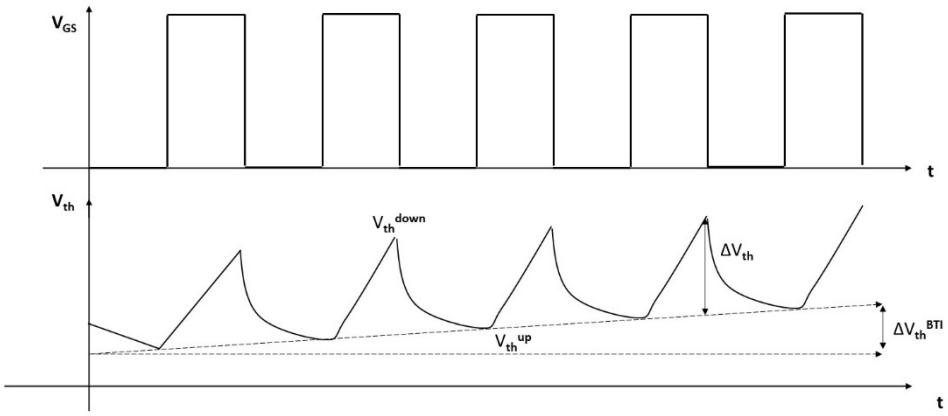



**Figure 4.2.27: Evolution of the threshold voltage over time in application.**

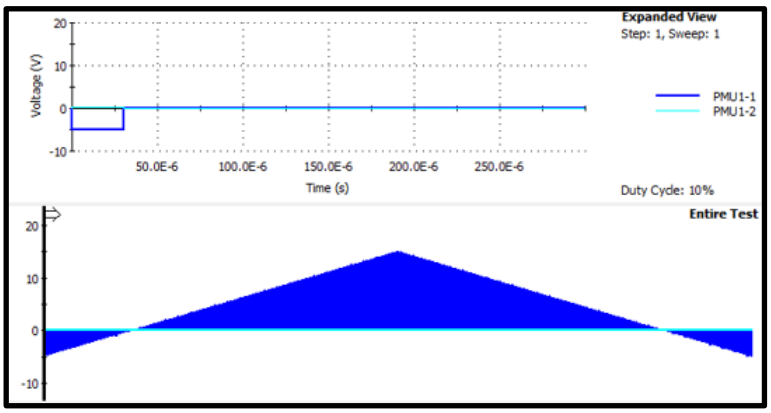



**Figure 4.2.28: $V_{GS}$ over time applied on the devices under test during the Threshold-Voltage Instability Measurements in pulsed regime.**

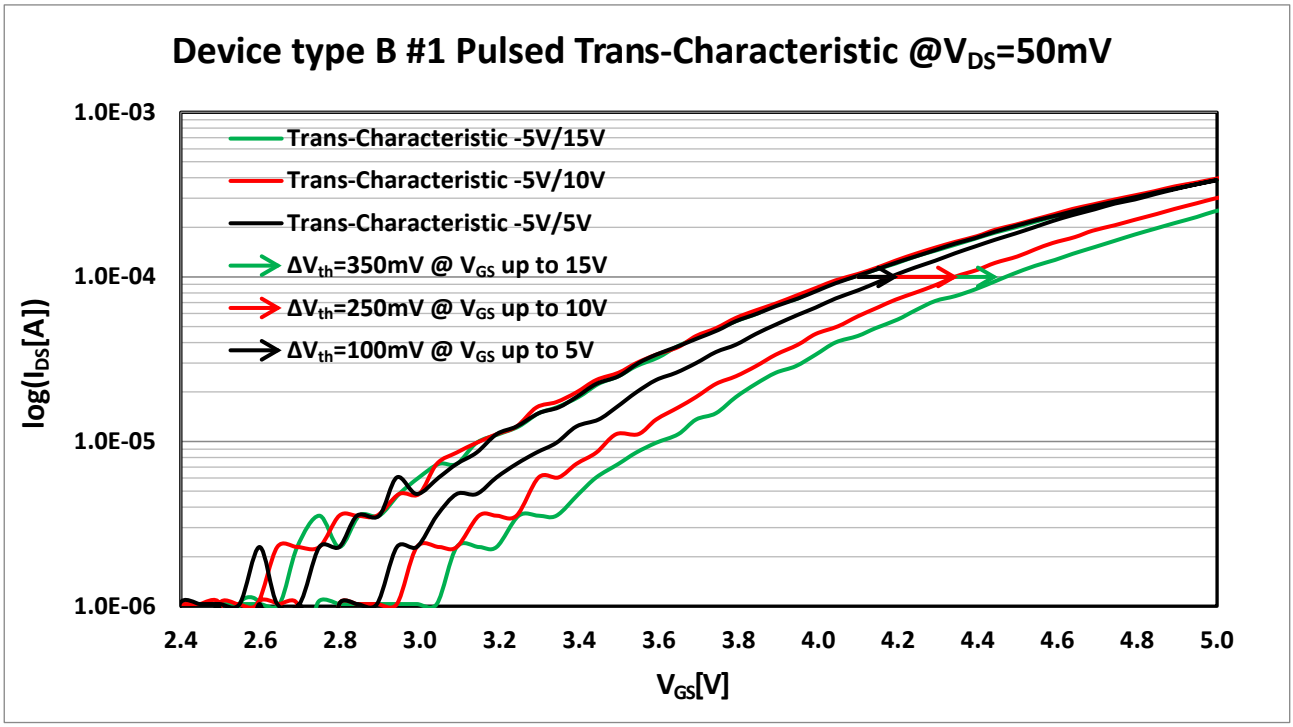



**Figure 4.2.29: Detail of the trans-characteristics on a logarithmic scale of piece 1 of the type B power MOSFET which show the hysteresis phenomenon for $V_{GS}$ which reaches values up to 5V, 10V and 15V.**

Also in these experiments it is possible to observe that the ascending phase of the characteristics of each measurement overlaps with the others confirming that the initial bias at -5V allows to reset the system. Now, it is possible to compare the $V_{th}$ shift results both in the quasi-static and pulsed regimes as shown in tab. 4.2.1. The comparison shows that in the pulsed regime the $V_{th}$ shift is lower than 150 mV and 100 mV for the $V_{GS}$ which reaches up to 15 V and 10 V with respect to the quasi-static condition. On the other hand, for the $V_{GS}$ that reaches up to 5 V, there is no difference in the $V_{th}$ shift between the two working conditions. The lower values observed in the $\Delta V_{th}$ is due to the transient of the $V_{GS}$. In fact, interface traps immediately respond to a fast transient in the $V_{GS}$ while border traps do not. Therefore, even if the $E_{VTH,ep}$ approaches the $E_V$ in faster $V_{GS}$ transients and this would lead to an increase in the $V_{th}$ shift, the lesser contribution of the border traps prevails leading to a decrease in the $\Delta V_{th}$. On the other hand, the $\Delta V_{th}$ value observed in both working conditions is related to the lowering of the $V_{th}$ (see figure 4.2.30). In fact, the $V_{th}$ decreases mainly because the border traps do not respond as mentioned above when the $V_{GS}$ transient is very fast. The comparison between the measured $V_{th}$ values for both the quasi-static and pulsed regimes based on the Williams method is summarized in tab. 4.2.2. In figure 4.2.30, the maximum value of the $I_{DS}$ is lower than that obtained by the quasi-static measurements due to external additive resistive components that cannot be eliminated. However, this phenomenon does not affect the results obtained since $V_{th}$ is estimated at 100 µA.

Another phenomenon that has been studied in these experiments has been how $V_{th}$ changes as the temperature changes. In fact, as shown in figure 4.2.2, the device is located on a hot plate to set exactly the desired temperature in a wide range of values. It is important underline that, due to the greater energy bandgap in SiC compared to silicon devices, the intrinsic concentration of carriers that can be thermally activated should be very low. Therefore, the $\Delta V_{th}$ as the T increases should be very low and, in any case, lower than with silicon devices. Figure 4.2.31 shows the $I_{DS}$-$V_{GS}$ curves obtained as function of temperature in a range between 20°C and 120°C for the piece 3 of the type B device. In this case, the $V_{th}$ value is obtained by setting the $I_{DS}$ to 1 µA. Instead, figure 4.2.32 shows how $V_{th}$ decreases as T increases. As can be seen in these graphs, the $V_{th}$ decreases rapidly with an increase in T and the rate is approximately 6.4 $mV°C^{-1}$. Unlike what is theoretically hypothesized, this estimated value is approximately the same observed in the silicon devices. This experimental result can only be explained by assuming that a smaller and smaller number of interface traps remains filled as the temperature increases [277]. Therefore, it is important to understand how temperature affects the threshold-voltage instability for tested devices. As an example, figure 4.2.33 shows the $\Delta V_{th}$ measured as a function of T for the piece 8 of the type A device. It is important to emphasize that the same behaviour was observed in the rest of the devices tested. Figure 4.2.33 shows that the $\Delta V_{th}$ decreases by increasing T. The origin of this behaviour is related to the fact that the $V_{TH}$ of the device decreases by increasing the T and to the different capture-emission time constants, CET, of the traps in the oxide [271], [275], [278]. The capture and emission processes are accelerated with increasing temperature even if the emission time constants are generally longer compared to the capture time constants. When the device is polarized at -5 V all the oxide traps are empty, thus, increasing the T, the $V_{TH}^{UP}$ remains almost the same value. Instead, by increasing the T, the $V_{TH}^{down}$ is lowered because the electrons are quickly emitted by the traps. Therefore, from Eq. (4.2.8), the $\Delta V_{th}$ decreases with increases temperature. This phenomenon will be better explained later when the BTI analysis will be introduced.

Tab. 4.2.1: Comparison in the $\Delta V_{th}$ measured between in the quasi-static and pulsed regimes.

| Piece 1 type B SiC power MOSFET | $\Delta V_{th}$ [mV] up to 15V | $\Delta V_{th}$ [mV] up to 10V | $\Delta V_{th}$ [mV] up to 5V |
|---|---|---|---|
| Quasi-static regime | 500 | 350 | 100 |
| Pulsed regime | 350 | 250 | 100 |

Tab. 4.2.2: Comparison in the $V_{th}$ measured between in the quasi-static and pulsed regimes.

| Piece 1 type B SiC power MOSFET | $V_{th}$ [V] in the ascending phase ($V_{GS}$ up to 15V) | $V_{th}$ [V] in the descending phase ($V_{GS}$ up to 15V) |
|---|---|---|
| Quasi-static regime | 3.00 | 3.50 |
| Pulsed regime | 2.65 | 3.00 |

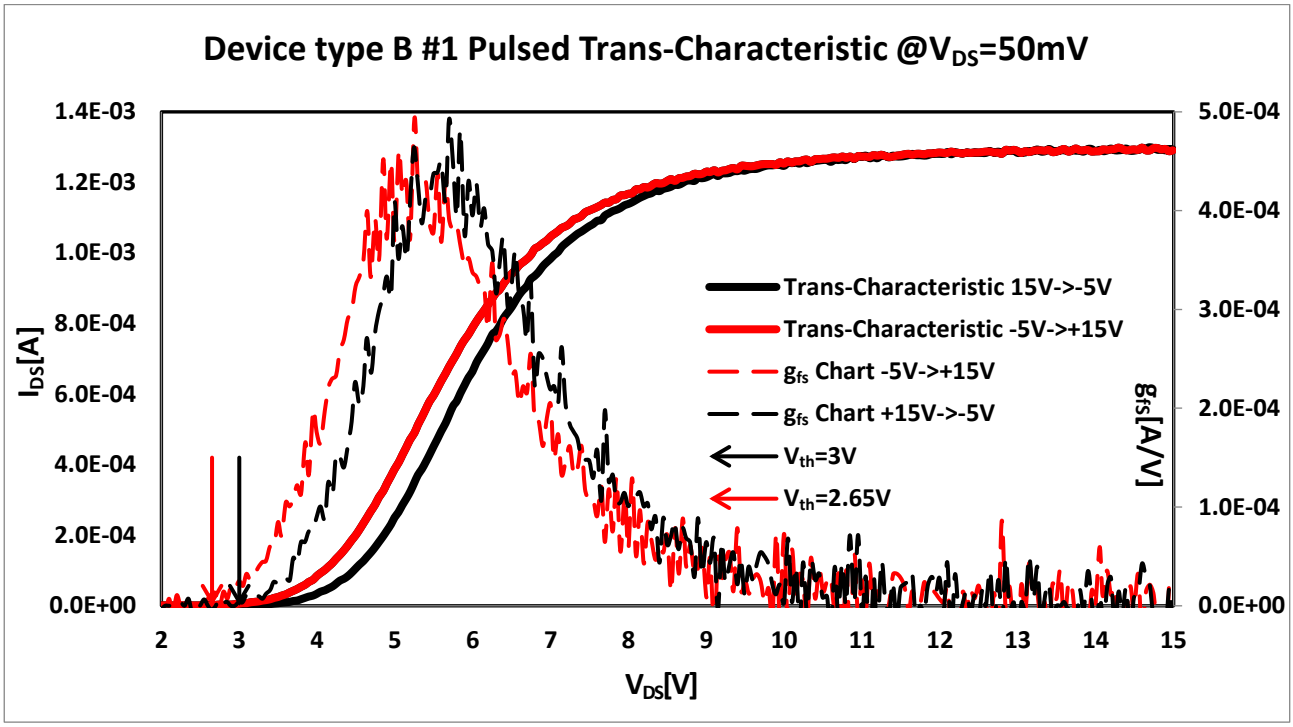



**Figure 4.2.30: Pulsed trans-characteristic of piece 1 of the type B device showing the gfs highlighting the $V_{th}$.**

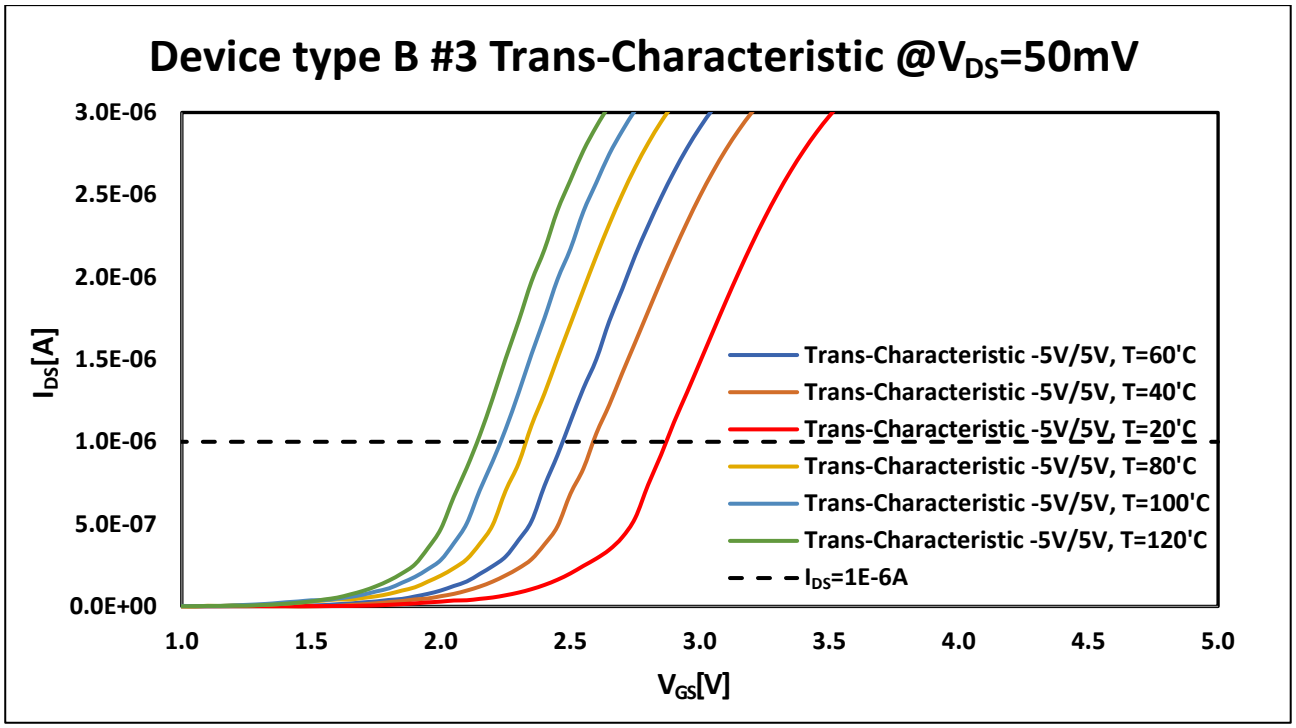



**Figure 4.2.31: Trans-characteristic of piece 3 of the type B device measured at different T which highlights the $V_{th}$.**

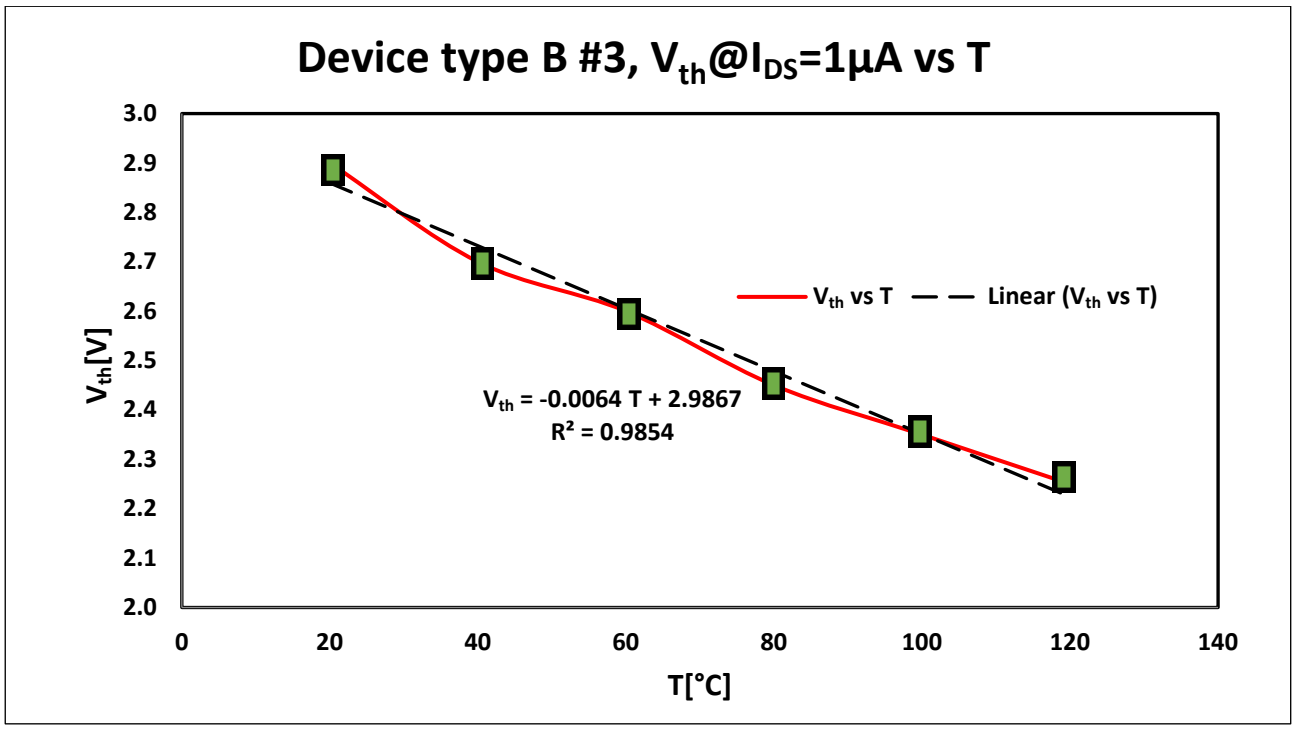



**Figure 4.2.32: $V_{th}$ as function of the temperature measured on piece 3 of the type B device by setting $I_{DS}$ to 1 µA.**

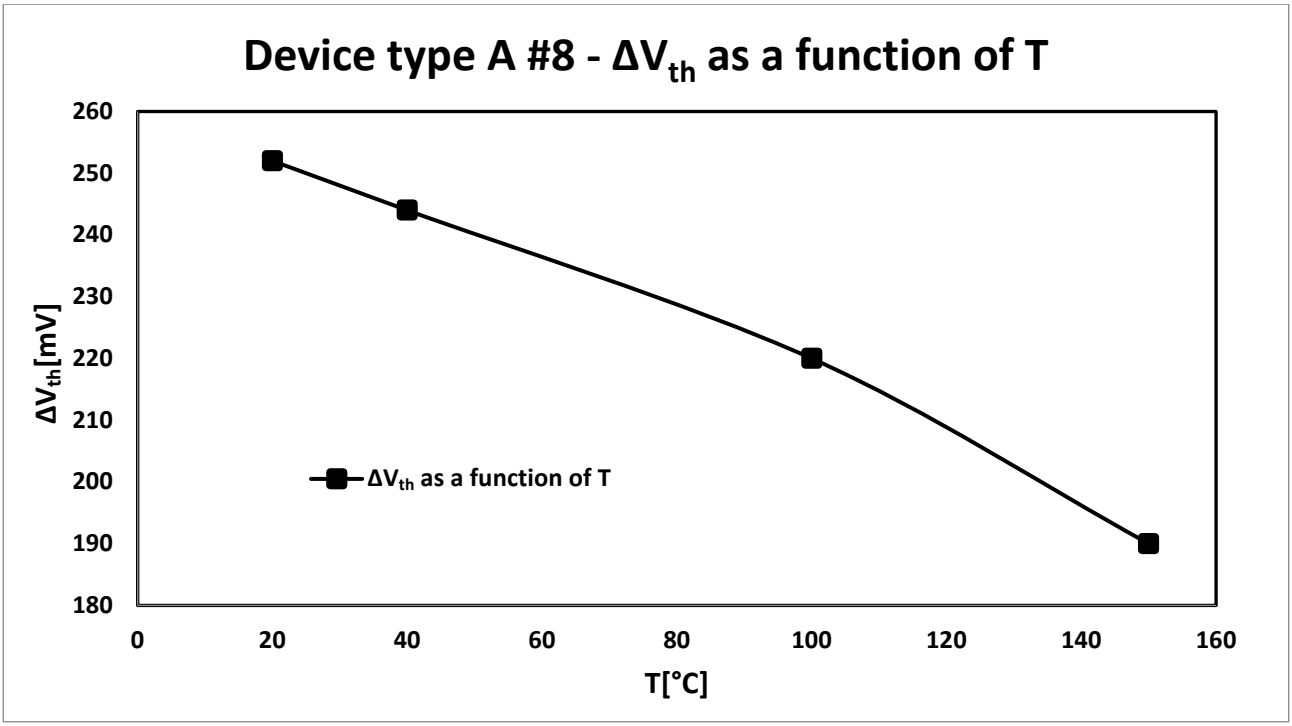



**Figure 4.2.33: $\Delta V_{th}$ as function of the temperature measured on piece 8 of the type A device under the same operating conditions as the device in figure 4.2.9.**

## 4.2.1 Effect of the Threshold-Voltage Instability on performances of SiC power MOSFETs

In applications, the threshold-voltage instability and, in particular, the BTI phenomena can influence the performance of the devices in two different ways by moving the trans-characteristic (as already seen in the previous chapter) and degrading the slope of the same trans-characteristic. Indeed, it has already been stated that the interface and the border traps are positively charged and become neutral when electrons are captured by the device channel. Therefore, as already observed experimentally, the $V_{th}$ measured in the ascending phase of the trans-characteristic is lower than the $V_{th}$ measured in the descending phase of the trans-characteristic and this determines a reduction of the drain current in the on state (by way of example, see figure 4.2.1.1 for piece 1 of the type A device which shows the lowering of the $I_{DS}$ due to the $V_{th}$ shift). Furthermore, a gradual positive drift of the $V_{th}$ reduces the overdrive voltage in the on state by increasing the $R_{ch}$ which degrades the efficiency of the system with consequent growth in the conduction losses and in the temperature of the device. In fact, $R_{ch}$ can be obtained as:

$$R_{ch} = \frac{\mathbf{L}}{\mu_n \mathbf{W} C_{ox}(V_{GS} - V_{th})} \tag{4.2.1.1}$$

From Eq. (4.2.1.1), the smaller the difference between the $V_{GS}$ and the $V_{th}$ the greater the value of the $R_{ch}$ (by a way of example, see figure 4.2.1.2 for piece 1 of the type A device). Unlike what indicated in figure 2.1.6 with regard to silicon devices, in SiC power MOSFETs the $R_{ch}$ can affect up to 50% of the $R_{DSON}$ due to the lower mobility of the carriers in the channel and the lower contribution in the $R_{drift}$ [277]. Therefore, the $R_{DSON}$ of a SiC power MOSFET is more sensitive to a reduction in the overdrive voltage compared to devices made of silicon. All these phenomena can also be a significant problem when the power MOSFETs located in the modules are connected in parallel to increase the maximum current supplied. In fact, the efficiency of the parallelization of the power MOSFETs depends on the matching of the $R_{DSON}$ and the $V_{th}$ of the single devices, otherwise an uneven distribution of the current occurs between each device.
The degradation in the slope of the trans-characteristic is due to the reduction of the mobility of the carriers in the channel by the interface and the border traps that act like scattering centers (see figure 4.2.19 and figure 4.2.20). In fact, the mobility of the carriers is directly proportional to the $g_{fs}$, thus, the slight variation observed in the peak of the $g_{fs}$ for both tested devices is due to the variation of the effective mobility. In particular, the maximum mobility of the carriers is slightly higher in the downward phase of the $I_{DS}$-$V_{GS}$ curves because the traps are neutralized and cannot attract other electrons against the oxide interface. However, the main effect in the lowering of the mobility of the carriers during the upward phase of the trans-characteristic is due to the higher overdrive voltage attributed to the $V_{th}$ shift.

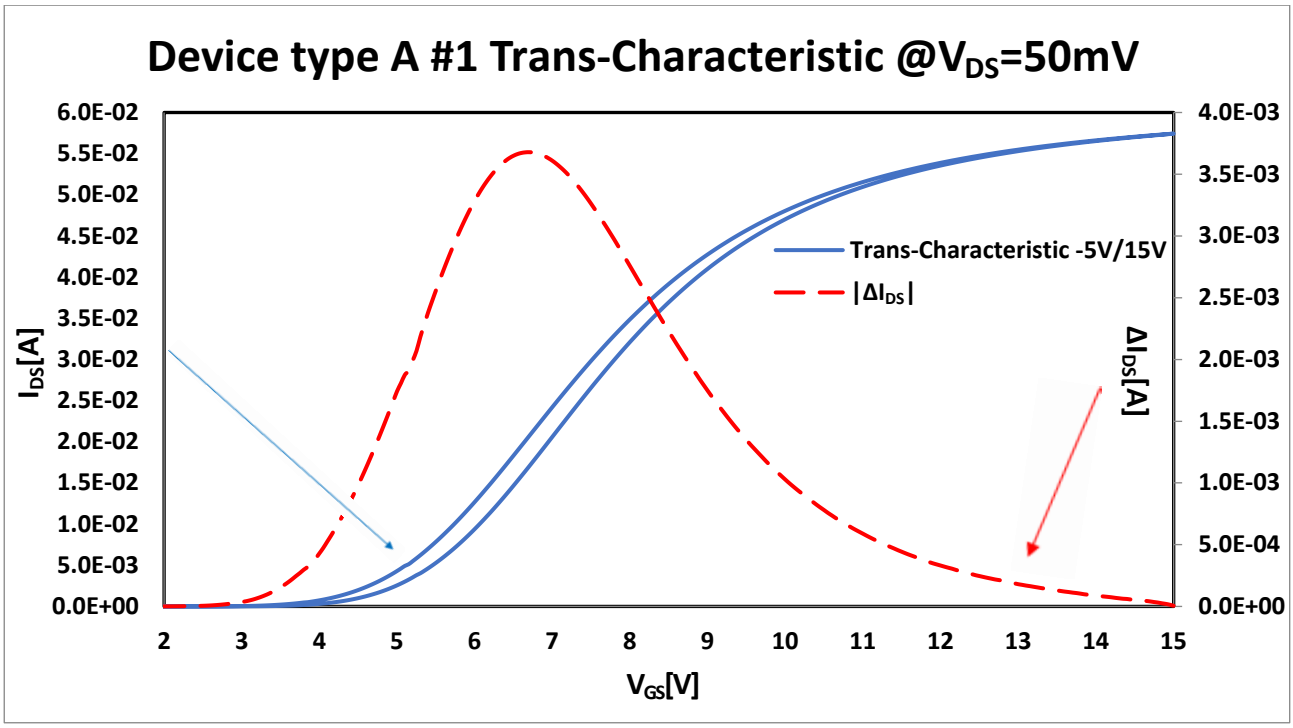



**Figure 4.2.1.1: Trans-characteristic of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 15V and highlights the decrease in the $I_{DS}$ due to the $V_{th}$ shift.**

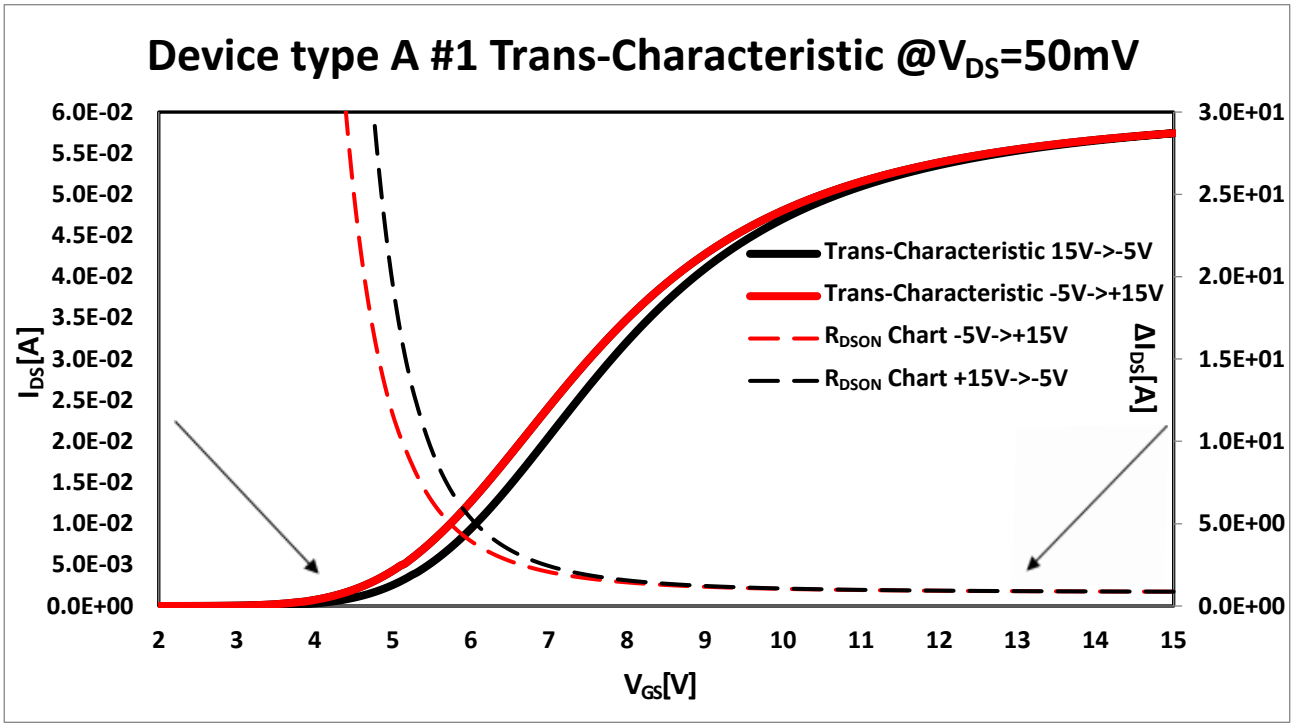



**Figure 4.2.1.2: Trans-characteristic of piece 1 of the type A power MOSFET which shows the hysteresis phenomenon for $V_{GS}$ reaching values up to 15V and highlights the increase in the $R_{DSON}$ due to the $V_{th}$ shift.**

# 4.3 Bias Temperature Instability Measurements in SiC power MOSFETs

BTI instability phenomena have already been briefly introduced in chapter 2.1.4. In this chapter, we will discuss the results of the Positive Bias Temperature Instability phenomena, PBTI, obtained by means of suitable measurements performed on the n-channel SiC power MOSFETs already tested during the threshold-voltage instability measurements. The equipment used to characterize BTI phenomena is the same utilized in the previous experiments, that is, the Keithley 4200 Semiconductor Characterization System (4200-SCS) by means of SMU units. As already mentioned during the study of the phenomenon of the hysteresis of the trans-characteristics of the devices, two types of defects are involved: interface traps and border traps. The former are fast traps and are modeled by SRH analysis. They can be easily characterized by the study of the hysteresis of the trans-characteristics as discussed in chapter 4.2. Instead, the border traps are oxide traps near the interface and, in general, are slow traps even if some of them, the closest to the interface region, are as fast as the interface traps. They can be better characterized just with PBTI analyses. The electric circuit used to perform BTI measurements on the tested devices is shown in figure 4.2.2. The procedure adopted for measuring BTI involves several steps: initial stabilization, measurement of the $I_{DS}$-$V_{GS}$ reference curve, multiple stress-sense measurements. Initial stabilization is performed by applying a negative gate voltage of -5 V for 10 s. During this phase, the device is stabilized by releasing the originally trapped charges. After this phase, an entire $I_{DS}$-$V_{GS}$ curve is measured by sweeping the $V_{GS}$ from 0 to 3.5 V and setting the $V_{DS}$ at 50mV. During the stress phase, the device is biased by applying a positive gate voltage and the $V_{DS}$ is fixed at 50mV, while during the sense phase the gate voltage is reduced to 3.5 V always fixing the $V_{DS}$ at 50mV. The stress phase is repeated several times by applying different voltages to the gate. The various stress pulses over time are applied as shown in figure 4.3.1 with a logarithmic increases in the stress time while the sense is immediately performed after each stress pulse in 60 ms. The observed decrease of the drain current during the sense phase is converted into the $V_{th}$ shift through the previously measured $I_{DS}$-$V_{GS}$ reference curve. Immediately after the stress phase, the recovery phase is performed similarly to the stress phase. In the latter case, the recovery pulses over time are applied both by short-circuiting the gate and source terminals and by applying a negative voltage on the gate as shown in figure 4.3.1. Immediately after each recovery pulse, the observed increase in the drain current is converted into the $V_{th}$ shift through the previously measured $I_{DS}$-$V_{GS}$ reference curve. By way of example, the first experimental results showing $\Delta V_{th}$ as a function of the time for both the stress and the recovery phases are shown in figure 4.3.2 and in figure 4.3.3 with reference to piece 2 of the type A device setting T at 20°C. From these graphs it is possible to observe that:

a) By applying a positive polarization to the gate, negative charges are captured inside the oxide which, as seen in the previous experiment, leads to a positive $\Delta V_{th}$. This effect is accelerated by increasing the gate voltage and is called Positive Bias Temperature Instability (PBTI).
b) During the recovery phase, the electrons captured in the stress phase are released from the oxide and this leads a negative $V_{th}$ shift. This effect is accelerated with the reduction of the gate voltage which is also fixed at negative values during the recovery phase as shown in figure 4.3.4 which considers the results carried out on the piece 3 of the type A device setting T at 80°C.

In this case, the recovery of $V_{th}$ is not completely achieved as instead observed for the piece 2 because more time is needed for the recovery.

c) As can be seen from figure 4.3.2 and figure 4.3.3, the recovery of a substantial part of $V_{th}$ occurs immediately when the voltage applied to the gate is removed after the stress phase. With reference to piece 2, the $\Delta V_{th}$ is completely recovered and this indicates that no permanent damage has been introduced during the stress phase.

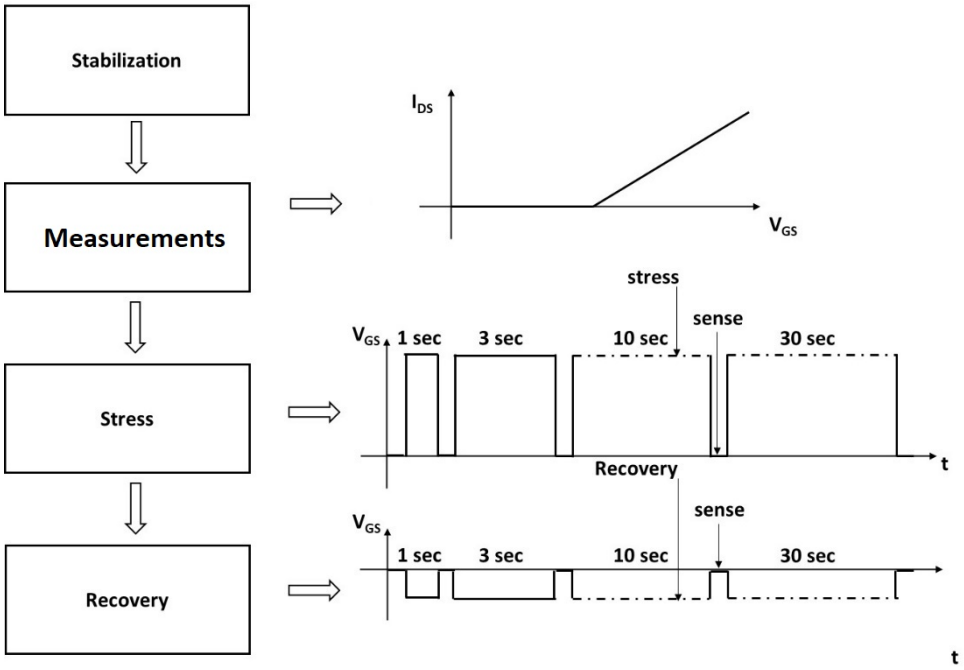



**Figure 4.3.1: BTI test procedure performed on SiC power MOSFETs tested in the previous experiment.**

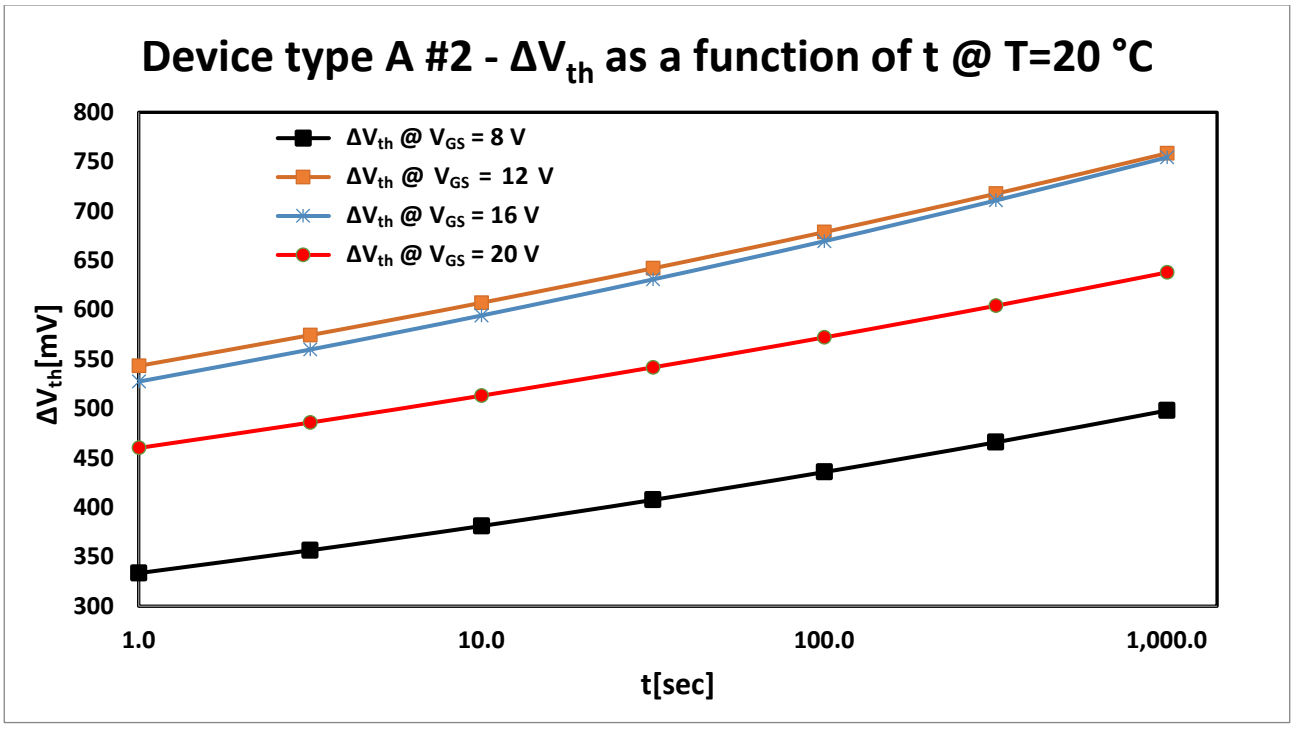



**Figure 4.3.2: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type A device for different stress values of the $V_{GS}$.**

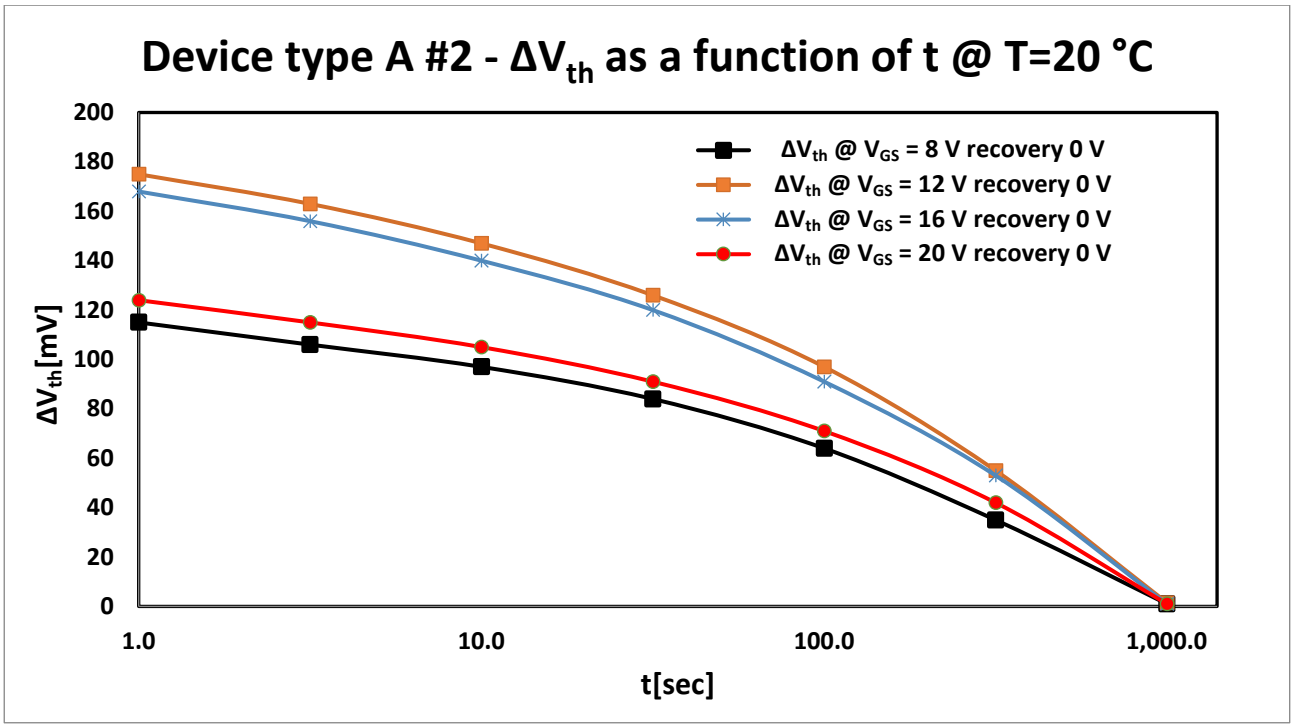



**Figure 4.3.3: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the recovery phase of piece 2 of the type A device when the $V_{GS}$ is equal to 0 V for different stress values of the $V_{GS}$.**

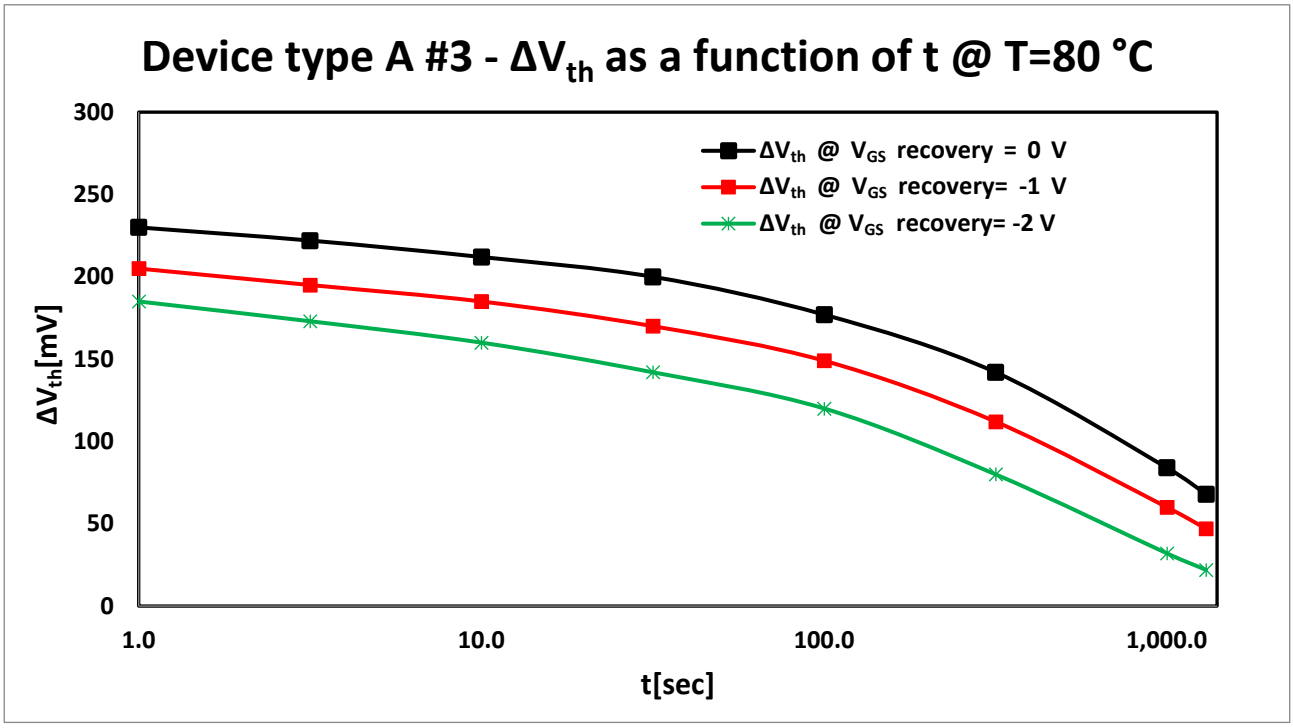



**Figure 4.3.4: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the recovery phase of piece 3 of the type A device when the $V_{GS}$ is equal to 0 V, -1 V and -2V for the stress value of the $V_{GS}$ equal to 8V and setting T at 80°C.**

To understand how temperature influences the BTI phenomenon, as an example, a complete characteriation was carried out on the piece 2 of the type B device. Figure 4.3.5, figure 4.3.6 and figure 4.3.7 show the $\Delta V_{th}$ as a function of time by setting the $V_{GS}$ to 8 V, 12 V and 16 V and varying T, tempertature, from 20°C up to 120°C. Instead, in figure 4.3.8, figure 4.3.9 and figure 4.3.10 are shown the $\Delta V_{th}$ as a function of time by setting T to 20°C, 100°C and 150°C and varying the $V_{GS}$ from 8 V to 16 V for the same device tested. The experimental results obtained for the piece 2 of the type B device are similar to those of the piece 2 of the type A device but a surprising dependence of the $\Delta V_{th}$ from temperature during the stress phase has been observed. In fact, the $\Delta V_{th}$ becomes smaller by increasing the temperature. A similar phenomenon was also observed during the recovery phase, as shown in figure 4.3.11 for piece 3 of the type A device. In this case the $V_{GS}$ is set to -2 V during the recovery phase by varying the T from 40°C to 100°C while the $V_{GS}$ was set to 8 V during the previous stress phase. However, in the latter case, it is worth pointing out that the maximum $\Delta V_{th}$ reached during the stress phase at lower temperatures is much higher than the same reached at higher temperatures, thus, the comparison is not directly related even if the differences in $\Delta V_{th}$ decrease with incresing T. All the results obtained from these experiments and the considerations made will be explained in this chapter to understand the nature of the observed phenomena. However, in first place, it is important to underline two other aspects that can be observed from these experimental results. The first concerns the fact that $\Delta V_{th}$ for both the stress and recovery phases roughly follows a power law as function of the stress time in the BTI tests. In fact, the graphs were obtained considering a logaritmic scale in the time axis. Indeed, as mentioned in chapter 3.1.4 and with reference to Eq. (3.1.4.2), the capture and emission events of electrons from the interface traps and border traps can be modeled as stochastic processes composed of many G-R phenomena with different time constants. Therefore, considering that the $\Delta V_{th}$ is proportional to the number of traps filled, applying the logaritmic function to Eq. (3.1.4.2), it is possible to obtain:

$$\ln(\Delta V_{th}) \propto \ln[\sum_i[\ln(N_{t0i})] - N_t(t)] = t \sum_i[\alpha_i^*] \tag{4.3.1}$$

The latter is the the equation of a straight line. Indeed, in figure 4.3.12, the logarithmic of $\Delta V_{th}$ shows a perfect linear trend as a function of time for different $V_{GS}$ during the stress phase with reference to the same piece 2 of the type B device previously tested. Therefore, based on Eq. (4.3.1), the slope of the straight lines representing the trend of the logarithmic of $\Delta V_{th}$ over time is proportional to the coefficients $\alpha_i^*$ which are the inverse of the capture and emission time constants as shown in figure 4.3.12. The second aspect concerns the fact that the time necessary to not detect any instability effect during the BTI tests can be estimated as explained in the work of Lelis et al. [198]. This time can be estimated by extrapolating the data from the logaritmic-linear graph of the $\Delta V_{th}$ over time during the BTI tests as shown in figure 4.3.13 for the stress phase of piece 2 of type A device by setting T at 20°C. By extrapolating the data in Fig. 4.3.13, in order not to see any instability effect, stress times must be considered which are in a range from 10 ns to 1000 ns depending on the $V_{GS}$ applied and which cannot be set with instrumentation used because too short. However, it is important underline that the stress time required to not detect any instability effect is strongly related to T as shown in figure 4.3.14 which refers to piece 2 of the type B device. On the basis of this model, it is possible to predict the dependence between the $V_{th}$ shift and the sense time. In the latter graph, it is possible to observe that the higher T, the shorter the time and this effect is closely related to the surprising dependence on $\Delta V_{th}$ on the temperature previously discussed. Based on the works of McLean [264] and Oldham et al. [266], performed on the interface between silicon and $SiO_2$ in the 70s and 80s, the observed BTI phenomena are due to the direct tunneling of electrons from the channel towards the border traps that penetrate inside the dielectric layer for about 2 Å every decade of time assuming a uniform distribution of the traps.

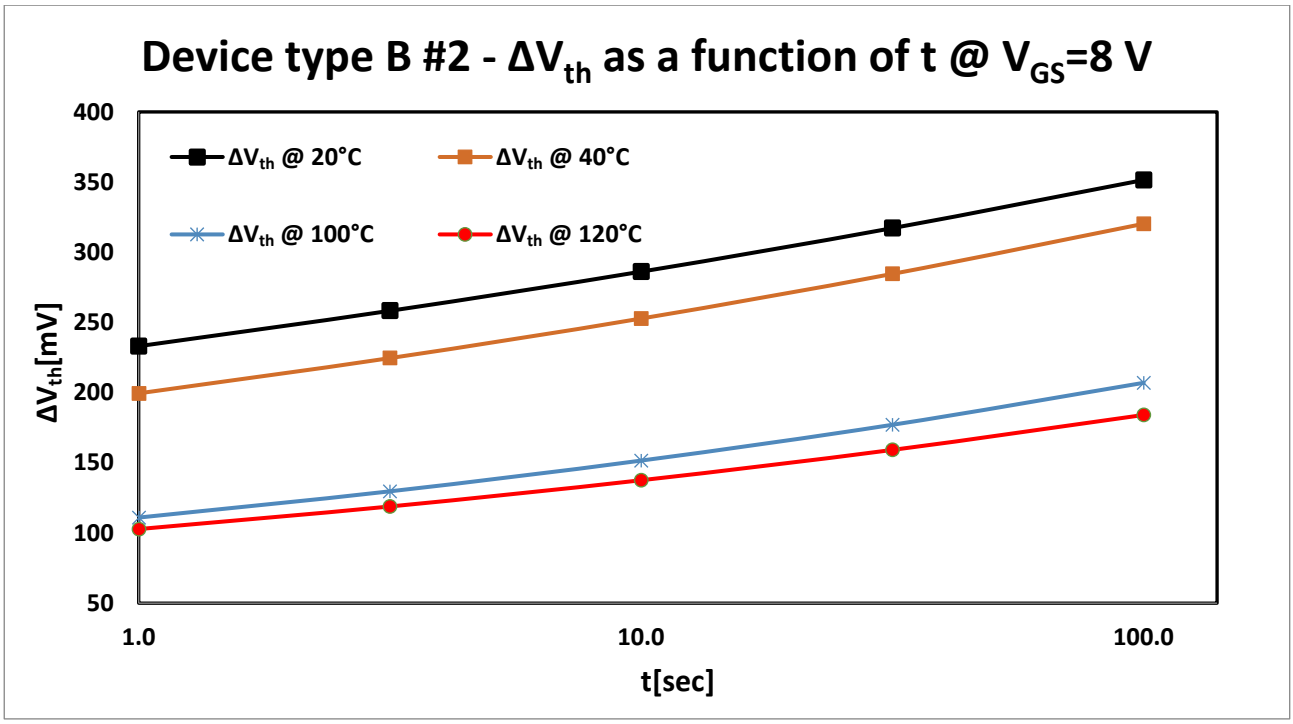



**Figure 4.3.5: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting $V_{GS}$ to 8 V for different temperatures.**

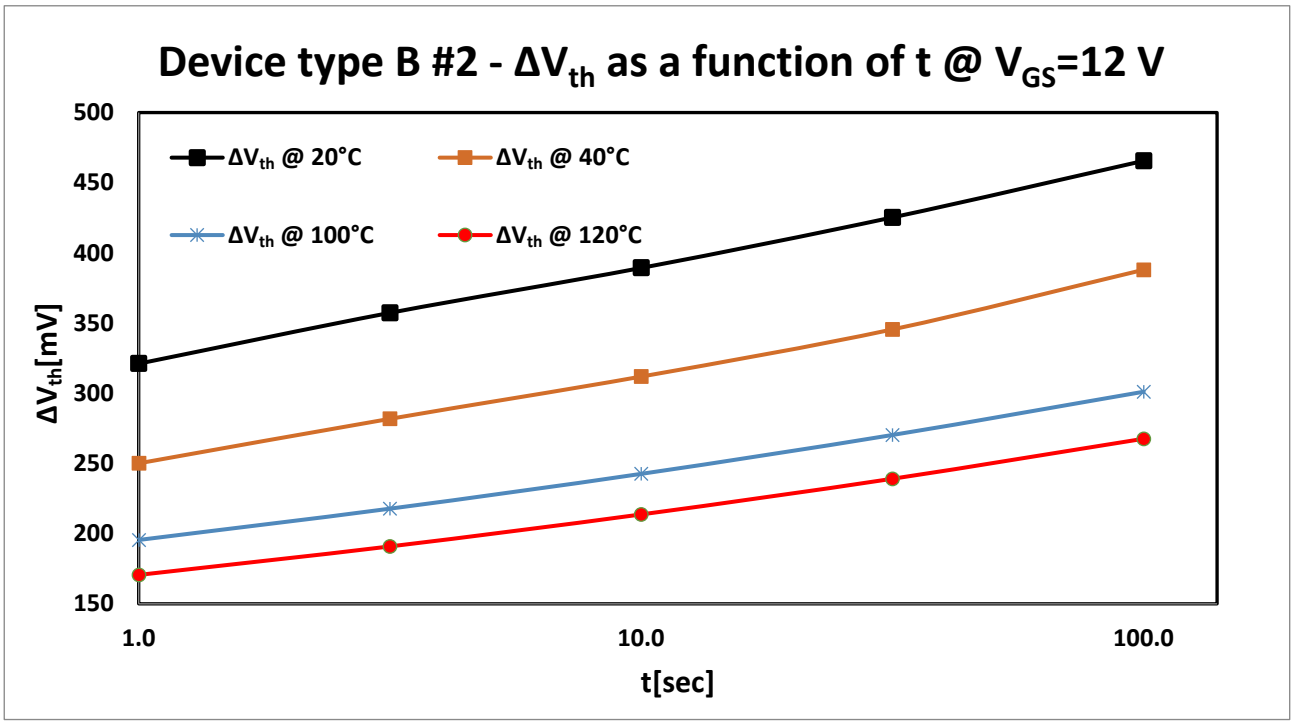



**Figure 4.3.6: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting $V_{GS}$ to 12 V for different temperatures.**

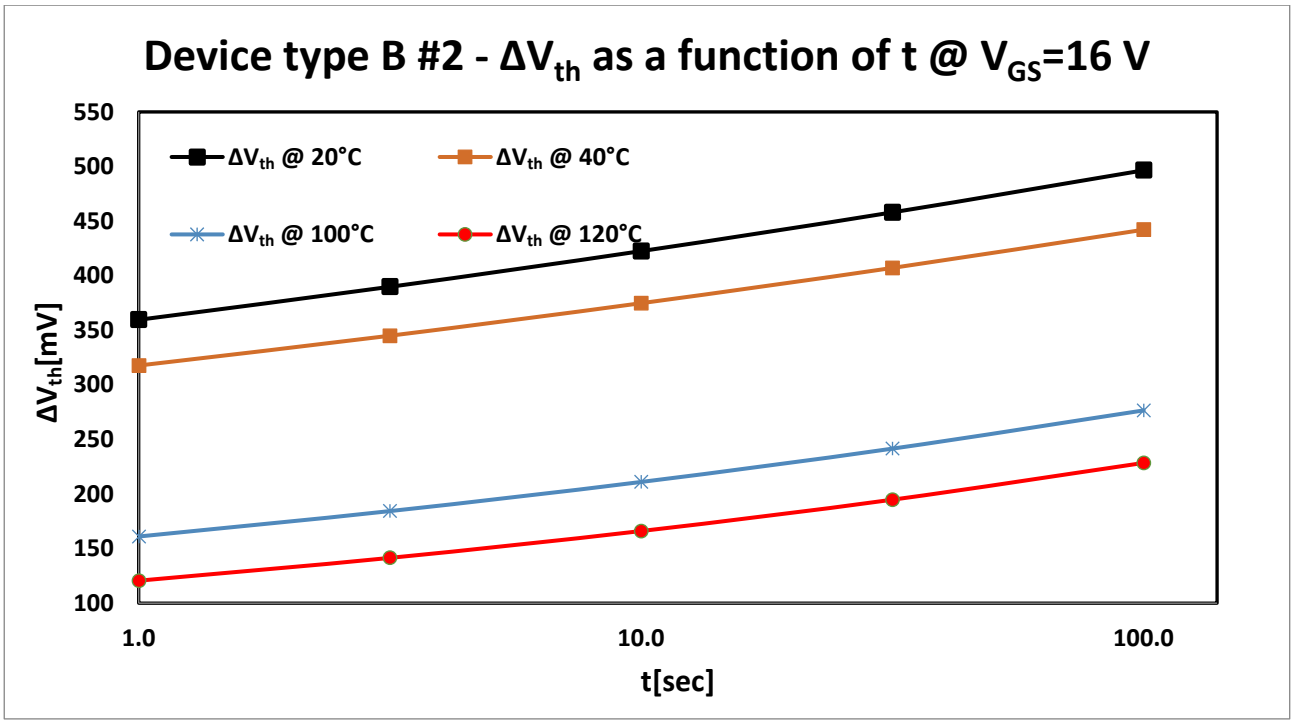



**Figure 4.3.7: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting $V_{GS}$ to 16 V for different temperatures.**

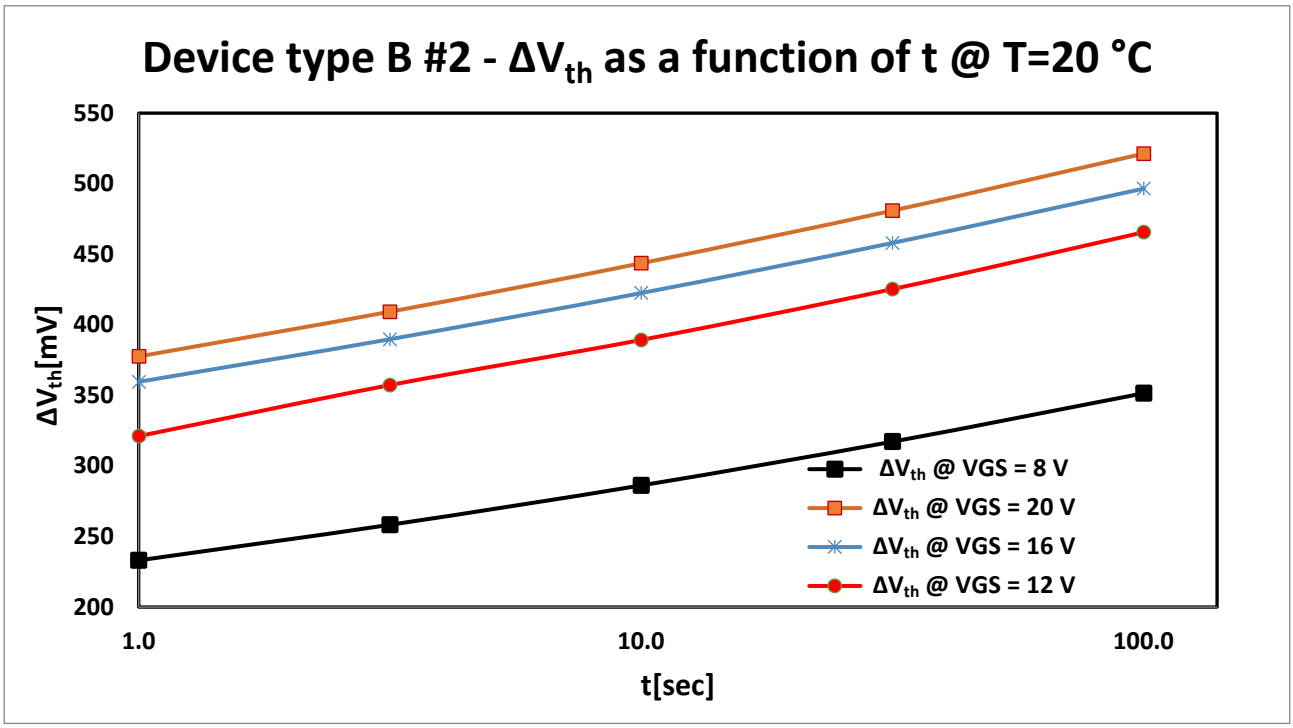



**Figure 4.3.8: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting T to 20°C for $V_{GS}$ equal to 8V, 12 V, 16 V and 20 V.**

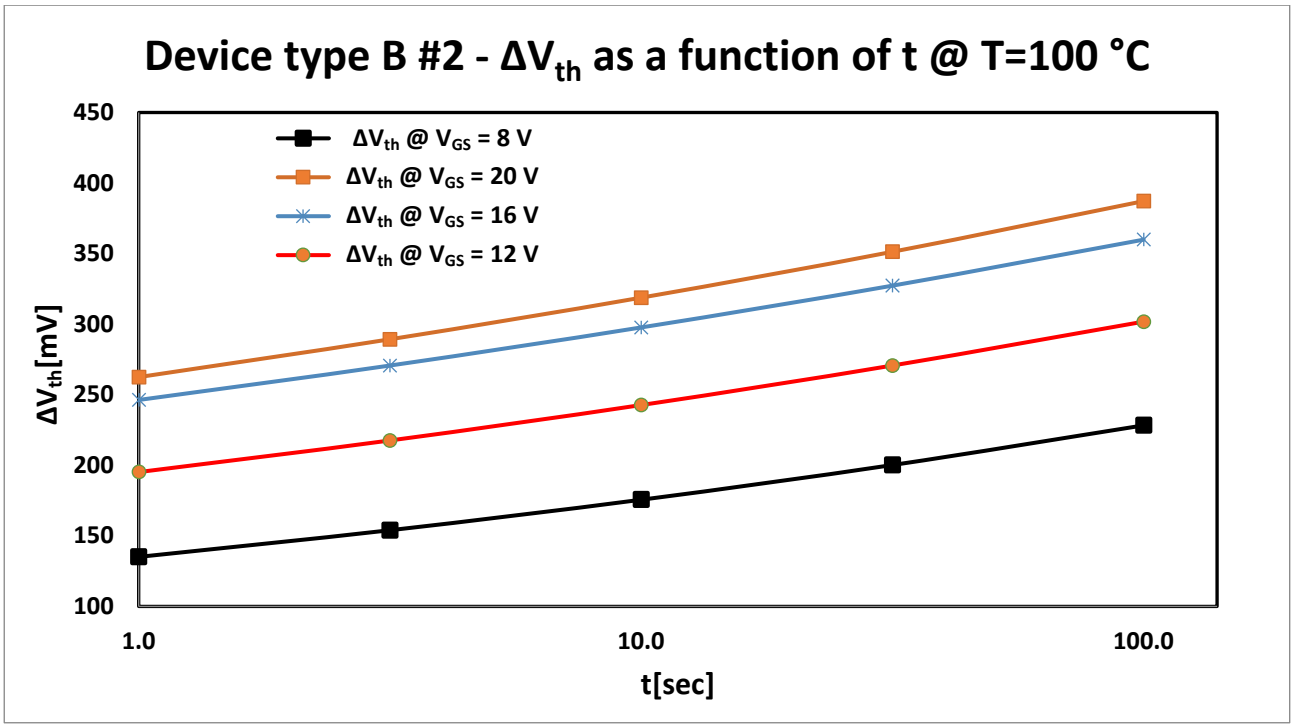



**Figure 4.3.9: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting T to 100°C for $V_{GS}$ equal to 8V, 12 V, 16 V and 20 V.**

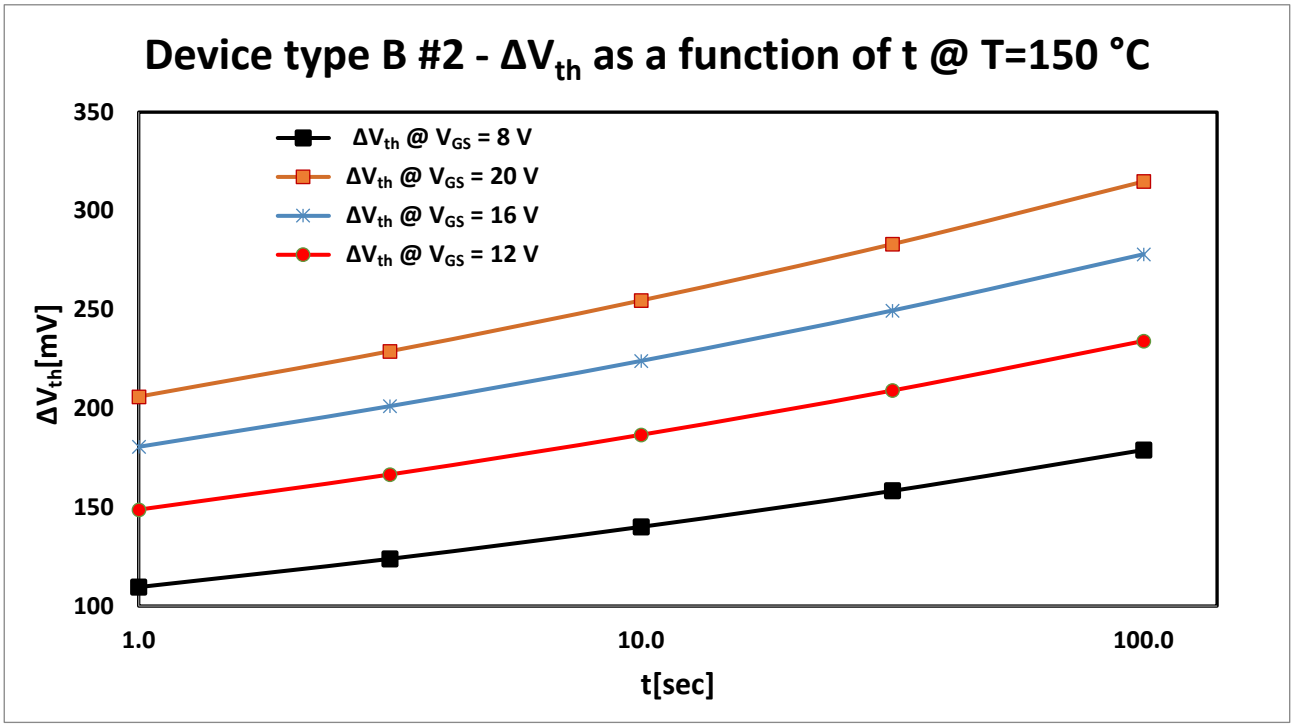



**Figure 4.3.10: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting T to 150°C for $V_{GS}$ equal to 8V, 12 V, 16 V and 20 V.**

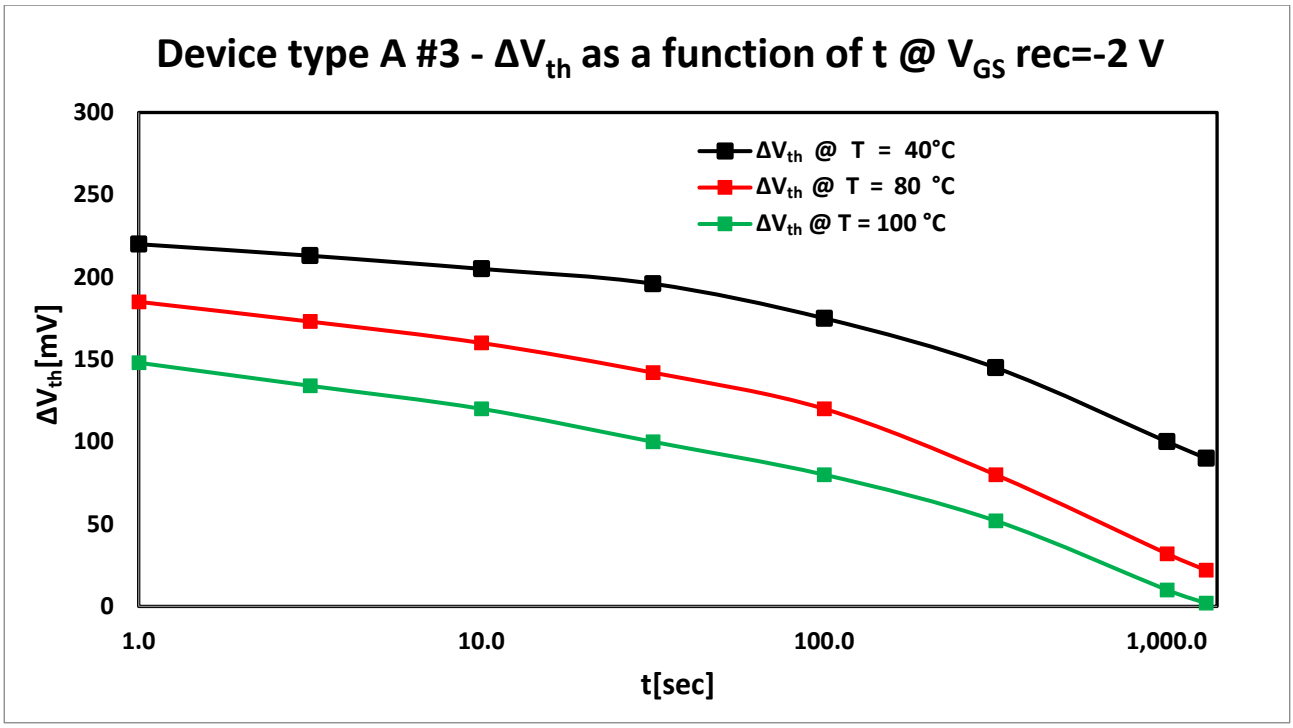



**Figure 4.3.11: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the recovery phase of piece 3 of the type A device by setting the $V_{GS}$ to -2V and varying the T from 40°C to 80°C (the $V_{GS}$ during the stress phase was set at 8 V).**

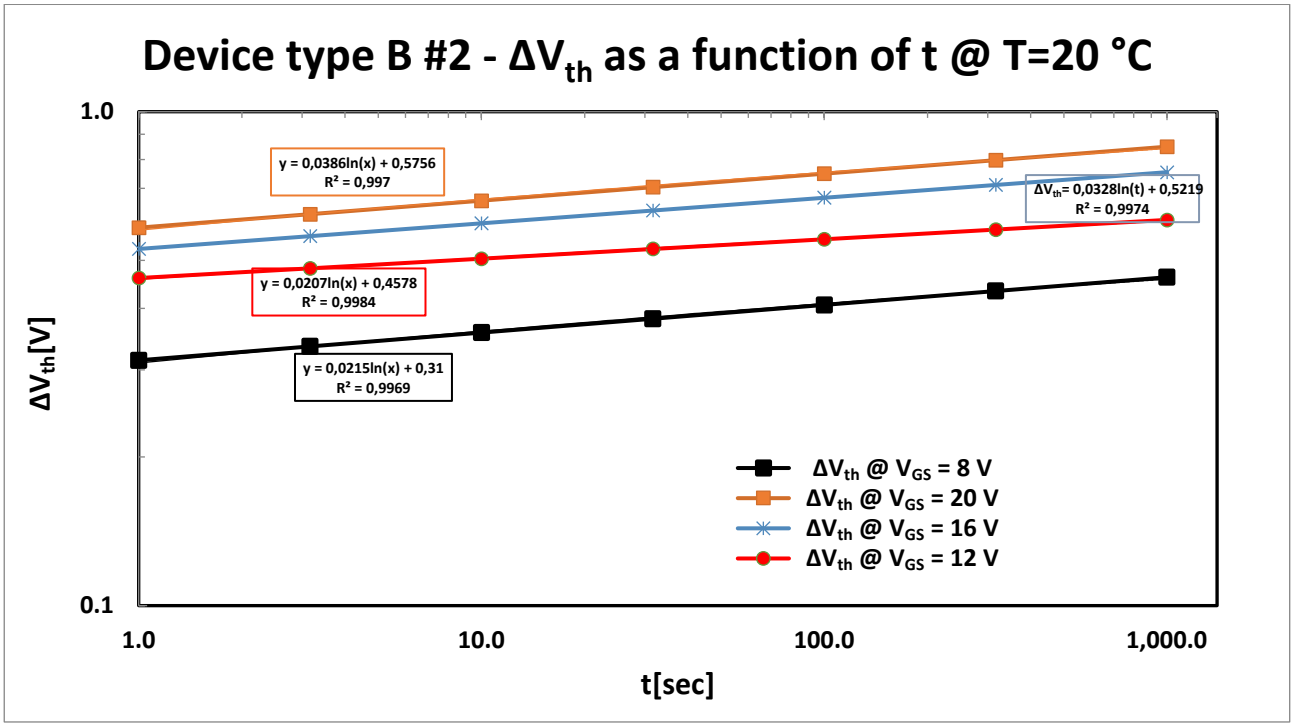



**Figure 4.3.12: Graph of $\Delta V_{th}$ as a function of time in logarithmic-logarithmic scale obtained during the stress phase and performed on piece 2 of the type B device by setting the T at 20°C for the $V_{GS}$ equal to 8 V, 12 V, 16 V and 20 V.**

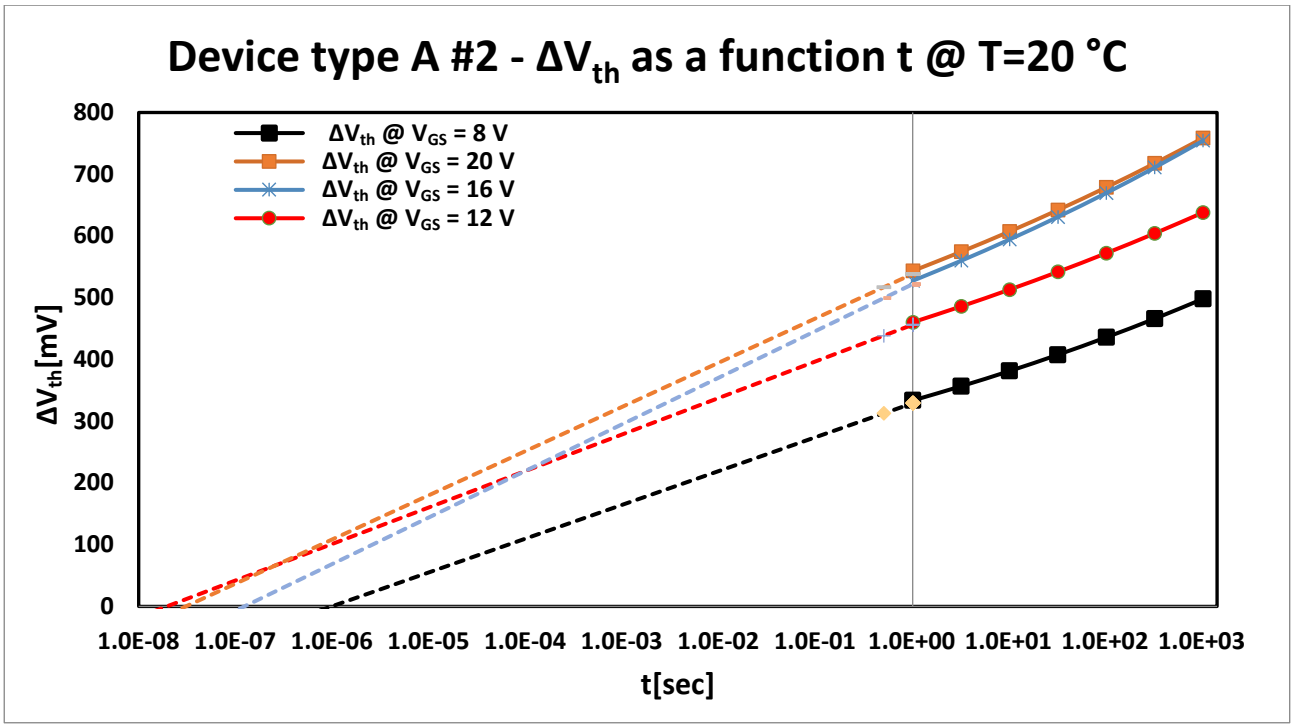



**Figure 4.3.13: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type A device by setting the T at 20°C for the $V_{GS}$ equal to 8 V, 12 V, 16 V and 20 V which allows to extrapolate the stress time in which no instability effect is observed.**

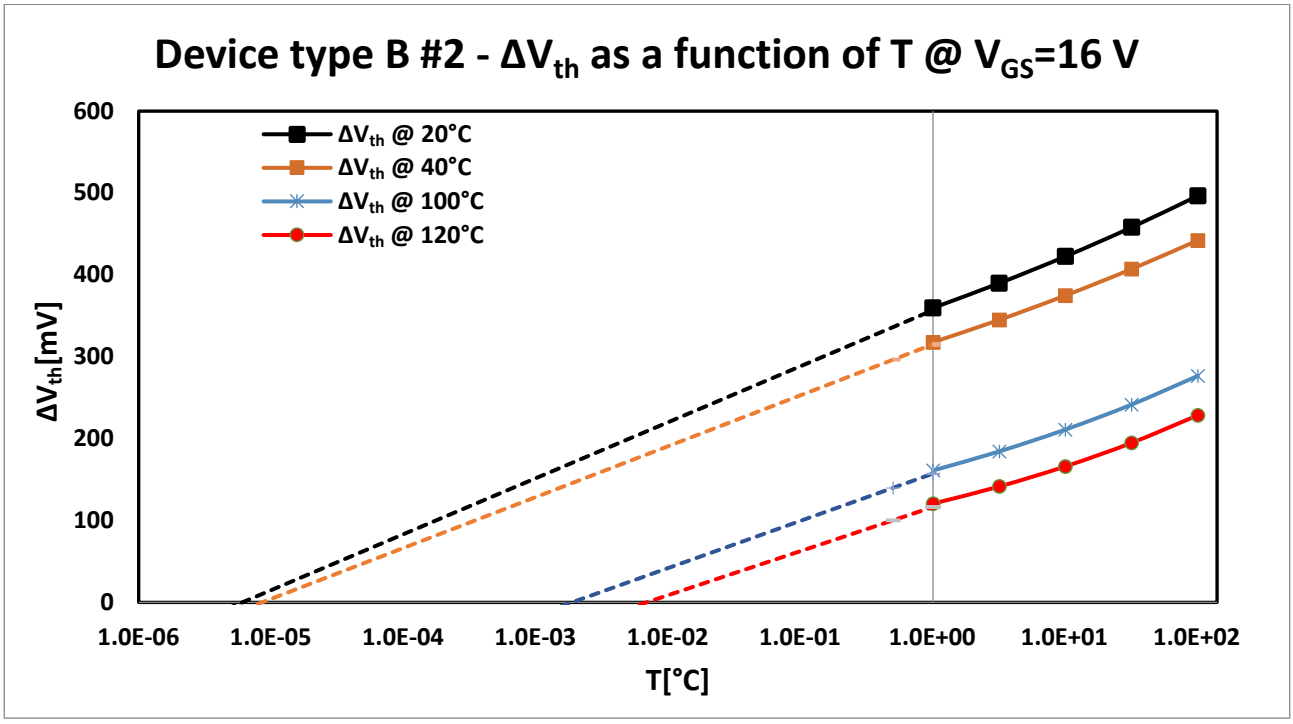



**Figure 4.3.14: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 2 of the type B device by setting the $V_{GS}$ at 16 V for the T equal to 20°C, 40°C, 100°C and 120°C which allows to extrapolate the stress time in which no instability effect is observed.**

If this condition is also applicable for SiC substrates, referring to the example of figure 4.3.14, the electrons have penetrated inside the oxide to fill the border traps up to about 20 Å after 1000 s due to the effect of the stress applied on the gate of the device. Therefore, based on these measurements, the thichness of the transition layer in the interface could be estimated even if, as will be discussed later, adequate spettoscopy analises will be performed to evaluete it exactly. However, the results obtained with spettroscopic analises could be compared with the same estimated with the Lelis method in order to validate the results. As shown in figure 4.3.2 and figure 4.3.3, much of the $\Delta V_{th}$ is immediately recovered before starting the recovery phase. By way of example, referring to the 20 V characteristic, the $\Delta V_{th}$ reaches the value of about 750 mV after the stress phase while at the beginning of the recovery phase it is possible to observe that the $\Delta V_{th}$ decreases down to the value of about 180 mV. Therefore, applying the same approch as Lelis et al. used previously, it is possible to estimate the time necessary to observe the beginning of the recovery of $V_{th}$ from the value reached at the end of the stress phase as shown in figure 4.3.15 for piece 2 of the type A device by setting T at 20°C. From this graph, it is possible to observe that the recovery process is very fast and, in any case, it is much faster than stress process because the $V_{th}$ starts the recovery for times that are reduced to the order of the femto seconds. Therefore, it is possible also to state that the emission time constants are much smaller than capture time constants as will be better understood later in this chapter.
Now, answers will be given to the questions mentioned earlier in the beginning of this chapter. First of all, why does $\Delta V_{th}$ increase by increasing the gate voltage during the stress phase? As seen in chapter 4.2 when discussing the hysteresis phenomenon of $V_{th}$, referring to the interface traps, when applying a higher $V_{GS}$, a higher $\Delta V_{th}$ are measured because the $E_F$ sweeps over to a larger portion of the SiC bandgap. Instead, from point of view of the border traps, the greater the energy provided by the gate potential, the greater the number of border traps involved in the charge exchange process with the substrate, thus, the greater the $\Delta V_{th}$. This phenomenon has also been observed experimentally by Grasser et al. [275] by performing an adequate time-dependent defect spectroscopy (TDDS) on MOSFET devices. The TDDS technique is an extension of the DLTS method in the Grasser's experiments in which spectral maps are introduced that visualize the capture-emission events of electrons from the traps, evaluating the intensity of the phenomenon, as a function of the capture-emission time constants connecting them to $\Delta V_{th}$. Grasser in his work demonstrates the strong gate bias dependence of the capture time constants during the stress phase by means of the spectral maps and,in particular, he notes that the greater the $V_{GS}$, the shorter the capture time constants, the greater the $\Delta V_{th}$. The answer to the second question concerning the acceleration of the release of electrons from the traps with the reduction of the gate voltage during the recovery phase is also explained by the experiments carried out by Grasser. Grasser observes from the spectral maps that when gate bias is reduced during the recovery phase, the emission times are shortened, thus, the electrons can be effectively removed from the oxide. In Grasser's work it is shown that the capture and emission time constants are distributed exponentially according to the Markov model conventionally described as a process that has two possible states which refer to full and empty traps. In addition, Grasser using the spectral maps notes that the capture and emission processes of electrons from traps are thermally activated. In practice, he observes that the higher the temperature, the shorter the capture and emission constant times. As will be discussed below, this phenomenon explains the surprising dependence on $\Delta V_{th}$ from temperature during the stress phase previously exposed. In fact, in order to observe the $\Delta V_{th}$ during the stress phase, it is important that the emission time constants of the electrons from the traps are greater or at least comparable to the delay in measurements imposed by the instrumentation.

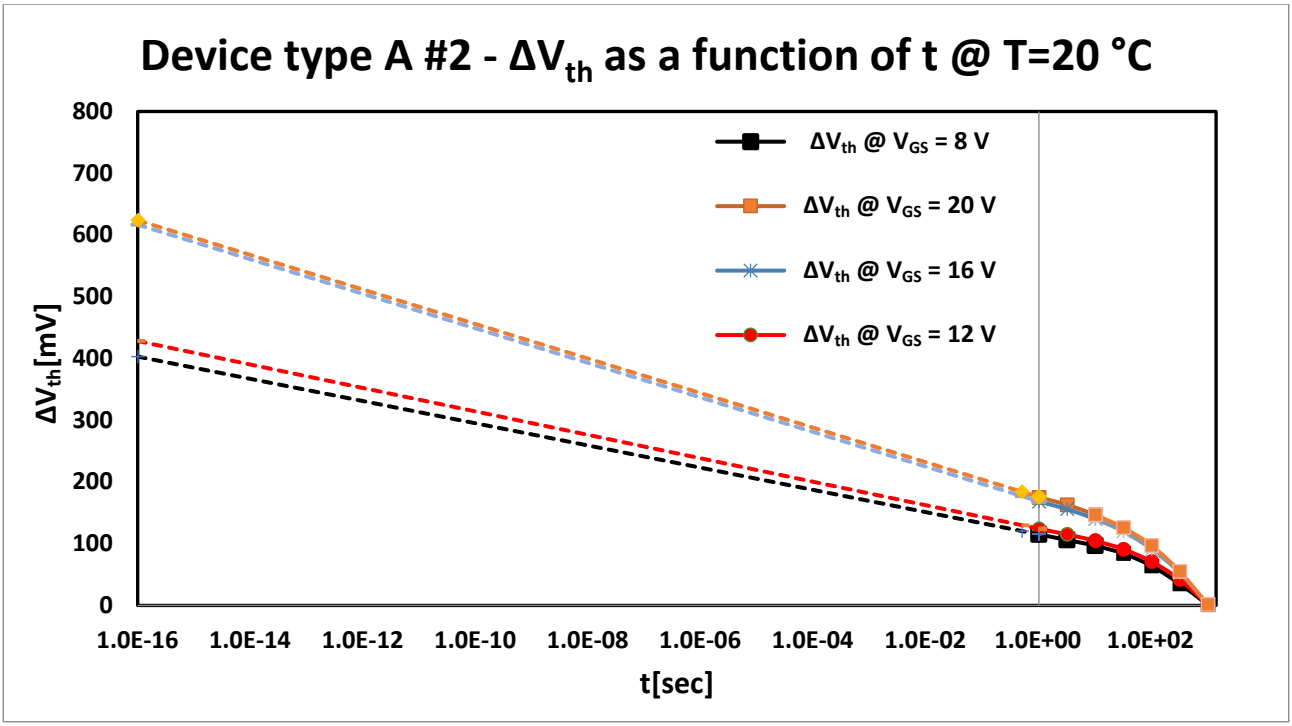



**Figure 4.3.15: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the recovery phase and performed on piece 2 of the type A device by setting the T at 20°C for the $V_{GS}$ equal to 8 V, 12 V, 16 V and 20 V which allows to estimate the time in which the $V_{th}$ starts the recovery.**

If a part of the electrons captured during the stress phase are released before the instrumentation detects the $\Delta V_{th}$ they cannot be monitored, thus, the measurement of the threshold voltage shift is less than the real correct value. When the BTI tests are performed at high temperatures, the capture and emission time constants of the electrons in the traps become much shorter than the same measured at room temperature and, thus, most of these processes are no longer observed and this has a significant impact in the measure of the $\Delta V_{th}$ because it is strongly reduced. The temperature also influences the $\Delta V_{th}$ measurements during the recovery phase. As the temperature increases, more traps are involved in the emission process than when the tests are performed at room temperature. In fact, even traps with usually longer emission time constants contribute to the $\Delta V_{th}$, thus, recovery may be slower [278]. However, in our experiments, this phenomenon is not so evident because $\Delta V_{th}$ at the end of the stress phase at lower temperatures is much higher than $\Delta V_{th}$ at higher temperatures. To better understand the temperature dependance of the BTI phenomenon, it is necessary to introduce the following assumptions based on the Reaction Diffusion theory, RD, and on the Arrhenius activation method of the individual defects time constants recently proposed [275], [279]. The BTI phenomenon is believed to be due to the creation of new crystallographic defects during the stress phase also due to the existence of precursor defects near the dielectric–semiconductor [280], [281]. During the creation of these defects one or more atomic bonds are broken and this leads a structural transformation of the reticule near the defects. The energy needed to break an atomic bond depends on the vibrational properties of the bond itself and, usually, to break the bond the more phonon energies must be added [282], [283]. The latter phenomenon leads to a temperature activation of the cross sections of the electrons which, according the classical physics, obeys the Arrhenius law. Now, according to Eq.(4.2.7), the time constants of the defects are proportional to the inverse of their cross-sections and, thus, they also depends strongly on the temperature as already seen in Eq. (4.2.9) and Eq. (4.2.10) for the capture and release events of a single border trap.

According to the work of Puschkarsky et al. [278], $\tau_{cn0}$ and $\tau_{en0}$ are equal to the value assumed by the time constant for an infinitely high temperature. The latter constant time value should be different for every single defect as assumed in the work of Toledano et al. [279] and, in particular, it should depend on the distance of the defect within the oxide from the interface. However, in the work of Nagumo et al. [284] there is no experimental evidence of a correlation between the depth of the defects within the oxide and the constant time and Grasser et al. hypothesize that this time constant is the same for all the defects [285]. In the Puschkarsky's work this time constant is estimated at $10^{-15}$ s [278]. Now, assuming the trap's energy barrier to be temperature independent, we can deduce that the time constant of the defect changes from one value, $\tau_{cn1}$, to another, $\tau_{cn2}$, when the temperature changes from $T_1$ to $T_2$. Therefore, starting from Eq. (4.2.9), it is possible to obtain:

$$\tau_{cn2}(T_2) = \tau_{cn0}\left(\frac{\tau_{cn1}}{\tau_{cn0}}\right)^{\left(\frac{T_1}{T_2}\right)} \tag{4.3.2}$$

and, for electron emission events, considering Eq. (4.2.10), it is possible to obtain:

$$\tau_{en2}(T_2) = \tau_{en0}\left(\frac{\tau_{en1}}{\tau_{en0}}\right)^{\left(\frac{T_1}{T_2}\right)} \tag{4.3.3}$$

with:

$$\tau_{cn0} = \tau_{en0} = 10^{-15}\text{s} \tag{4.3.4}$$

Therefore, by setting a reference temperature, in this case $T_1$, and the respective time constants, $\tau_{cn1}$ and $\tau_{en1}$, it is possible to obtain any other capture and emission constant times, $\tau_{cn2}$ and $\tau_{en2}$, given the reference one as obtained from Pobegen et al. [286]. In practice, from Eq. (4.3.2) and Eq. (4.3.3), if $T_2$ is greater than $T_1$, $\tau_{cn2}$ and $\tau_{en2}$ become shorter than $\tau_{cn1}$ and $\tau_{en1}$ and, conversely, if $T_2$ is less than $T_1$, $\tau_{cn2}$ and $\tau_{en2}$ become larger than $\tau_{cn1}$ and $\tau_{en1}$ as observed in the experiments of Grasser by means of spectral maps.

In the previous chapter 4.2, with reference to figure 4.2.27, it was said that the border traps could be charged more than they are discharged during long-term operation and this can lead to a gradual drift of the $V_{th}$ with a conseguente negative impact on the operation of the application. However, the power MOSFETs slownly heat up because they dissipate energy during the conduction and switching phases, thus, increase their temperature. As just explained, the higher T the shorter the emission constant times of the electrons from the traps, thus, the drift of the $V_{th}$ is greatly attenuated by this phenomenon.

In BTI tests, $\Delta V_{th}$ is determined by the collective response of a very large number of defects that behave according to a first-order process as described in Eq. (3.1.4.2) with the time constants described by Eq. (4.2.9) and Eq. (4.2.10) and not from a single defect. According to the work of Pobegen and Grasser [273], based of the RD theory, the energy barriers of traps in Eq. (4.2.9) and Eq. (4.2.10) are distributed according to a Gaussian curve because they follow the form of the distribution of the dissociation energies of the atoms which compose the defect, thus, the time constants have a log-normal distribution. Therefore, to estimate $\Delta V_{th}$, it is possible to introduce a log-normal distribution both for the stress phase, when the electrons are captured by the border traps, and for the recovery phase, when the electrons are released from the border traps, such as [285]:

$$\Delta V_{th}(t) = \frac{\Delta V_{th}^{max}}{2}\,\text{erfc}\left(-\frac{KT\ln\frac{t}{\tau_0} - \boldsymbol{\mu_c}}{\boldsymbol{\sigma_c}\sqrt{2}}\right) \tag{4.3.5}$$

$$\Delta V_{th}(t) = \frac{\Delta V_{th}^{max}}{2}\,\text{erfc}\left(\frac{KT\ln\frac{t}{\tau_0} - \boldsymbol{\mu_e}}{\boldsymbol{\sigma_e}\sqrt{2}}\right) \tag{4.3.6}$$

where the Eq. (4.3.5) refers to the stress phase while Eq. (4.3.6) refers to the recovery phase, $\Delta V_{th}^{max}$ is the maximum shift of $V_{th}$, $\boldsymbol{\mu_c}$ and $\boldsymbol{\mu_e}$ are the mean values of the capture and emission activation

energies with their standard deviations $\boldsymbol{\sigma_c}$ and $\boldsymbol{\sigma_e}$. Finally, erfc is the complementary error function usually given by:

$$\mathrm{erfc}(z) = 1 - \mathrm{erf}(z) = \frac{2}{\sqrt{\pi}} \int_z^{\infty} e^{-z^2}\, dz \tag{4.3.7}$$

It is important to underline that the $\Delta V_{th}^{max}$ allows to estimate the total number of precursor defects inside the oxide accessible at a given gate voltage. Therefore, in order to obtain $\Delta V_{th}^{max}$, the BTI stress must be performed for a very long time in the stress phase to reach the saturation of the curve as shown in figure 4.3.16. By way of example, in this figure is shown that during the stress phase, to saturate the $\Delta V_{th}$ curves, it is necessary to apply a stress time of up to about $10^4$ s. Furthermore, it is possible to observe that each $\Delta V_{th}$ curve is well fitted from Pobegen's log-normal distributions according Eq. (4.3.5) by optimizing the parameters $\boldsymbol{\mu_c}$ and $\boldsymbol{\sigma_c}$ using the OLS method. It is important to emphasize that, according to Pobegen's study, these parameters are not affected by the change in gate voltage. In fact, the estimated $\boldsymbol{\mu_c}$ is equal to 0.83 eV the $\boldsymbol{\sigma_c}$ is equal to 0.15 eV and these are values quite similar to those obtained by Puschkarsky in her experiments. Based on the results obtained on piece 7 of the type A device, as shown in figure 4.3.16, it is possible estimate the total number of accessible precursor defects present in the oxide as function of $V_{GS}$. In particular, we obtain $4.3 \times 10^{11}$ defects $cm^{-2}$ for $V_{GS}$ equal to 8 V, $4.7 \times 10^{11}$ defects $cm^{-2}$ for $V_{GS}$ equal to 12 V, $5.3 \times 10^{11}$ defects $cm^{-2}$ for $V_{GS}$ equal to 16 V and $5.8 \times 10^{11}$ defects $cm^{-2}$ for $V_{GS}$ equal to 20 V. A similar analysis can be performed considering the recovery phase taking into account Eq. (4.3.6). By way of example, in figure 4.3.17 the results obtained for piece 5 of type A device are shown by fixing the T at 120°C. As it is possible to see in this figure, the $\Delta V_{th}$ curve fits well to the log-normal distribution of Pobegen according to Eq. (4.3.6) by setting $\boldsymbol{\mu_e}$ equal to 0.9 eV and $\boldsymbol{\sigma_e}$ equal to 0.35 eV. On the basis of these experimental results and the previous ones shown in figure 4.3.13, given the works of McLean and Oldham, the thickness of the transistion layer can be estimared at around 25 Å. Puschkarsky et al. in their work [278] introduce the concept of CET maps, Capture-Emission Time, in which the capture and emission constant times and the capture and emission activation energies are modeled according two bivariate Gaussian distributions [285]. In the Puschkarsky's work, the emission activation energies, $E_{en}$, increase with growth of capture activation energies such as:

$$E_{en} = E_{cn} + \Delta E_{en} \tag{4.3.8}$$

where $\Delta E_{en}$ is an increase factor of the $E_{cn}$ to obtain the $E_{en}$. The variance of the emission activation energy, $\boldsymbol{\sigma_e^2}$, can be obtained from $\boldsymbol{\sigma_c^2}$ as [287]:

$$\boldsymbol{\sigma_e}^2 = \mathbf{r}\,\boldsymbol{\sigma_c}^2 + \boldsymbol{\sigma_{\Delta e}}^2 \tag{4. 3.9}$$

**r** is a correlation parameter used to calculate the activation energy and it varies between 0 and 1 while $\boldsymbol{\sigma_{\Delta e}^2}$ is the variance related to $\Delta E_{en}$. The correlation parameter, **r**, is equal to 1 for the recoverable component of the $\Delta V_{th}$ and is equal to 0 for the permanent component. Therefore, Puschkarsky calculates the charged trap density from the bivariate distribution of the activation energies, $g(E_{cn}, E_{en})$, such as [278], [287]:

$$g(E_{cn}, E_{en}) = \frac{1}{2\pi\boldsymbol{\sigma_c}\boldsymbol{\sigma_e}} e^{\left[-\frac{(E_{cn}-\boldsymbol{\mu_c})^2}{2\boldsymbol{\sigma_c}^2} - \frac{(E_{en}-rE_{cn}+\boldsymbol{\mu_{\Delta e}})^2}{2\boldsymbol{\sigma_{\Delta e}}^2}\right]} \tag{4.3.10}$$

where $\boldsymbol{\mu_{\Delta e}}$ is the mean value of the increase in the emission activation energies from the capture activation energies. Starting from Eq. (4.3.10), Puschkarsky obtain the CET map and energy activation map for her experiments as shown in figure 4.3.18. From the Puschkarsky's CET map it is possible to see that most border traps have very short capture and emission time constants also well below 1 μs. Furthermore, border traps which have short capture constant times also have much shorter emission constant times as obtained from the results of the experiments carried out in this work. This phenomenon leads to a very fast recovery of a substantial part of $V_{th}$ when the stress phase ends as observed during the recovery phase in our BTI tests.

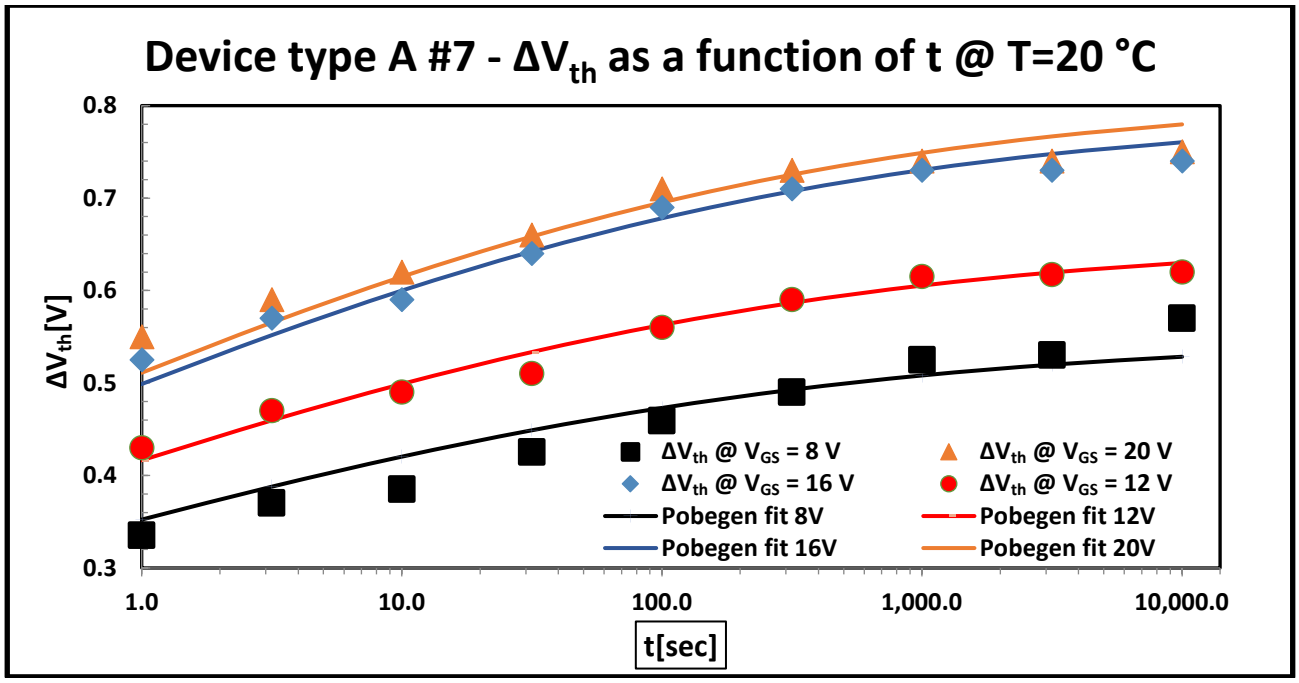



**Figure 4.3.16: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 7 of the type A device by setting T to 20°C for $V_{GS}$ equal to 8V, 12 V, 16 V and 20 V for a stress time which reaches to 10000 s in order to obtain the saturation of the curves showing the fitting obtained through the Pobegen method based on Eq. (4.3.5).**

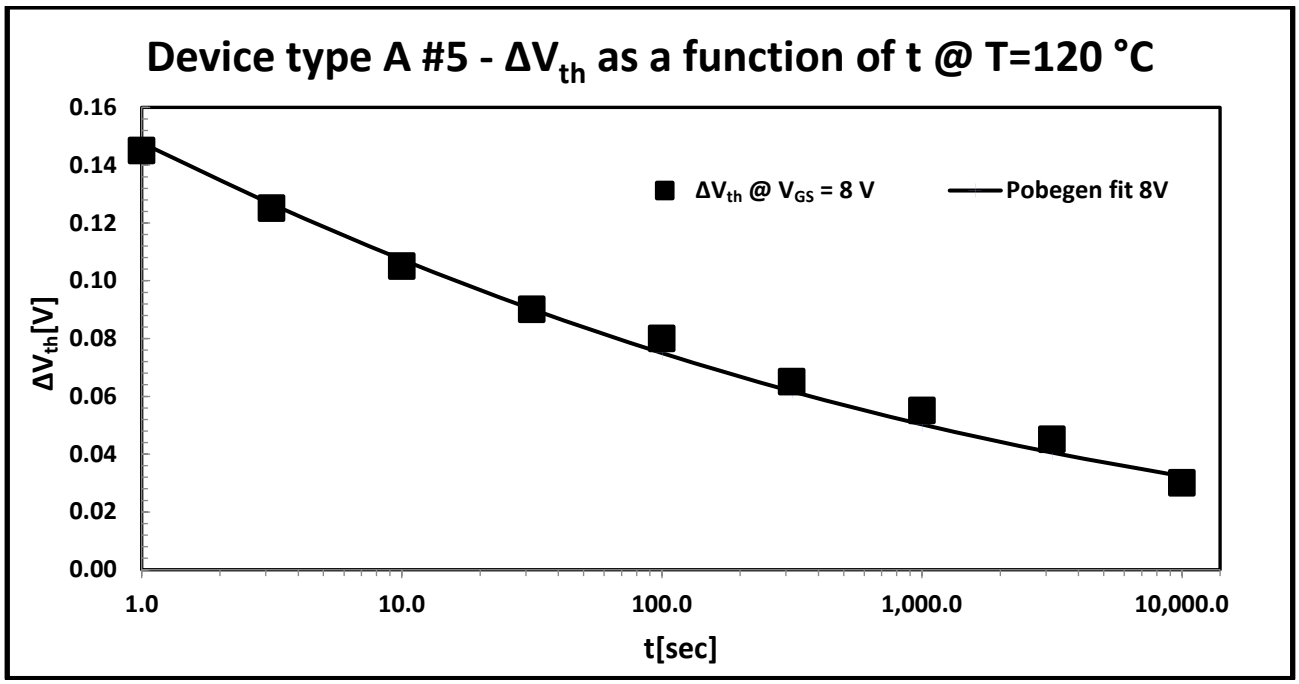
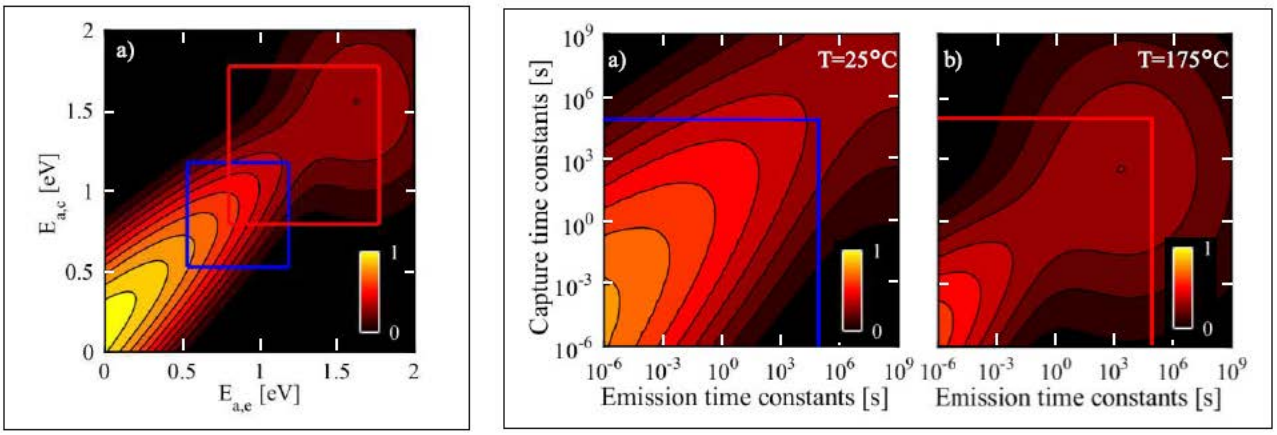



**Figure 4.3.17: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the recovery phase and performed on piece 5 of the type A device by setting $V_{GS}$ at -2 V in the recovery phase and T to 120°C for $V_{GS}$ equal to 8V in the stress phase for a time up to 10000 s which shows the fitting obtained through the Pobegen method based on Eq. (4.3.6).**




a) b)

**Figure 4.3.18: Charts extrapolated from the work of Puschkarsky's et al. [278]: a) map of the activation energies; b) capture and emission time constants at T = 25◦C and T = 175◦C.**

Figure 4.3.18b also shows that, due to the thermal activation phenomenon, the capture and emission time constants of the border traps decrease drastically increasing the T from 25°C to 175°C and, as previously mentioned, this explain the surprising dependence of the $\Delta V_{th}$ from temperature seen in our BTI tests.

Previously, it was said that the stress and recovery phases of the $\Delta V_{th}$ behaves roughly in accordance with a power law curve, in fact, in figure 4.3.12, the $\Delta V_{th}$ as a function of time was obtained considering a logarithmic-logarithmic scales. Therefore, to better study the $\Delta V_{th}$ evolution, it is possible to evaluate the trapping rate parameter defined as:

$$\mathbf{b} = \frac{\partial \log(\Delta V_{th})}{\partial \log(t)} \tag{4.3.11}$$

When **b** is constant by changing the stress time than the $\Delta V_{th}$ evolution follows a classic power law function [288]. By way of an example, in figure 4.3.19, parameter **b** is measured during the stress phase by setting the $V_{GS}$ at 8 V and the T at 20°C for the piece 2 of the type A device. As shown in the latter figure, **b** decreases slightly increasing the stress time and this implies that the $\Delta V_{th}$ does not follow a perfectly power law. Now, to better explain this experimental result, in figure 4.3.20 **b** is obtained as a function of $\Delta V_{th}$ for the same piece 2 under different conditions of $V_{GS}$ and T. It is important to underline once that the number of the accessible border traps is directly proportional to the $\Delta V_{th}$ as indicated in eq. (4.2.1), thus, from the graph in figure 4.3.20 it is also possible to highlight the correlation that exists between the same **b** and the number of traps involved in the process during the stress phase. From the experimental results shown in this figure, it is understood that there is a universal decreasing behaviour of the charging rate as a function of the number of filled traps independent of the stress time, the stress voltage, the temperature and this leads us to believe that the probability that an electron can be trapped is associated with the number of empty traps available in the time window analysed. Previously, it has been shown that the $\Delta V_{th}$ as a function of the time during the BTI tests can be theoretically simulated by log-normal distributions as proposed by the Pobegen method according to Eq. (4.3.5) and Eq. (4.3.6). Now, it is possible to demonstrate that the same $\Delta V_{th}$ function obtained during the stress phase in the BTI tests can be simulated with a semi-empirical method proposed by Zafar et al. [289]. The model predicts that the threshold voltage increases with a power law dependence on the stress time and on the injected charge carrier density in the initial stages of stressing. Zafar's method assumes a continuous distribution of the capture cross sections.

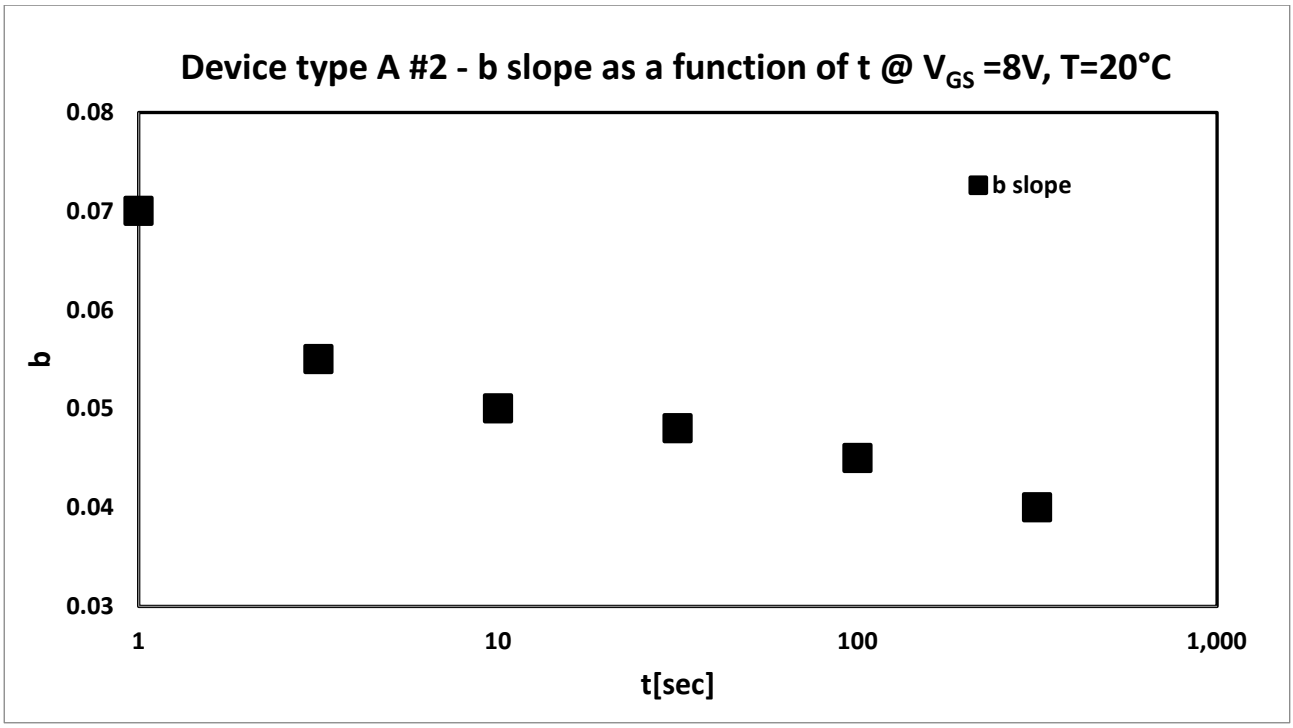



**Figure 4.3.19: Trapping rate parameter b measured during the stress phase for the piece 2 of the type A device by applying a $V_{GS}$ of 8 V and setting the T at 20° C.**

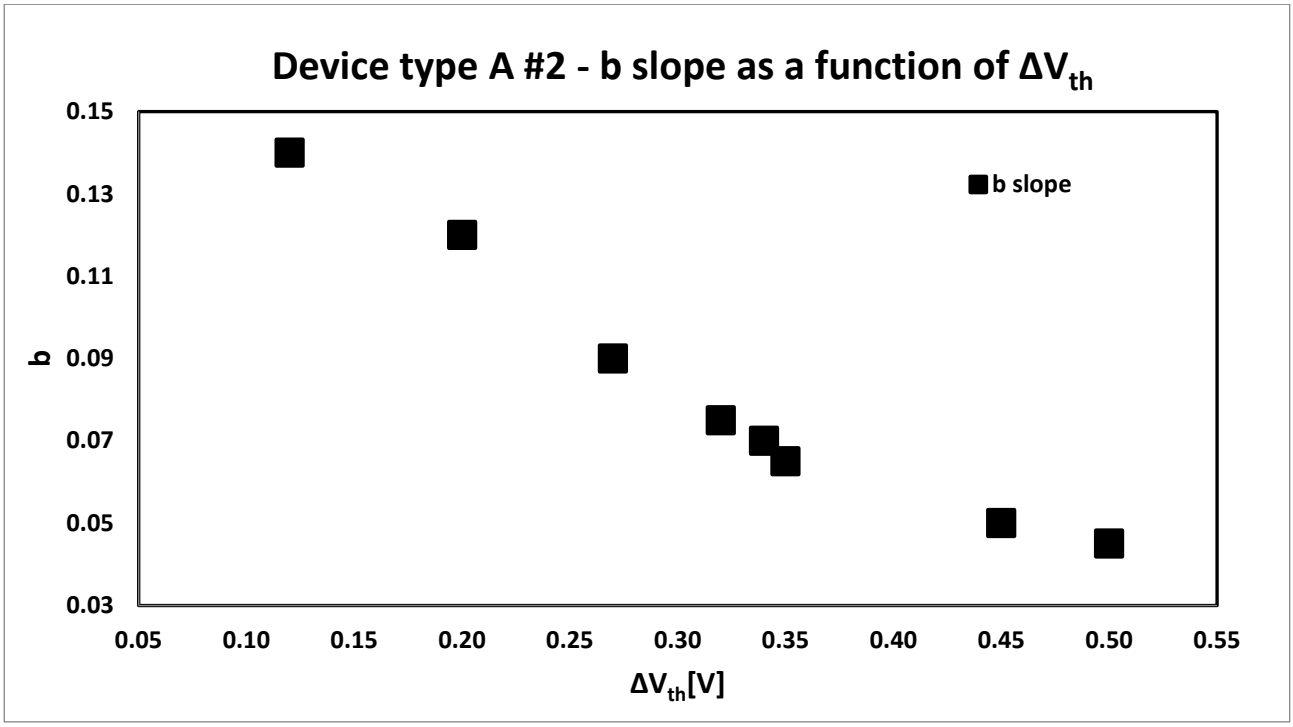



**Figure 4.3.20: Trapping rate parameter b measured during the stress phase for the piece 2 of the type A device as a function of $\Delta V_{th}$ at different stress voltages and temperatures applied.**

As already shown in figure 4.3.19, parameter **b** decreases sligtly increasing the stress time but, in any case, by way of a example, it is possible to assume it remains constant concluding that no new traps are created during stressing. In Zafar's experiments the $\Delta V_{th}$ and the density of the gate current are measured as a function of the stress time. Zafar notes by the experiments that the gate current density decreases during BTI tests with a power law dependence such as:

$$J = J_0 t^{-\alpha t} \tag{4.3.12}$$

Finally, simplifying, Zafar obtains a law that relates the $\Delta V_{th}$ to the stress time such as:

$$\Delta V_{th}(t) = \Delta V_{th}^{max}\left[1 - e^{-\left(\frac{t}{\tau_0}\right)^{\gamma}}\right] \tag{4.3.13}$$

$\gamma$ and $\tau_0$ are empirical parameters introduced in the Zafar model. By way of a example, figure 4.3.21 shows the results of the $\Delta V_{th}$ as a function of the stress time during the BTI tests for the piece 7 of type A device by setting the T at 100°C and for different values of $V_{GS}$ and the relative curves that fit the real data obtained by applying the semi-empirical method of Zafar. As it is possible to see from this graph, even in the latter case, the real data and curves obtained from the model proposed by Zafar correspond. The estimated values for the empirical parameters of Zafar are shown in the Tab. 4.3.1.

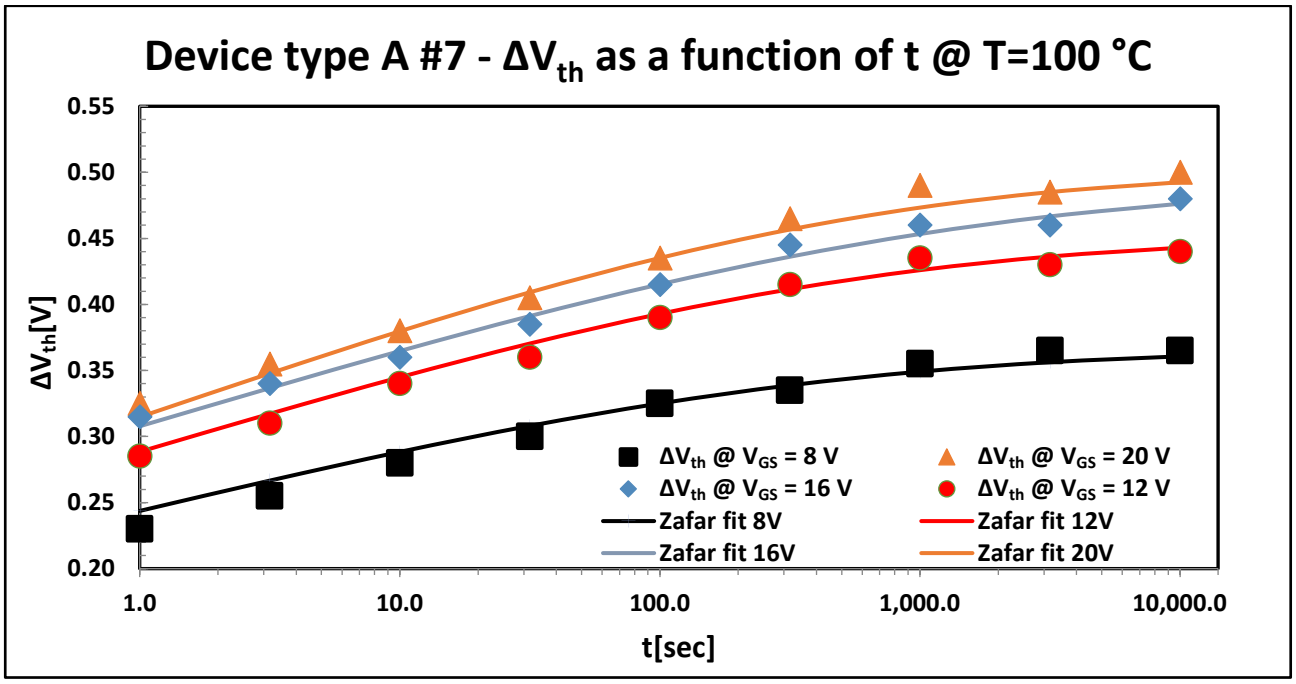



**Figure 4.3.21: Graph of $\Delta V_{th}$ as a function of time in logarithmic-linear scale obtained during the stress phase and performed on piece 7 of the type A device by setting T to 100°C for $V_{GS}$ equal to 8V, 12 V, 16 V and 20 V for a stress time which reaches to 10000 s in order to obtain the saturation of the curves showing the fitting obtained through the semi-empirical Zafar method based on Eq. (4.3.13).**

Tab. 4.3.1: Estimated values for the empirical parameters of Zafar related to the figure 4.3.21.

| | 8 V | 12 V | 16 V | 20 V |
|---|---|---|---|---|
| | | | | |
| $\Delta V_{th}^{max}$ [V] | 0.365 | 0.451 | 0.490 | 0.500 |
| $\tau_0$ [s] | 0.528 | 0.853 | 1.081 | 1.045 |
| $\gamma$ | 0.151 | 0.152 | 0.139 | 0.157 |

## 4.4 Characterization and Modeling of BTI in SiC MOSFETs by TCAD simulations

In the last two chapters, the SiC power MOSFETs under test have been investigated by performing two different types of measurements, the hysteresis between the upward and the downward swept and the positive bias temperature instability, PBTI, at different temperatures. It has already been said that the characterization of the hysteresis phenomenon of the transfer characteristics of the power MOSFETs better analyse the interface traps because they are fast traps and allow to evaluate the dynamics in the switching phase. Instead, the characterization of the PBTI phenomenon of power MOSFETs performed with measurements at long stress times can reveal the role of an additional degradation of the interface due to the border traps. Therefore, in order to fully understand the role played of both mechanisms, some simulations performed with TCAD have been performed to reproduce the experimental results because it has been demonstrated to be a comprehensive tool [290]. In particular, the Synopsys TCAD solver was used to perform simulations on a power MOSFET prototype to implement the RD model which was already discussed in chapter 4.3. In fact, it emphasizes the physical aspects of the interface degradation and recovery processes in the presence of BTI phenomena [291], [292]. Therefore, the experimental results obtained previously in the hysteresis measurements and PBTI analysis on the devices tested and carried out at different temperatures were used to configure and calibrate the TCAD simulator to explain, only from a qualitative point of view, the anomalous dependence on the temperature of the $V_{th}$ shift. First of all, based on the experimental results previously obtained, the mean value of the hysteresis amplitude in $\Delta V_{th}$ evaluated by setting $I_{DS}$ at 5 mA in function of the mean value of $\Delta V_{th}$ induced by the PBTI stress by setting $V_{GS}$ at 20 V and with a stress time of 1 s are shown in figure 4.4.1. The two phenomena exhibit a similar temperature dependence and are strongly correlated, this suggests that the same physical mechanism is responsible for them. Now, due to the lack of information on the specific technology of the tested SiC power MOSFETs, by way of as example, the data published on a similar device have been used to carry out the simulation. In practice, a 4H-SiC power MOSFET with a p-body retrograde profile having a breakdown voltage of 1.3 kV was used as reference as proposed in the work of Fujihira et al. [293]. The TCAD simulation was carried out using the geometric description of the device and the doping profile of the channel taken from Fujihira's work as shown in Fig. 4.4.2. Material-specific models for the incomplete ionization and the channel mobility, accounting for the role of Coulomb scattering, surface roughness and interface charge, have been adopted in the TCAD setup to investigate the device characteristics. The physical models were used with default parameters present in the TCAD simulator. The profile of the interface traps was extracted by comparing the simulated and measured transfer characteristics at two different $V_{DS}$ with reference to the density of the traps in the upper half of the SiC bandgap, as shown in figure 4.4.3. By way as example, these traps have been classified as acceptors, thus, when the traps capture the electrons they are negatively charged and degrade the channel's mobility. The extracted $D_{it}$ shows an exponential tail near the edge of the conduction band in agreement with what has been observed in the SiC devices as indicated in the references [64] and [294] and shown in figure 4.4.4. Fast transient defects mostly attributed to the interface traps were modeled in the TCAD simulator by means of further Gaussian distribution of acceptor-like traps at the $SiC/SiO_2$ interface with a peak density of $6x10^{11}$ $cm^{-2}eV^{-1}$ at 0.42 eV from the valence band as shown in Fig. 4.4.4. The cross sections of these traps have been calibrated to obtain trapping and releasing effects of the stress ramps in the range of 0.1 to 1 s as applied in our experimental measurements.

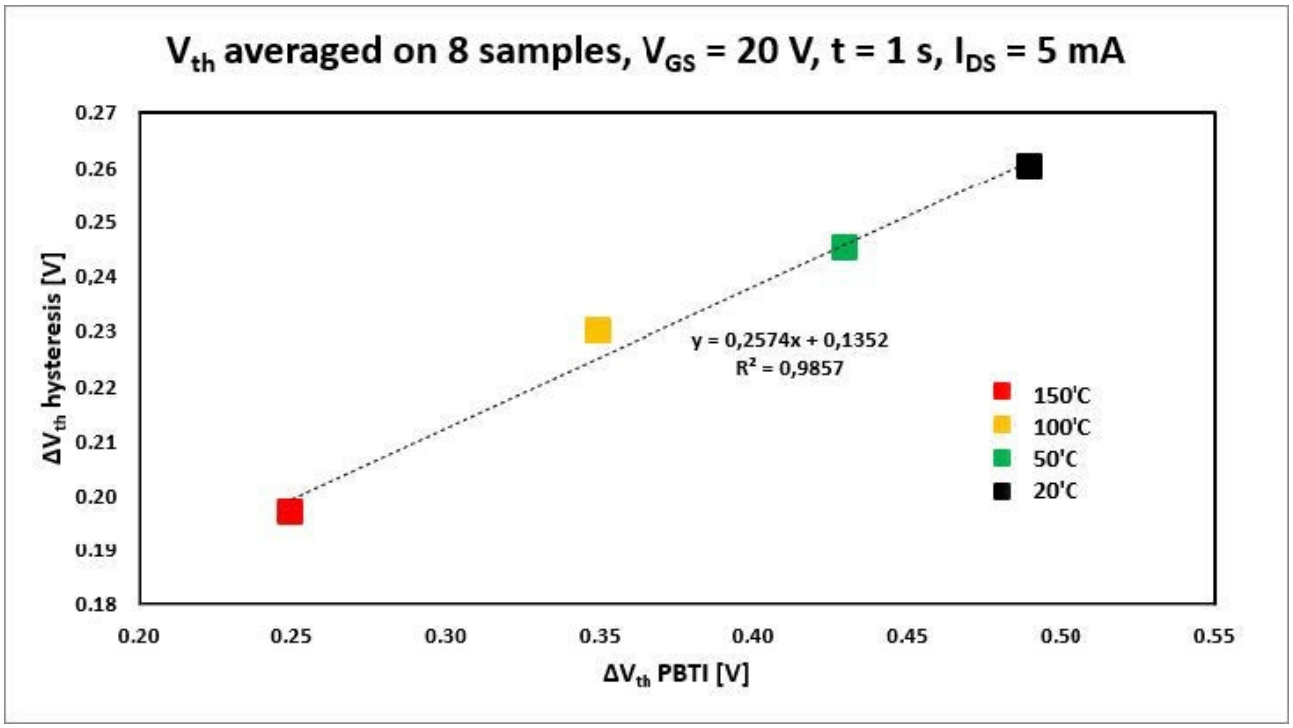



**Figure 4.4.1: Average value of $\Delta V_{th}$ due to hysteresis evaluated at $I_{DS}$ = 5 mA with respect to the average value of $\Delta V_{th}$ due to the PBTI by setting the $V_{GS}$ to 20 V and the stress time to 1 s measured on 8 samples of type A devices at different temperatures.**

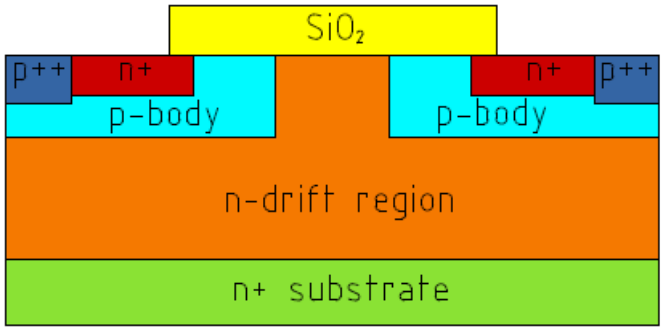



**Figure 4.4.2: Schematic of the SiC-MOSFET structure as considered in Fujihira's work [293].**

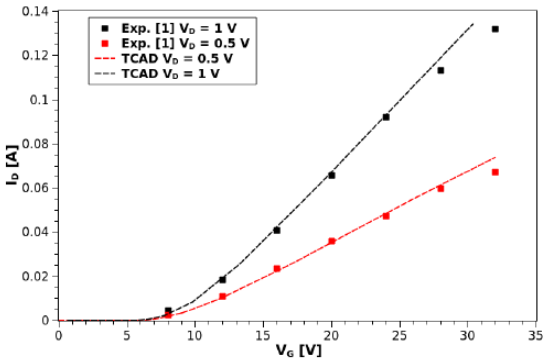



**Figure 4.4.3: Experimental and TCAD simulated data of the transfer characteristics of one of the tested SiC power MOSFET performed at two different $V_{DS}$ values ($V_{DS}$=1 V and $V_{DS}$=0.5 V).**

The TCAD simulations to model the PBTI were carried out in accordance with what was done in the experimental tests, that is, we start by applying a negative gate voltage at -5 V for 10 s and then we perform the stress phases at different temperatures by setting the $V_{GS}$. From the simulation performed, a good agreement was found with the experimental results as shown in figure 4.4.5. In the previous two chapters it has been shown that experiments clearly show a dependence of the BTI phenomena of the applied voltage stress. To consider exactly this aspect, Alam et al. [291] show that the RD model leads to good results since it is based on a physical approach of the problem [290]. Just as an example, these simulations consider the generation of defects at the $SiC/SiO_2$ interface caused by the breaking of the passivated Si-H bonds as can be observed in the interface between silicon and oxide. The released hydrogen atoms diffuse away from the interface in the oxide layer to recombine during recovery phase. For long stress times the model predicts the saturation of the $\Delta V_{th}$ when all the Si-H bonds have broken. Furthermore, the anomalous dependence on temperature observed in the experimental curves from $\Delta V_{th}$ can be ascribed to the rapid recovery time with the increase of T as described in Puschkarsky's work [278]. In our TCAD simulations this effect was introduced in the RD model by changing the activation energy of the hydrogen diffusion coefficients as shown in figure 4.4.6.

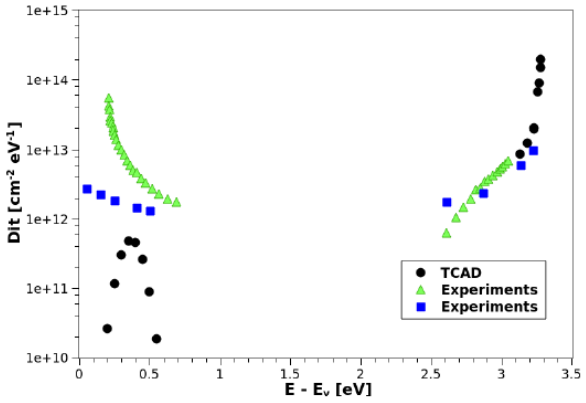



**Figure 4.4.4: Density of the states at the Interface as a function of the energy ranging from the SiC valence band to the conduction band. Green triangles and blue squares are the data reported in [64] and [294], while black circles are the data obtained from our simulations.**

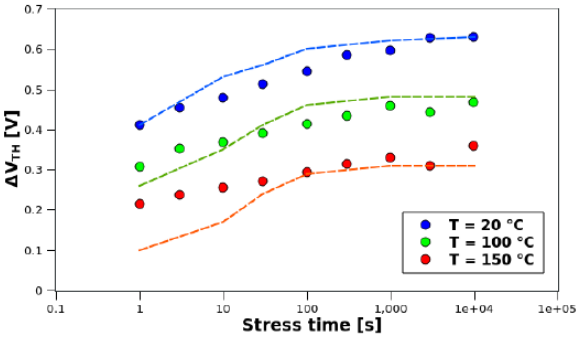



**Figure 4.4.5: Comparison of $\Delta V_{th}$ as a function of the stress time between the simulated TCAD data (dashed lines) and the experimental results at different temperatures and $V_{GS}$.**

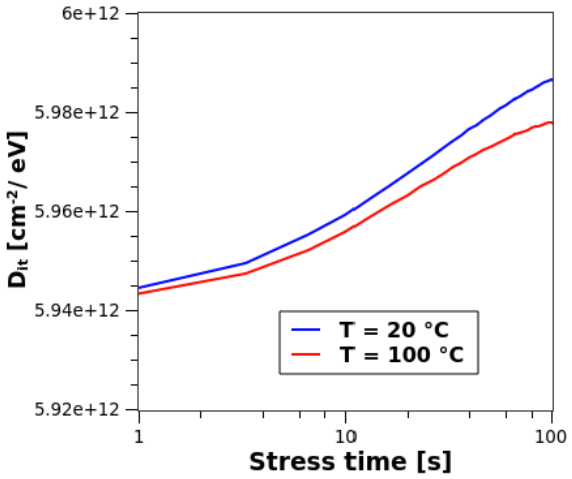



**Figure 4.4.6: Density of the interface traps simulated as a function of the stress time obtained for two different activation energies with a huge gap between them of the diffusion coefficients in the RD model by setting T at 20°C and 100°C.**

## 4.5 Characterization of the SiC-$SiO_2$ interface using spectroscopic techniques

As already mentioned in the introduction of this work, the analyses under study of this doctoral thesis were carried out in the framework of European project WInSiC4AP (Wide Band Gap Innovative SiC for Advanced Power). Numerous other actors participate in this project including the CNR working group for Microelectronics and Microsystems of the Catania site (CNR-IMM). In this last three years, I have participated in some conferences with some people of this group and, in particular, with P. Fiorenza, and we have exchanged information related to SiC power MOSFETs. The CNR team of Catania carried out several spectroscopic analyses on prototypes of SiC power MOSFETs and SiC MOS structures in order to characterize the interface between the SiC and silicon dioxide and understand exactly the nature of the trapping mechanisms. Therefore, to complete the analyses carried out in this work and better understand the meaning of the results of the experiments, it is important to introduce the results obtained by the CNR team and integrate them with ours data. The analyses carried out by the CNR team are based on Scanning Transmission Electron Microscopy (STEM) and sub-nm resolution Electron Energy Loss Spectroscopy (EELS) which allow to highlight the chemical composition of the $SiO_2$/4H-SiC interface region. First of all, Fiorenza et al. in their article [295] have carried out their experiments on a lateral MOSFETs fabricated on 4°-off-axis n-type (0001) 4H-SiC epitaxial layers with a doping concentration of $1\times10^{16}$ $cm^{-3}$ on a heavy doped 4H-SiC substrates. The p-well consisted of a region implanted with aluminium with an acceptor level of about $10^{17}$ cm-3 activated at 1650°C. The gate oxide had a thickness of 40 nm and it was subjected to a standard post deposition annealing treatment in an $N^2O$ ambient at 1150°C for four hours. STEM analyses were performed in a state of the art (Cs)-probe corrected JEOL ARM200CF at a primary beam energy of 200 keV operating in scanning mode. The images were acquired in a dark field z-contrast configuration using an annular dark-field detector. The images obtained by the EELS Spectroscopy are acquired by means of a Gatan Quantum spectrometer in dual EELS configuration for the of the correction energy drift. The energy dispersion was set to 0.25 eV/pixel in order to have all the three elements edge (100 eV for silicon, 285 eV for carbon and 530 eV for oxygen) in the same spectrum. The energy resolution – the half height width of the zero-loss peak – results in this configuration is 1.2 eV. The 3D spectrum image datacubes were acquired with a pixel size of 0.08 nm and pixel time of 0.02 s in fast spectroscopy mode. The carbon and oxygen elemental maps are extracted using a power-law background subtraction and 30 eV signal windows. TEM samples were prepared by mechanical polishing followed by low energy ion milling (0.5 keV) and left 72 hours in a high temperature degassing station (150°C) under vacuum condition ($10^{-7}$ hPa). Finally, the lamella was treated for 60 s in the plasma $O^2$ to remove the residual contamination of the surface carbon. The sample was prepared to be inspected along the direction orthogonal to the surface steps related to the off-axis substrate in order to obtain flat and clean images of the interface. Figure 4.5.1a shows the cross-section of the interface region in the high resolution dark-field spectrum image that simultaneously collected all the EELS elemental maps. The profile of the chemical elements highlights a sub-stoichiometric transition layer of oxycarbide compounds ($SiO_xC_y$) probably including also carboxyl defects as shown in figure 4.5.1b. It is worth noting that the presence of the carboxyl defects in the SiC-$SiO_2$ interface had already been experimental observed by Ettisserry et al. [197] as mentioned in chapter 2.2.5 and the effects of the oxycarbide compounds were simulated by Salemi [232] as seen in chapter 2.2.7.

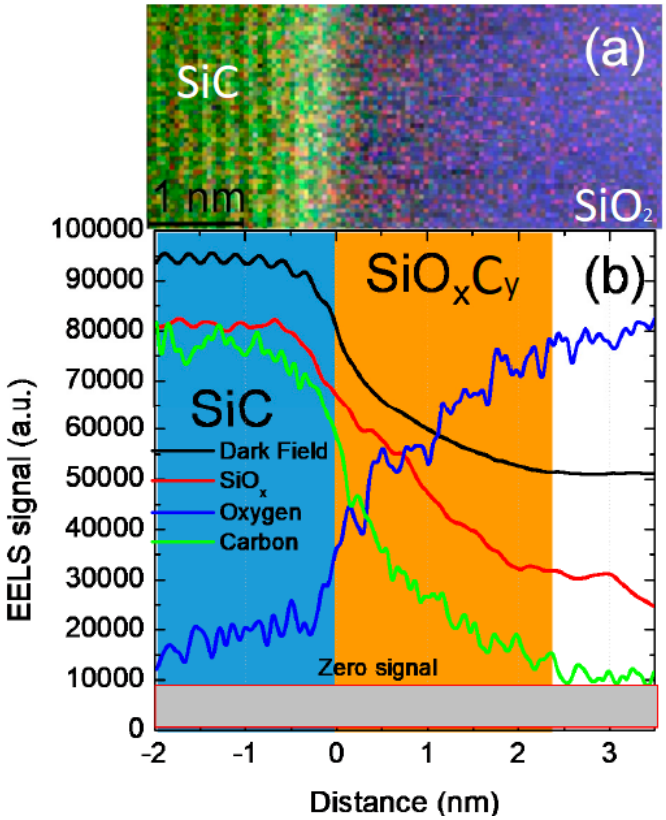



**Figure 4.5.1: Image of the spectroscopy analysis carrierd out on the lateral SiC MOSFET prototype estrapolated from the presentation of Fiorenza at the XXV International congress of aeronautics and astronautics and also shown in an article published in 2019 [296]: a) high-resolution spectrum imaging cross section STEM image of the $SiO_2$/4H-SiC interface; b) EELS spectra of the interface region between the SiC-$SiO_2$ layers.**

This experimental evidence suggests the presence of a non-abrupt interface and, thus, a transition layer which in this experiment is estimated to have a thickness of about 2.5 nm in accordance with what has been estimated in our BTI experiments using the method proposed by Lelis [198]. Indeed, as has already been mentioned previously, according to the approximation of WKB [250] based on Eq. (3.2.9), a single tunneling event of an electron occurs at a certain distance from the interface in logarithmic time. Paulsen et al. [298] introduced a more detailed expression to calculate the tunnelling times needed to reach the border traps as a function of the distance from the interface such as:

$$\tau(x) = \frac{4\pi^2 m^* \left(1+\frac{1}{2x\eta_1}\right)}{h^3 \eta_2 D_{it}} e^{2x\eta_1} \qquad (4.5.1)$$

where $\eta_1$ and $\eta_2$ are functions of the doping of the material and where $m^*$ is the effective mass for the electrons inside the oxide. From Eq. (4.5.1), by replacing the exact values in the constants as considered in the Paulsen work [298], it is possible to obtain the graph shown in figure 4.5.2 as attached in the Fiorenza paper [296] where the time constant as a function of depth within the oxide in logarithmic-linear scales shows a linear trend. The data of the time constant extrapolated from the latter graph are in good agreement with what is indicated by Lelis in chapter 4.3.
Another important Fiorenza study carried out on the lateral SiC MOSFET prototypes concerns the conduction mechanisms in the $SiO_2$/4H-SiC interface which involves the capture and release events of electrons from the border traps. The phenomena have been studied by means of transient gate current measurements performed on lateral n-channel MOSFETs by short-circuiting the source, body and drain terminals and by applying a potential in the gate terminal [297].

Fiorenza in his work tries to distinguish the contribute of the fast traps, intended as interface traps, from the slow traps, intended as border traps or NIOTs, focusing mainly on the effects produced by the latter. Fiorenza states that the current observed by applying a potential of up to 15 V in absolute value in the gate terminal is related to the charging and discharging of the interface states located close the 4H-SiC valence band. Therefore, Fiorenza observes the gate current when applying potentials in absolute values above 15 V and up to 35 V where the Fermi level intersects the edges of 4H-SiC band gap, that is, the conduction band for positive bias and the valence band for negative bias. The curves of the gate current as a function of $V_{GS}$ measured by applying a gate voltage in the range of 25 V–30 V are shown in figure 4.5.3 as also reported in [297]. In this graph, an anomalous gate current flow was observed at the $SiO_2$/SiC interface. In fact, the second $V_{GS}$ stress sweep does not overlap the first $V_{GS}$ stress sweep at least when negative voltages are applied. It is important to underline that the positive gate bias region is related to the electron injection through FN tunneling from the 4H-SiC conduction band while the negative gate bias region is related to the hole injection through FN tunneling from the 4H-SiC valence band. Fiorenza explained the anomalous phenomenon observed during the application of negative gate polarizations considering the combined effect of an electron Variable Range Hopping (VRH), related to the neutralization of the border traps in the oxide, with the FN tunneling. In particular, the measurements were acquired by repeating the voltage sweeps twice from 0 to -35 V followed by two voltage sweeps from 0 to 35 V. At the beginning, thus, when the first negative bias is applied, the conduction of holes occurs through the insulator layer. Therefore, in the second negative sweep, the characteristic shifts towards more negative gate bias values. Fiorenza observes in his experiments that, before applying the negative bias to the gate terminal, the hole barrier due to the offset between $SiO_2$ and 4H-SiC valence bands is significantly lower than the theoretical value due to the Coulombic effect due to the presence of negative charges in the border traps which are neutralized after the first negative gate bias is applied to the gate terminal. In fact, negative charges are accumulated in the border traps because a positive bias of 35 V was applied to the device for 120 s before performing the measurements. In his experiments, Fiorenza has also carried out gate current-gate bias characteristics by varying the measurement temperature in the range between 25 °C and 125 °C observing that the gate current measured during the first negative sweep increases with increasing the temperature while, in the second sweep, the characteristics are superimposed. These latest experimental results confirm that this process is a thermally activated trapping mechanism that can be explained by the Mott VRH model which describes conduction in disordered systems in which the gate current is proportional to $T^{-1/4}$. Instead, the thermal activation process does not exist when the second negative sweep is applied, thus, in this phase, an ideal temperature independent FN tunneling is observed. In his work, Fiorenza introduces a modified FN tunnelling model which considers the discharge, at negative bias, of negatively charged defects present in the oxide. First of all, Fiorenza measures the transient of the gate current obtained by setting the $V_{GS}$ to -25 V at different temperatures as shown in figure 4.5.4. From this graph it can be observed that the gate current decreases with time for all temperatures. Fiorenza concludes that this behaviour is due to a gradual change in the dominant transport mechanism from VRH to FN tunnelling due the progressive neutralization of the negative trapping centres. The equation of the gate current in the modified FN tunnelling model introduced by Fiorenza, to take into account the dependence of the oxide electric field on temperature, time and charge variation, it can be rewritten as:

$$I_{FN} = SA\left(\frac{V_{GS}-V_{FB}-\frac{Q_{it}}{C_{ox}}}{t_{OX}}\right)^2 e^{-\frac{B}{\left(\frac{V_{GS}-V_{FB}-\frac{Q_{it}}{C_{ox}}}{t_{OX}}\right)}} \quad (4.5.2)$$

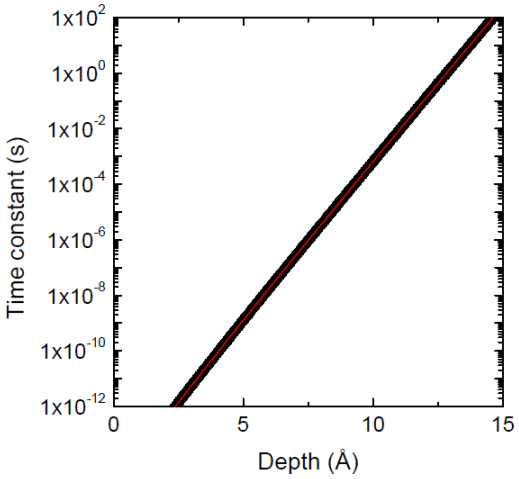



**Figure 4.5.2: Tunnenilng time constant as a function of the depth inside the oxide in logaritmic-linear scales obtained from the Paulsen Eq. (4.5.1) and extrapolated from the work of Fiorenza et al. [296].**

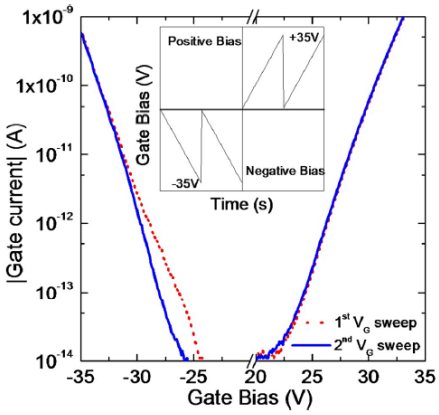



**Figure 4.5.3: Gate current-gate bias characteristics of the tested lateral MOSFET acquired in two sequential voltage sweeps, first of all, applying the $V_{GS}$ sweep in red (dotted line) and, than, applying a new $V_{GS}$ sweep in blue (solid line) as extrapolated from the work of Fiorenza et al. [297].**

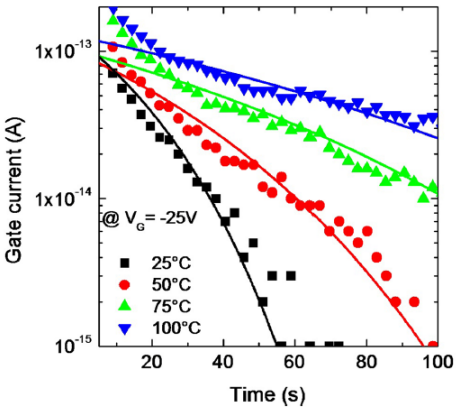



**Figure 4.5.4: Gate current transient over time characteristics in semi-logaritmic scales of the tested lateral MOSFET obtained by setting the $V_{GS}$ to -25 V at different temperatures extrapolated from the work of Fiorenza et al. [297].**

with:

$$E_{OX} = \left( \frac{V_{GS} - V_{FB} - \frac{Q_{it}}{C_{OX}}}{t_{OX}} \right) \tag{4.5.3}$$

and,

$$Q_{it} = qSN_t e^{-P_t t} \tag{4.5.4}$$

where $P_t$ is the single average time independent neutralization probability. In conclusion, Fiorenza with his experiments confirms that the capture and emission events of electrons from border traps are due to FN tunneling even if the model must be slightly modified to take into account the VRH effect.

## 4.6 Low frequency noise measurements on SiC power MOSFET devices previously tested

The first information on the amount of defects was be estimated by carrying out other characterization techniques such as threshold-voltage instability measurements and the PBTIs. On the other hand, the second information can be obtained by carrying out noise measurements on the current and voltage signals of the SiC power MOSFETs. As already exposed in chapter 3, any electronics component is a source of noise that can be generated by the chaotic movement of carriers inside it. This type of noise is called the internal source of the component to distinguish it from the external source caused by the presence of electromagnetic fields in the environment. In our study, of course, we focused on characterizing the internal source of noise of the tested SiC power MOSFETs because they provide us adequate information on the quality of the interface. As already seen in chapter 3, noise in SiC power MOSFETs, as in other electronics component, is due to thermal noise, shot noise, GR noise, RTS noise and flicker noise. We have already seen, for example, from Grasser's experiments discussed in chapter 4.3, that the typical noise events observed in the SiC power MOSFET interfaces are due to a sum of a huge number of RTS or G-R signals with time constants distributed over a wide time interval depending on the distance of the traps from the same interface. According to Bernamont's studies introduced in chapter 3, the sum of these last events involves a flicker noise in which the PSD of the signal depends approximately on the inverse of the frequency. Therefore, the experiments illustrated in this chapter will focus on the analyses carried out to characterize the flicker noise observed in the tested devices. Noise measurements can be analysed in the time domain and in the frequency domain. In the time domain it is possible to study the distribution of the signal amplitude, its PDF, the average value assumed by the signal and its variance. In the time domain it is also possible to establish if the noise signal has a persistence, if it is an ergodic process by analysing the autocorrelation diagram and if it is a stationary process. On the other hand, in the frequency domain it is possible to study the distribution of the power of the noise signal at different frequencies. Another fundamental aspect that can be studied in the frequency domain concerns the understanding of the noise mechanism. In fact, in chapter 3.2, in chapter 3.3, in chapter 3.4 and in chapter 3.5 it has been seen that different mechanisms can cause noise in currents and voltages due to defects in the interface region of the device such as fluctuation of the number of carriers in the channel, studied by the McWhorter's model, the fluctuation of the mobility of the carriers, studied by the Hooge's model, and by a combination of both models as in the correlated number-mobility fluctuation model and in the unified model for flicker noise. In our analyses, noise will be studied in both time and frequency domains to better understand all aspects of the phenomenon analysed. One of the main aspect concerning the noise measurements on the tested SiC power MOSFETs refers to the instrumentation used and to the setup of the same measures. It is important to note that in our tests we followed the guidelines proposed by Haartman et al. [235] and by Magnone in his PhD thesis [299] to extrapolate good noise signals from the measurements carried out. First of all, measuring noise is a complicated task because the current signal is very small in the order of pico-amperes, thus, it can be subjected to undesired disturbances that can compromise the measurements. Therefore, the measurements setup must be carefully designed with appropriate shielding and preferably using batteries as power sources, as effectively performed in our tests. Measurements are preferably performed in the frequency domain by measuring the PSD with a spectrum analyser. It is necessary to use a preamplifier to amplify the weak noise signal so that it

can be studied with the spectrum analyser. It is also important to use well-shielded triaxial or BNC cables for connection and avoid any open circuit. Furthermore, metal film resistors with low margin of error and Low-Noise Amplifiers, LNA, must be used. The noise at the output of the board where the tested SiC power MOSFET is located can come from many sources. Therefore, it is necessary to calculate the expected noise level at the output from different sources, measure the white noise and compare it with the expected noise in order to calibrate the measuring instrument well. It is also necessary to avoid bad contacts that can introduce the addition of further noise in the measurements. And again, it is important to use narrow frequency spans for good frequency resolution when measuring PSD. It is important to highlight once again that all the precautions indicated above have been adopted in the noise tests performed on the devices analysed. Haartman in its work [235] suggests that it is important to use on the board, where the SiC power MOSFET is located, a low-noise current amplifier which amplifiers the current through its low-impedance input and provides a voltage to the output which is amplified by the transimpedance gain. The value of the metal film resistors must be carefully selected so that the noise coming from the device under test is maximized at the output and, at the same time, the other noise components are minimized. Another important part of the measure concerns the spectrum analyser, as already introduced above in this chapter. Again, Haartman in its work [235] suggests what types of performances are needed to carried out the noise measurements better. First, the spectrum analyser is the tool used to measure and analyse a signal in the frequency domain and utilizes the discrete Fast Fourier Transform algorithm, FFT, to convert the measured signal from the time domain to the frequency domain as shown in figure 4.6.1. In this figure, the noise signal enters the analog part of the schematic consisting of an attenuator block followed by a low-pass filter. Subsequently, the analogic signal enters the ADC block, Analog to Digital Converter, which performs the conversion in a digital signal by sampling the input data. Then, the output signal of the ADC enters the digital part of the schematic managed by a microprocessor that performs a DSP, Digital Signal Processing, which implements the FFT algorithm. This algorithm is based on a swept-tuned analyser that uses a bandpass filter to study the signal in a small frequency range centered gradually on increasing values to cover the entire bandwidth of the signal. The power of the signal is measured after the bandpass filtering and divided by the frequency range considered to obtain the PSD at the various f. It is important to note that the frequency resolution of the spectrum measurement is established by the resolution bandwidth, the frequency span and the number of frequency points. The display resolution, which is equal to the frequency span divided by the number of frequency points minus one, is improved for narrower spans and frequency points while the frequency resolution is limited by the resolution bandwidth. Furthermore, a narrower resolution bandwidth not only improves frequency resolution, but also reduces the background noise because there is less noise power in a smaller range of f. In any case, a compromise must be made between the bandwidth and measurement time because by reducing the former, the latter increases significantly. Another important aspect that must be taken into consideration when performing the FFT algorithm concerns that the signal is assumed periodically from one time record to the next even if it is not the real case and this involves a broadening of the spectrum in the frequency axis. Therefore, to overcome this issue, the signal is multiplied by a weighting function in the time domain called window function which realizes a periodic signal. Typical window functions are the Hanning, the rectangular, the Gaussian top and the flattop and each of them have advantages and disadvantages. For example, Hanning gives a good frequency resolution while flattop gives high accuracy in the amplitude of the signal even if, in our experiments, the rectangular window was chosen because it does not introduce particular distortions of the original signal.

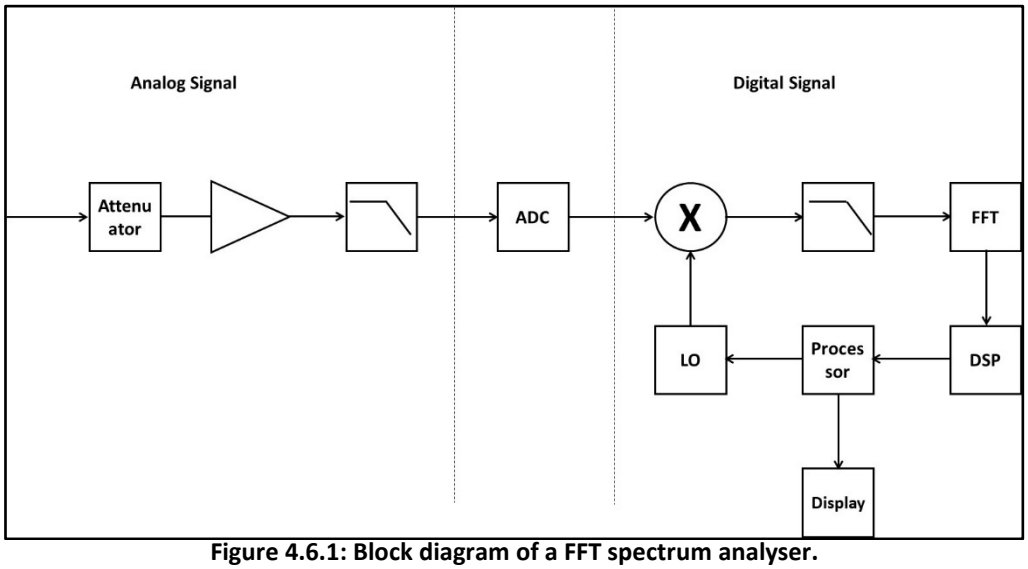



**Figure 4.6.1: Block diagram of a FFT spectrum analyser.**

Typically, the PSD graph extrapolated from the spectrum analyser provides the noise in term of voltage in $V^2Hz^{-1}$ or $VHz^{-1/2}$ and is the result of averaging at least few hundreds samples to obtain reliable noise measurements. Furthermore, it is common for the LF noise to be extracted at a selected frequency, for example 100 Hz, in order to study the variation of the noise spectrum with the gate voltage. With reference to the previously mentioned LNA amplifiers, it is important to introduce a parameter called as Signal to Noise Ratio, SNR, defined as:

$$\mathrm{SNR} = \frac{\mathrm{DUT_{noise}}}{\mathrm{LNA_{background\ noise}}} \tag{4.6.1}$$

where $LNA_{background\ noise}$ is the equivalent input noise calculated at the input of the LNA stage while $DUT_{noise}$ is the noise introduced by the tested SiC power MOSFET. It is important to note that, for aspects that will be explained later, the LNA is composed by two or more stages of cascaded amplification and that the most important contribution to background noise comes from the first stage because the contributions of noise entering the stages subsequent are divided by higher gains, thus, make a smaller contribution. Therefore, in a cascade network the noise is mainly influenced by the first stage, provided that the gain of this stage is greater. Now, the schematic of the measurements and the instrumentation used to carry out the experiments will be illustrated in detail. The measures were implemented using the National Instrument chassis NI PXI-1045. This instrumentation supports two modules, the NI PXI-4472 and the NI PXI-8831 MXI-4. The first is an AC/DC-Coupled, 8-input, 102.4KS/s, 3.4Hz and, through dedicated BNC cables, receives and analyses the signals of the devices under test. In particular, this instrumentation converts the analogic signals coming from the devices under test into digital signals which must be transferred to the PC. The second module is a GPBI controller and allows to connect the NI PXI-1045 chassis to the PC via the IEEE-488 GPIB connector. The transmission speed reaches up to 500Mb/s and the reception speeds reaches up to 800Mb/s. The digital data received from the NI PXI-1045 chassis is analysed by a DSA software provided by NI that runs on the PC. This software has a simple graphic interface in which two different kinds of graphs are represented simultaneously. In the first, the signal is shown over time while, in the second, the average values of the PSD as a function of the frequency is shown. The window function length can be adjusted by a suitable spectrum analyser selector from which you can set the sampling frequency and the bandwidth of the sampled signals. In particular, the larger the window function length, the higher the sampling rate and the bandwidth of the sampled signals. The analogical signals received by the NI PXI-8831 MXI-4 module are not the signals coming directly from the devices under test.

The signals coming from the devices under test before reaching the NI PXI-8831 MXI-4 module are amplified, as already said, by LNAs. The amplifier module allows to polarize the device under test by applying an established gate-source voltage with values just above the estimated threshold voltage (for us set to 3V), by fixing the drain-source voltage to 50mV. Due to the capture and release processes of the electrons flowing through the channel of the devices under test caused by the traps in the interface region between SiC and oxide layers, it is possible to detect RTS signals as variable signals in the time domain. These signals are amplified by two different stages. The first stage of amplification is a transimpedance preamplifier which converts the current signal that passes through the power MOSFET channel into voltage signals. It is important to note that the feedback resistor of the transimpedance amplifier is the key element of the circuit because a large value reduces the bandwidth of the amplifier stage and increases the DC output voltage that could lead to the same amplifier into saturation while, for too small values, it decreases the transimpedance gain and increases the input noise of the same amplifier. Therefore, it is necessary to find a compromise value which, in our case, is 1 MΩ. The output of this first stage is the input of two different second stages. The first of these second stages is an OP AMP in follower configuration which allows to detect the level of DC current flowing in the devices under test. Instead, in the second, the output of a no-inverter amplifier module allows to detect the AC components of the signals. A high-pass filter is inserted before the input of this last stage to eliminate the DC component of the signals. This filter also avoids saturating the second stage of the AC amplifier. Instead, the second AC stage amplifier is used to increase the entire gain of the system by avoiding to saturate the first stage of the preamplifier. The bandwidth of the whole system depends on the smallest bandwidth of the different stages. The Amplifier Module is inserted inside a metallic box to shield all the electronic components contained within it from external noise source of electromagnetic waves. The components to be tested are polarized by DC power suppliers which charges large capacitors included inside the amplifier module by means of a suitable circuit. In fact, the generators that powers the gate and the terminals cannot be simple batteries since we have to adjust the voltages of the tested devices. On the other hand, standard DC-DC converters are too noisy to be used for these applications, thus, the realization of very low noise programmable voltage sources is required. As will be shown later, a simple implementation of a low noise programmable voltage source can be realized by means of low-noise amplifiers connected in voltage follower configuration using switches. When the switch is closed, the capacitors are charged to the desired potential. Once the switch is open, the output voltage is maintained by the same capacitors that supply the tested components. Based on the Magnone experience [299], this type of polarization networks followed by the transimpedance amplifier greatly reduce the noise coming from the same voltage follower amplifier modules. The block diagram of the entire circuit used to carried out noise measurements on the test devices is shown in figure 4.6.2. As it is possible to see from figure 4.6.2 and previously exposed, the amplifier module has two output terminals, AC and DC. The AC terminal is connected, in our cases, to the CH 0 channel while the DC terminal is connected to CH 1 of the NI PXI-8831 module via two BNC cables. The AC and the DC signals come from the drain current of the tested devices and whose noise must be studied. The DC component provides information on the polarization levels of the device under test while the AC component depends on the physical and electrical characteristics of the interface region between the SiC and the oxide along the channel regions. The NI PXI-8831 module receives these two signals and through an ADC converts the analog signal to digital. Subsequently, the digital signal is managed by the NI PXI-4472 module which allows to transfer it from the NI PXI-1045 chassis to the PC via IEEE-488 GPBI cable. In the PC the signal is studied in the frequency domain through an NI software that implements the DSA. The PSD graph of the signal is shown in the monitor through a graphical interface. In the upper side of the monitor, it is possible to see the graph of the signal over time while, in the lower part, the PSD graph in the frequency domain is shown.

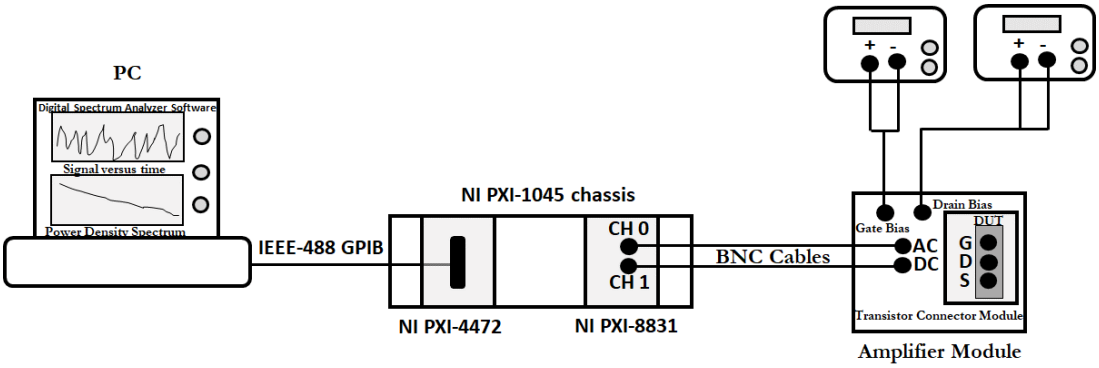



**Figure 4.6.2: Block Diagram of the circuit used for making noise measurements.**

In the graphical interface of the software it is possible to adjust the amplitude of the sampled bandwidth of the signal, the scales of the graphs and the selected channels to be shown on the display. Furthermore, as mentioned above, the signal can be processed with special digital filters, such as Hamming, Hanning, Blackman-Harris, Blackman, Flattop and others. The graphs below show the images of the instrumentations used. Instead, the electric circuit of the amplifier module is shown in figure 4.6.8. This module contains a part of the circuit relating to the DC polarization of the gate of the device to be tested (light violet part), a part of the circuit relating to the DC polarization of the MOSFET drain (green part), a transimpedance preamplifier stage (violet part), a second amplification stage made by an OP AMP in voltage follower configuration (red part), an high-pass filter (yellow part) and a second amplification stage with a no-inverter configuration to analyse the noise signal (orange part). The DC biasing part of the gate circuit is composed of the low noise OP AMP TLC2201 present on the board connected in voltage follower configuration. The no-inverter input of this OP AMP is connected to external DC power supplier via a P1 button. First, the power supplier voltage is fixed at 3V. The other input of the OP AMP is short-circuited with the output terminal of the OP AMP itself. All five low noise OP AMPs located on the board are polarized to +6 V and -6 V by two batteries of 6 V each, V3 and V4, placed inside the box. When the P1 button is pressed, the 3 V supplied by V1 are provided directly from the input to the output of the OP AMP 01. The input impedance of the OP AMP 01 is very high, thus, a very low current flows in the order of pico-Amps. Instead, in the output terminal of OP AMP 01, the impedance is very low and the 3V are applied on the network composed of R1-C2-R2-C3 by charging the capacitors C2 and C3 in a certain time. The equivalent electrical circuit of the gate polarization can be represented as in figure 4.6.9. The MOSFET gate resistance, $R_g$, is of the order of several MΩ. Considering that the gate resistance is very high and that $C_{GS}$ << C3, the circuit can be simplified as in figure 4.6.10a and figure 4.6.10b. At the beginning, before acting on the button P1, the capacitors C2 and C3 are discharged, no current flows in the circuit which is to be represented as in fig. 4.6.10a. Subsequently, after activating the button P1, the circuit becomes polarized and both capacitors begin to charge. In this condition, the current $i_1$ passes through $R_1$ and the power supplier, $i_3$ passes through $R_2$ and $C_3$ and $i_2$ flows through $C_2$. $V_{C2}$ and $V_{C3}$ are the voltages present in the terminals of the capacitors $C_2$ and $C_3$ respectively (see figure 4.6.10b). In node A it is possible to apply the Kirchhoff's law for currents (LKI) such as:

$$\sum_k i_k(t) = 0 \tag{4.6.2}$$

Instead, for the M1 and M2 networks, Kirchhoff's law for voltages (LKV) can be applied, such as:

$$\sum_k V_k = 0 \tag{4.6.3}$$

In our case, we can obtain:

$$i_1(t) = i_2(t) + i_3(t) \tag{4.6.4}$$

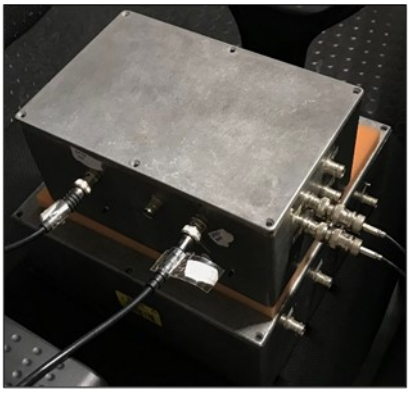


**Figure 4.6.3: Metal box containing the amplifier module and the device to be tested.**

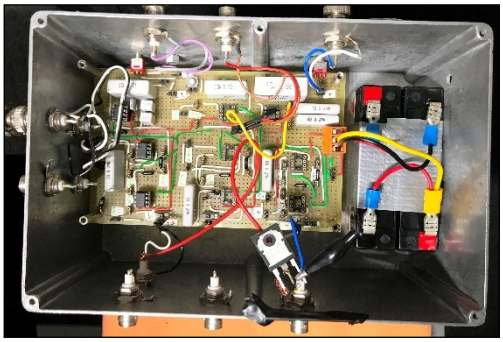


**Figure 4.6.4: Internal view of the Amplifier Module box.**

**Figure 4.6.5: Instrumentation used.**


**Figure 4.6.6: NI PXI-8831 and NI PXI-4472 modules.**

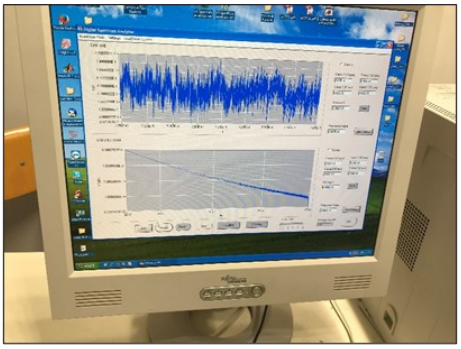


**Figure 4.6.7: Graphical interface of the NI DSA software that shows an example of the trend of a signal measured on a device in real-time with its PSD.**

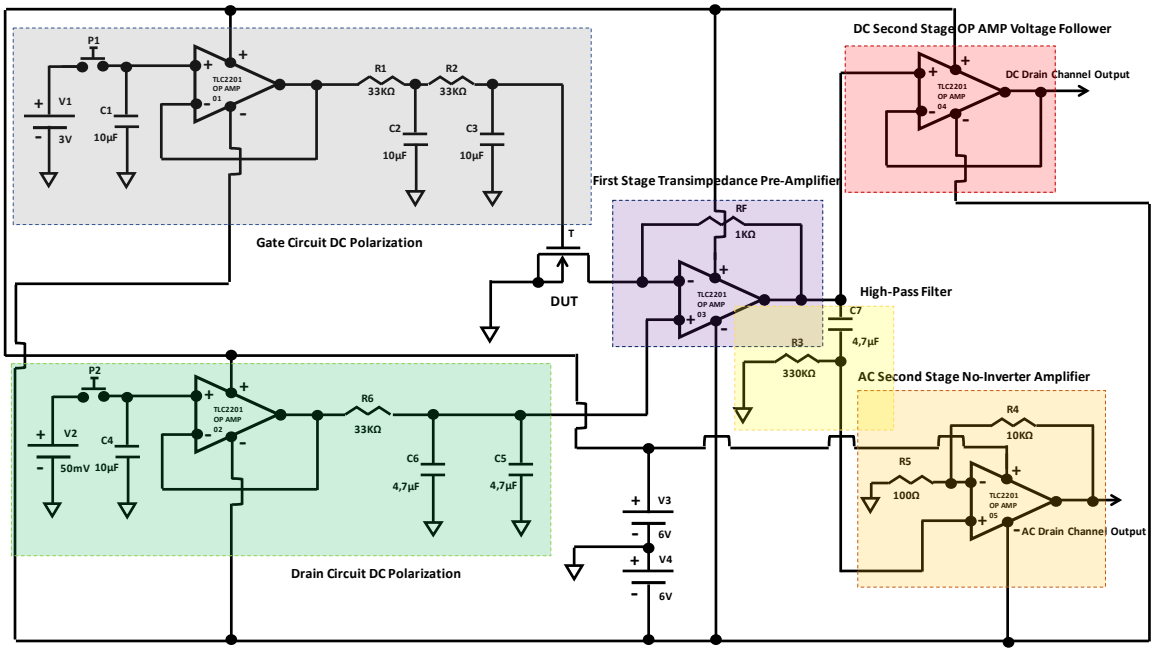



**Figure 4.6.8: Electric circuit of the amplifier module.**

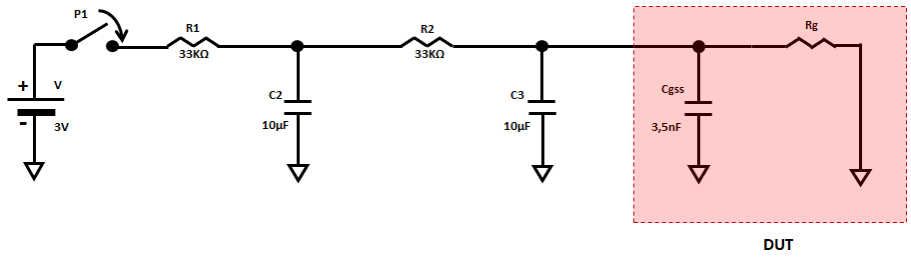



**Figure 4.6.9: Equivalent electrical circuit relating to the gate polarization of the device to be tested.**

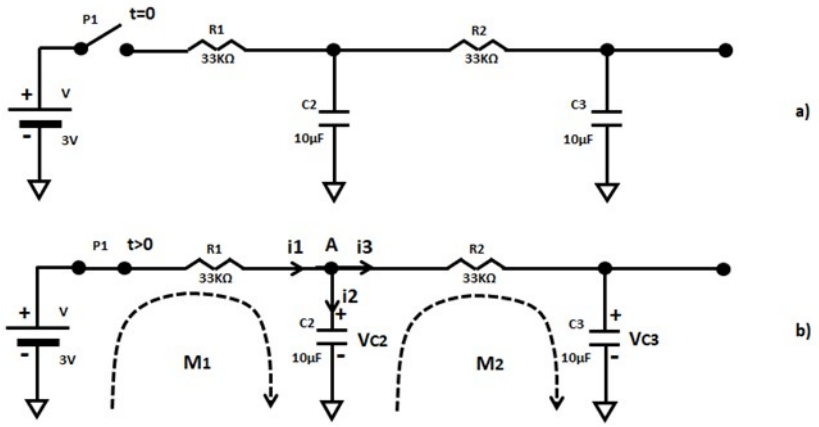



**Figure 4.6.10: Simplified electrical circuit relating of the polarization of the gate of the MOSFET to be tested: a) with P1 off and considered t=0; b) with P1 on and considered t>0.**

and:

$$V = R_1 i_1(t) + v_{c2}(t) \tag{4.6.5}$$

and, again:

$$v_{C2}(t) - R_2 i_2(t) - v_{C3}(t) = 0 \tag{4.6.6}$$

Considering that:

$$i_2(t) = C_2 \frac{dV_{c2}(t)}{dt} = C_2 \dot{V_{C2}} \tag{4.6.7}$$

and, that:

$$i_3(t) = C_3 \frac{dV_{c3}(t)}{dt} = C_3 \dot{V_{C3}} \tag{4.6.8}$$

it is possible to obtain the differential equation for $V_{C3}(t)$ which is the voltage applied on the gate terminal of the MOSFET as:

$$\ddot{V_{c3}} + \vartheta \dot{V_{c3}} + \theta V_{c3} = \hat{V} \tag{4.6.9}$$

with:

$$\vartheta = \frac{R_1(C_2+C_3)+R_2C_3}{R_1R_2C_2C_3} \tag{4.6.10}$$

$$\theta = \frac{1}{R_1R_2C_2C_3} \tag{4.6.11}$$

and:

$$\hat{V} = \frac{V}{R_1R_2C_2C_3} \tag{4.6.12}$$

Taking into account that $R_1 = R_2 = R$ and $C_1 = C_2 = C$, it is possible to obtain:

$$\vartheta = \frac{3}{RC} = \frac{3}{\tau} \tag{4.6.13}$$

$$\theta = \frac{1}{R^2C^2} = \frac{1}{\tau^2} \tag{4.6.14}$$

$$\hat{V} = \frac{V}{\tau^2} \tag{4.6.15}$$

with:

$$\tau = RC \tag{4.6.16}$$

The differential equation Eq. (4.6.9) is second-order, linear with constant and non-homogeneous, thus, it can be solved considering the sum of the solutions of the associated homogeneous differential equation plus a particular solution of the same non-homogeneous differential equation. The associated homogeneous differential equation of Eq. (4.6.9) is equal to:

$$\ddot{V_{c3}} + \vartheta \dot{V_{c3}} + \theta V_{c3} = 0 \tag{4.6.17}$$

Furthermore, considering that $\hat{V}$ is a constant, we can assume as a particular solution of Eq. (4.6.9) the following:

$$V_{c3}{}^{*} = \varphi \tag{4.6.18}$$

obtaining:

$$\varphi = \frac{\hat{V}}{\theta} = V \tag{4.6.19}$$

Assumed that $y_1$ and $y_2$ are two different solutions of Eq. (4.6.17), any other solution can be obtained as a linear combination of these. These two different solutions must however be linearly independent in the closed domain in which they are defined and this can be verified by the determinant of the Wronskian matrix defined as:

$$W(t) = \begin{vmatrix} y_1 & y_2 \\ \dot{y_1} & \dot{y_2} \end{vmatrix} \neq 0 \tag{4.6.20}$$

To solve the Eq. (4.6.20) it is necessary to associate and solve the characteristic polynomial of the homogeneous differential equation Eq. (4.6.17) such as:

$$\lambda^2 + \vartheta\lambda + \theta = 0 \tag{4.6.21}$$

obtaining:

$$\lambda_{1,2} = \frac{-\vartheta \pm \sqrt{\Delta}}{2} \tag{4.6.22}$$

with:

$$\Delta = \vartheta^2 - 4\theta \tag{4.6.23}$$

If $\Delta > 0$, there are two different real solutions, $\lambda_1$ and $\lambda_2$, obtaining:

$$V_{C3}(t) = \gamma_1 e^{\lambda_1} + \gamma_2 e^{\lambda_2} \tag{4.6.24}$$

If $\Delta = 0$, then there is only one real solution:

$$V_{C3}(t) = \gamma e^{\lambda} = \gamma e^{-\frac{\vartheta}{2}} \tag{4.6.25}$$

If $\Delta < 0$, there are two complex conjugate solutions of the type $\lambda_{1,2} = \vartheta + j\theta$, and we get:

$$V_{C3}(t) = e^{-\frac{\vartheta}{2}t}\left(\gamma_1 \cos\sqrt{\frac{-\Delta}{2}} + \gamma_2 \text{sen}\sqrt{\frac{-\Delta}{2}}\right) \tag{4.6.26}$$

In our case, the solutions are as in Eq. (4.6.24) because:

$$\Delta = \frac{5}{\tau^2} = \frac{5}{(RC)^2} > 0 \tag{4.6.27}$$

Therefore, the solution of Eq. (4.6.9) is equal to:

$$V_{c3}(t) = V\left(1 - \frac{3+\sqrt{5}}{2\sqrt{5}} e^{\frac{-t(3+\sqrt{5})}{2RC}} + \frac{3-\sqrt{5}}{2\sqrt{5}} e^{\frac{-t(3-\sqrt{5})}{2RC}}\right) \tag{4.6.28}$$

with:

$$\gamma_1 = \frac{3+\sqrt{5}}{2\sqrt{5}} \tag{4.6.29}$$

and:

$$\gamma_2 = -\frac{3-\sqrt{5}}{2\sqrt{5}} \tag{4.6.30}$$

The current flowing in C3 can be obtained as:

$$i_3(t) = C_3\dot{V_{C3}} = \frac{CV}{4\sqrt{5}RC}\left[\left(3+\sqrt{5}\right)^2 e^{\frac{-t(3+\sqrt{5})}{2RC}} + \left(3-\sqrt{5}\right)^2 e^{\frac{-t(3-\sqrt{5})}{2RC}}\right] \tag{4.6.31}$$

From Eq. (4.6.28) and Eq. (4.6.31), the voltage across the terminals of $C_2$ can be written as:

$$V_{C2}(t) = i_3(t)R + V_{C3}(t) \tag{4.6.32}$$

and its current can be obtained as:

$$i_2(t) = C_2\dot{V_{C2}} \tag{4.6.33}$$

The transients of these electrical characteristics can also be easily obtained by carrying out simulations with the LTspice software. Figure 4.6.11 shows the electrical circuit drawn in LTspice used to simulate the gate polarization circuit of the MOSFET. Instead, figure 4.6.12 shows the simulations of the different electrical parameters over time performed with LTspice. As it is possible to see in figure 4.6.12, the steady state condition is obtained after about 6 s that the button P1 has been turned on. From a point of view of small signals in the frequency domain, the gate polarization electric circuit can be represented as in figure 4.6.13. In the left part of figure 4.6.13, the electrical

circuit for small signals is shown while, on the right side, the simplified circuit according to Thevenin's theorem is shown. The impedance Z(s) is that measured by the output terminals of the circuit by disconnecting C3 and considering V(s) in short circuit. E(s) is equal to $V_{C2}(s)$ when C3 is disconnected and Z(s) can be obtained as:

$$Z(s) = R_2 \frac{s+\frac{R_1+R_2}{R_1R_2C_2}}{s+\frac{1}{R_1C_2}} \tag{4.6.34}$$

Based on the previous simplifications, Eq. (4.6.34) becomes:

$$Z(s) = R\frac{s+\frac{2}{RC}}{s+\frac{1}{RC}} \tag{4.6.35}$$

The impedance measured from the terminals of E(s) is equal:

$$Z(s) + \frac{1}{sC} = R\frac{s^2+\frac{3}{RC}s+\frac{1}{R^2C^2}}{s\left(s+\frac{1}{RC}\right)} \tag{4.6.36}$$

and the current flowing in the equivalent Thevenin circuit is equal to:

$$I(s) = \frac{E(s)}{R}\frac{s\left(s+\frac{1}{RC}\right)}{s^2+\frac{3}{RC}s+\frac{1}{R^2C^2}} \tag{4.6.37}$$

The voltage across the terminals of $V_{C3}$ is equal to:

$$V_{C3}(s) = I(s)\frac{1}{sC} = \frac{E(s)}{RC}\frac{s+\frac{1}{RC}}{s^2+\frac{3}{RC}s+\frac{1}{R^2C^2}} \tag{4.6.38}$$

Finally, the transfer function can be written as:

$$G(s) = \frac{V_{C3}(s)}{E(s)} = \frac{1}{RC}\frac{s+\frac{1}{RC}}{s^2+\frac{3}{RC}s+\frac{1}{R^2C^2}} \tag{4.6.39}$$

The Body diagram of the transfer function obtained from MATLAB is illustrated in figure 4.6.14. As you can see in figure 4.6.14, the noise coming from the output of the OP AMP are attenuated strongly already at very low frequencies less than 1 Hz.

The electrical circuit equivalent of the drain polarization of the MOSFET is shown in figure 4.6.15. Since the input resistance of the OP AMP is very high and that the $C_{DS}$ << C6 + C5, the circuit can be simplified as in figure 4.6.16a and figure 4.6.16b as a low-pass filter in which, for simplicity, let's set **C** as the sum of C6 and C5. At the beginning, before acting on the P2 button, the capacitor **C** is discharged and no current passes through the circuit as shown as in figure 4.6.16a. Subsequently, by turning on the P2 button, the circuit is powered and the capacitor starts charging as (see figure 4.6.16b):

$$i(t) = \mathbf{C}\frac{dV_c(t)}{dt} = \mathbf{C}\dot{V}_C \tag{4.6.40}$$

Furthermore, it is possible to obtain:

$$V - R_6 i(t) - V_C(t) = 0 \tag{4.6.41}$$

Therefore, the differential equation for $V_C$ can be written as:

$$\dot{V}_c + \frac{V_c}{RC} = \frac{V}{RC} \tag{4.6.42}$$

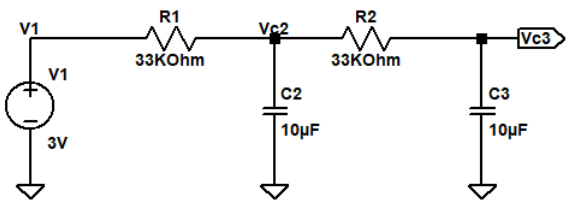



**Figure 4.6.11: Electrical circuit drawn in LTspice of the polarization stage of the MOSFET gate to be tested.**

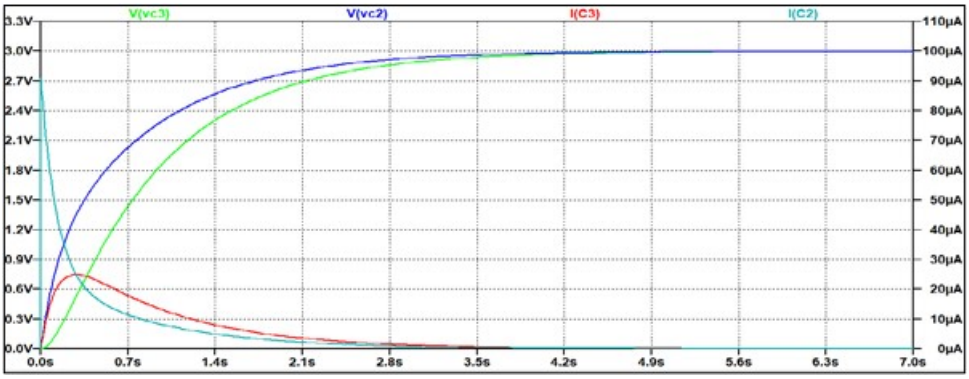



**Figure 4.6.12: Electrical parameters over time of the electrical circuit of the gate polarization stage obtained with LTSpice.**

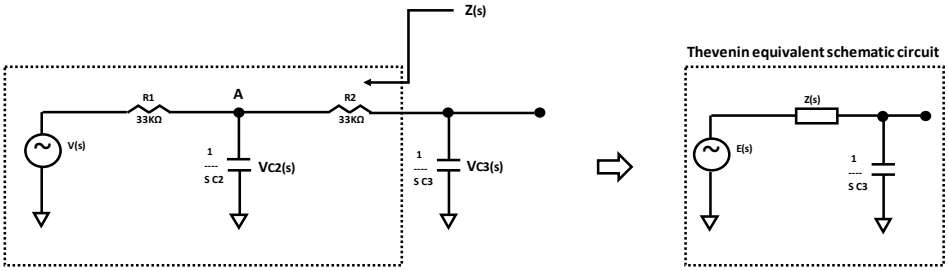



**Figure 4.6.13: Equivalent electrical circuit of the gate polarization stage from a small signals point of view.**

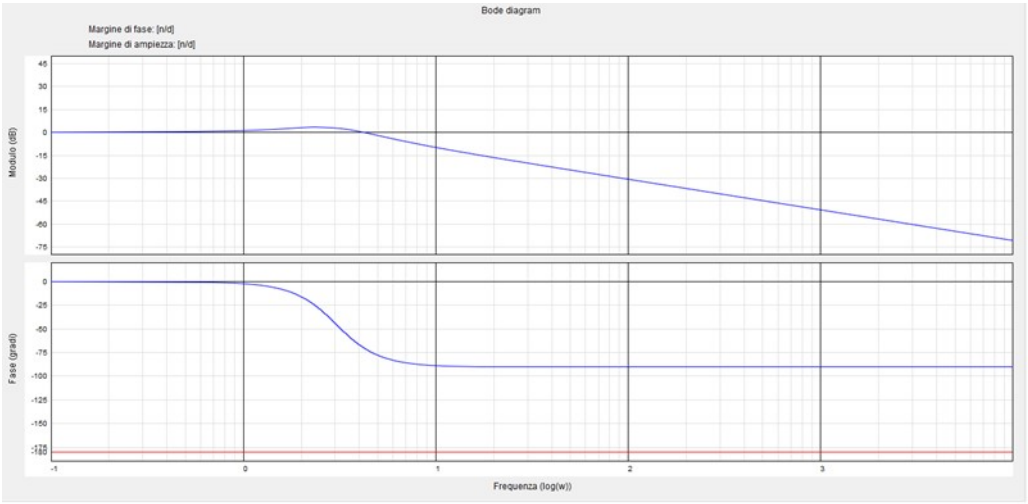



**Figure 4.6.14: Bode diagram of the transfer function relating to the gate electric circuit.**

The particular solution associated with Eq. (4.6.42) is equal to:

$$V_c = V \tag{4.6.43}$$

and the associate homogeneous different equation is given by:

$$\dot{V}_c + \frac{V_c}{RC} = 0 \tag{4.6.44}$$

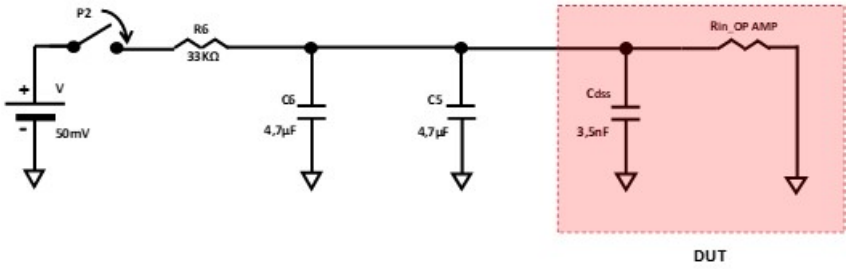



**Figure 4.6.15: Equivalent electrical circuit relating to the drain polarization of the device to be tested.**

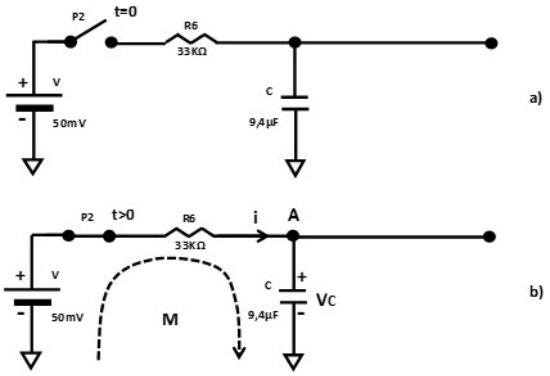



**Figure 4.6.16: Simplified electrical circuit relating of the polarization of the drain of the MOSFET to be tested: a) with P2 off and considered t=0; b) with P2 on and considered t>0.**

Therefore, the solution of Eq. (4.6.44) is given by:

$$V_c(t) = V + \gamma_1 e^{-\frac{t}{RC}} \tag{4.6.45}$$

considering that $V_C(0)=0$, $V_C(+\infty)=V$ and:

$$\mathbf{C}\dot{v_c}(0) = \frac{V}{R} \tag{4.6.46}$$

it is possible to obtain:

$$\gamma_1 = -\frac{1}{RC} \tag{4.6.47}$$

and, finally:

$$V_c(t) = V\left(1 - e^{-\frac{t}{RC}}\right) \tag{4.6.48}$$

The current flowing in the circuit can be written as:

$$i(t) = C\dot{V_c}(t) = \frac{V}{R}e^{-\frac{t}{RC}} \tag{4.6.49}$$

where, in our case, R is equal to 33 KΩ and **C** is equal to 9.4 μF.
Figure 4.6.17 shows the electrical circuit drawn in LTspice used to simulate the drain polarization circuit of the MOSFET.

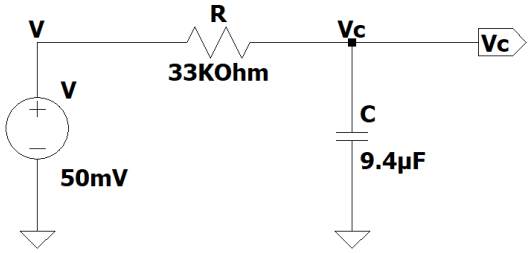



**Figure 4.6.17: Electrical circuit drawn in LTspice of the polarization stage of the MOSFET drain to be tested.**

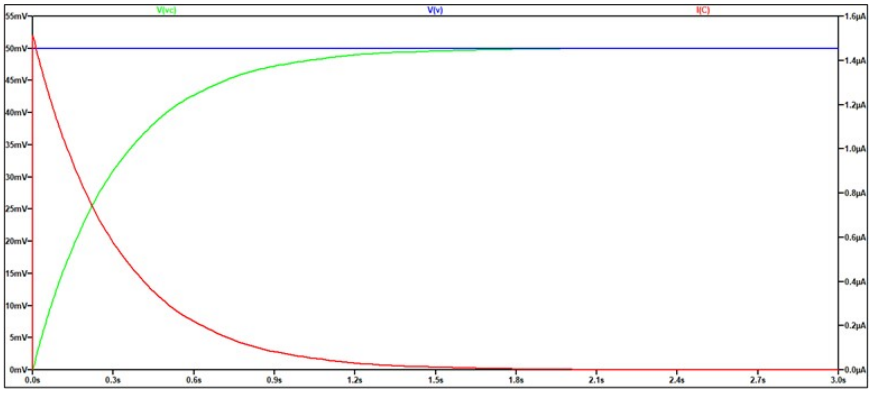



**Figure 4.6.18: Electrical parameters over time of the electrical circuit of the drain polarization stage obtained with LTSpice.**

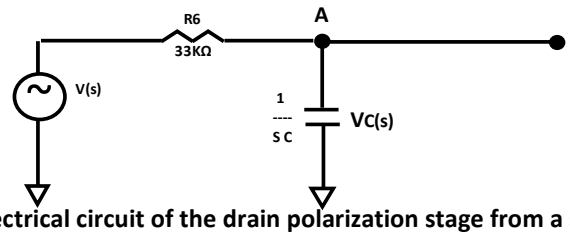



**Figure 4.6.19: Equivalent electrical circuit of the drain polarization stage from a small signals point of view.**

Instead, figure 4.6.18 shows the simulations of the different electrical parameters over time performed with LTspice. As you can see, the steady state condition is obtained after about 2.5 seconds after pressing the P2 button. From a point of view of small signals in the frequency domain, the drain polarization electric circuit can be represented as in figure 4.6.19. The impedance measured at the terminals of the voltage generator V(s) is equal to:

$$\mathbf{Z}(s) = \frac{sR_6\mathbf{C}s+1}{\mathbf{C}s} \tag{4.6.50}$$

The current flowing in the circuit is equal to:

$$I(s) = \frac{V(s)}{Z(s)} = V(s)\frac{\mathbf{C}s}{sR_6\mathbf{C}s+1} \tag{4.6.51}$$

and the voltage across the terminals of **C** is equal to:

$$V_c(s) = \frac{I(s)}{s\mathbf{C}} = V(s)\frac{1}{sR_6\mathbf{C}s+1} \tag{4.6.52}$$

Finally, the transfer function can be written as:

$$G(s) = \frac{V_c(s)}{V(s)} = \frac{1}{sR_6\mathbf{C}s+1} \tag{4.6.53}$$

The Body diagram of the transfer function obtained from MATLAB is illustrated in figure 4.6.20. As you can see in figure 4.6.20, noise coming from the OP AMP output is greatly attenuated very low frequencies below 1 Hz.

Now, let's focus on the transimpedance pre-amplifier stage. The equivalent circuit of the transimpedance stage is shown in figure 4.6.21a. In figure 4.6.21b the MOSFET is replaced with the channel resistance of the same device which depends on the voltage applied on the gate terminal. The current flowing in the $R_F$ reference resistance is equal to:

$$i = \frac{V_{out}-V}{R_F} \tag{4.6.54}$$

The same current can be written as:

$$i = \frac{V}{R_{ch}} \tag{4.6.65}$$

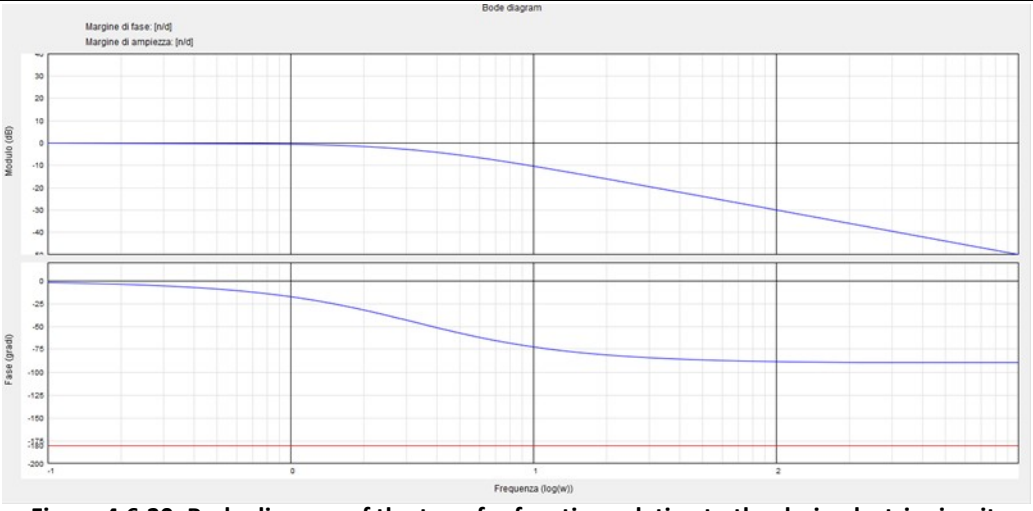



**Figure 4.6.20: Bode diagram of the transfer function relating to the drain electric circuit.**

Therefore, the current i changes its value as a function of the gate polarization. The voltage gain factor can be obtained as:

$$A_v = 1 + \frac{R_F}{R_{ch}} \tag{4.6.66}$$

From a small signal point of view, the equivalent circuit of the transimpedance stage can be represented as shown in figure 4.6.21. From figure 4.6.21, it is possible to obtain:

$$V_{out}(s) = R_F I(s) \tag{4.6.67}$$

and, again:

$$G_1(s) = \frac{V_{out}(s)}{I(s)} = R_F \tag{4.6.68}$$

In figure 4.6.8, one of the two stages located at the output of the transimpedance stage is an amplifier in the voltage follower configuration. In this case, the output signal to the voltage follower is the same as the input signal to the non-inverter terminal of the OP AMP, that is, the signal coming from the transimpedance stage. This stage allows us to measure the DC voltage at the output of the transimpedance stage in order to evaluate the current flowing in $R_F$ and, thus, in the MOSFET channel and also allows to evaluate the possible imbalance phenomenon in the inputs of the OP AMP which can be estimated by measuring the output voltage when the input terminals are short-circuited. The AC signal output from the transimpedance pre-amplification stage, which monitors the noise signal, is further amplified by the amplifier in the non-inverting configuration of the second AC stage. However, to eliminate the DC component and avoid saturation of the second amplification stage, it is necessary to introduce a high pass filter as shown in figure 4.6.8 and highlighted in figure 4.6.23 for the analysis of small signals.

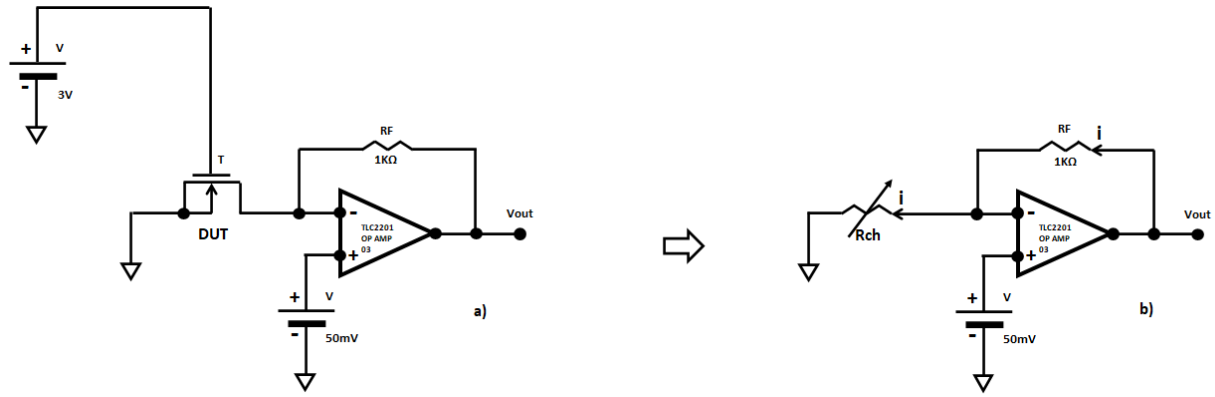



**Figure 4.6.21: Transimpedance pre-amplifier stage: a) real circuit; b) simplified circuit.**

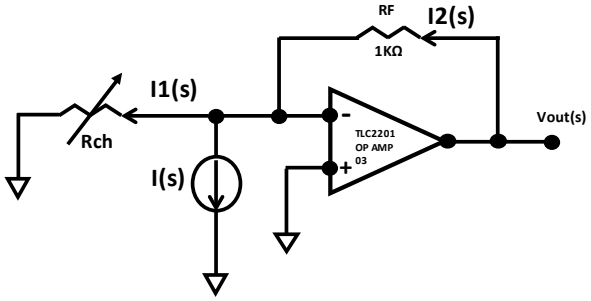



**Figure 4.6.22: Electrical circuit for small signals of the transimpedance stage.**

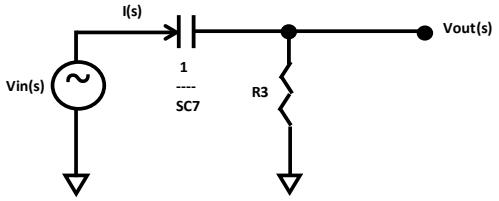



**Figure 4.6.23: Electrical circuit for small high-pass filter signals.**

From figure 4.6.23, it is possible to observe that the impedance Z(s) measured by the terminals of $V_{in}(s)$ is equal to:

$$\mathrm{Z(s)} = \frac{\mathrm{sR_3C_7+1}}{\mathrm{sC_7}} \tag{4.6.69}$$

The current flowing in the circuit can be written as:

$$\mathrm{I(s)} = \frac{\mathrm{V_{in}(s)}}{\mathrm{Z(s)}} = \mathrm{V_{in}(s)}\frac{\mathrm{sC_7}}{\mathrm{sR_3C_7+1}} \tag{4.6.70}$$

Therefore, the voltage in the output terminals is equal to:

$$\mathrm{V_{out}(s)} = \mathrm{I(s)R_3} = \mathrm{V_{in}(s)}\frac{\mathrm{sR_3C_7}}{\mathrm{sR_3C_7+1}} \tag{4.6.71}$$

Finally, the transfer function of this stage can be written as:

$$\mathrm{G_2(s)} = \frac{\mathrm{V_{out}(s)}}{\mathrm{V_{in}(s)}} = \frac{\mathrm{sR_3C_7}}{\mathrm{sR_3C_7+1}} \tag{4.6.72}$$

The body diagram of the transfer function is shown in figure 4.6.24. From this graph it is possible to observe that well below about 1 Hz the amplitude of the signal decreases rapidly. The output of the high pass filter is the input in the non-inverting terminal of the OP AMP 05 of the second AC stage as shown in figure 4.6.25. Figure 4.6.25 shows an amplifier in configuration non-inverting which has a voltage gain of:

$$\mathrm{G_3(s)} = \frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = 1 + \frac{\mathrm{R_4}}{\mathrm{R_5}} = 101 \tag{4.6.73}$$

The entire equivalent electrical circuit of the amplification module from the point of view of small signals is shown in figure 4.6.26. The transfer function of the entire circuit is equal to:

$$\mathrm{G(s)} = \mathrm{G_1(s)G_2(s)G_3(s)} = \frac{\mathrm{V_{out}(s)}}{\mathrm{I(s)}} = \mathrm{R_F}\left(1 + \frac{\mathrm{R_4}}{\mathrm{R_5}}\right)\frac{\mathrm{sR_3C_7}}{\mathrm{sR_3C_7+1}} = 101000\,\frac{1.551\mathrm{s}}{1.551\mathrm{s}+1} \tag{4.6.74}$$

As it is possible to see from Eq. (4.6.74), the gain factor of the entire amplification module is equal to 101000. The Bode diagram of this latter transfer function is shown in figure 4.6.27, the schematic circuit such as design in LTspice is shown in figure 4.6.28. As it is possible to see from the Body diagram, signals with frequencies above about 1 Hz are strongly amplified, this allows us to study the noise of the SiC power MOSFETs to be tested. Again, the input and the output are in phase.

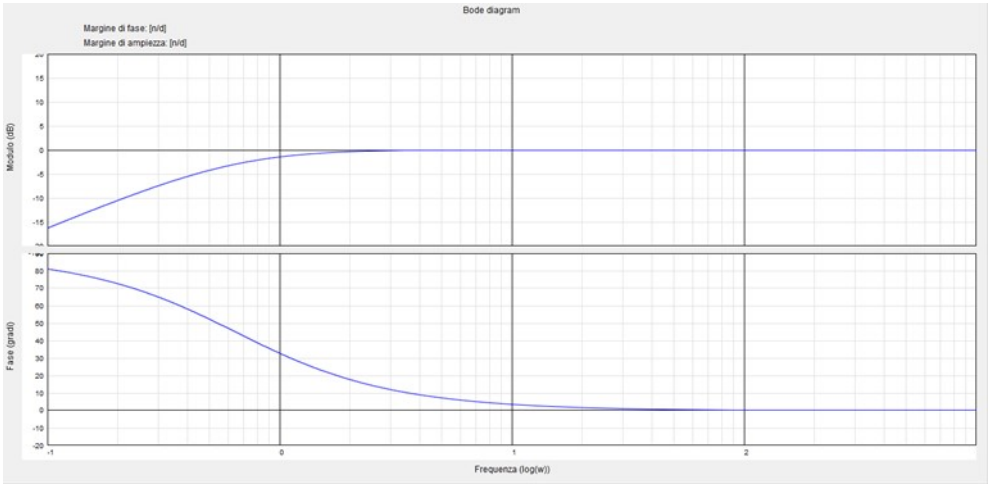



**Figure 4.6.24: Bode diagram of the transfer function relating to the high-pass filter.**

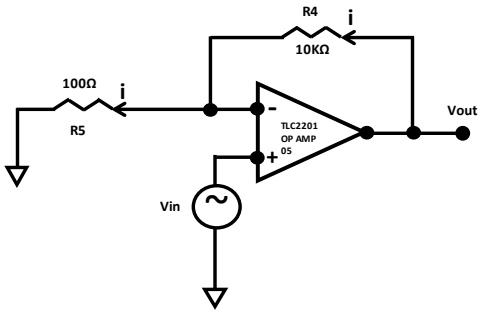



**Figure 4.6.25: Electrical circuit for small signals of the second stage of AC amplification.**

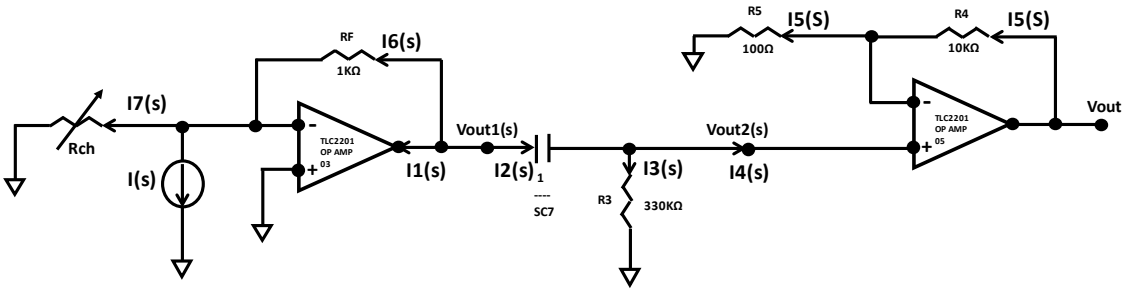



**Figure 4.6.26: Electrical circuit for small signals of the entire amplifier module.**

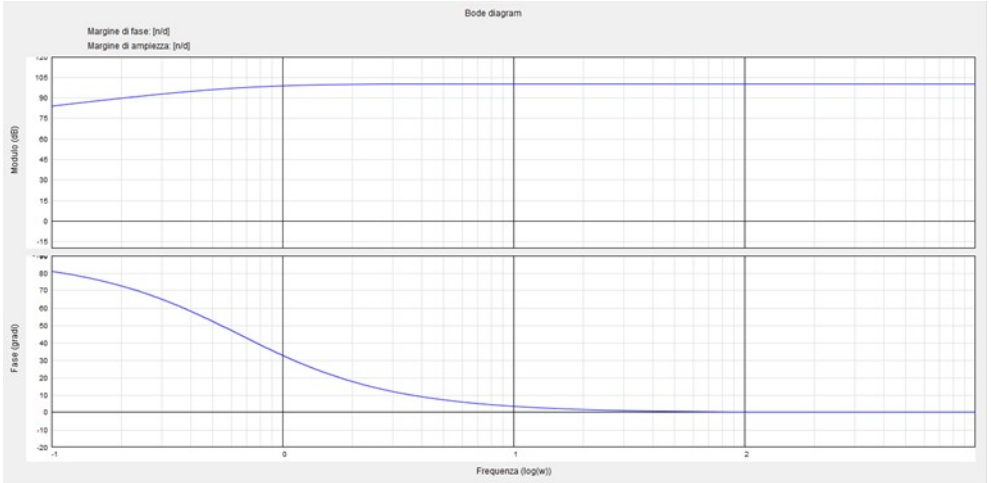



**Figure 4.6.27: Bode diagram of the transfer function of the entire amplifier module.**

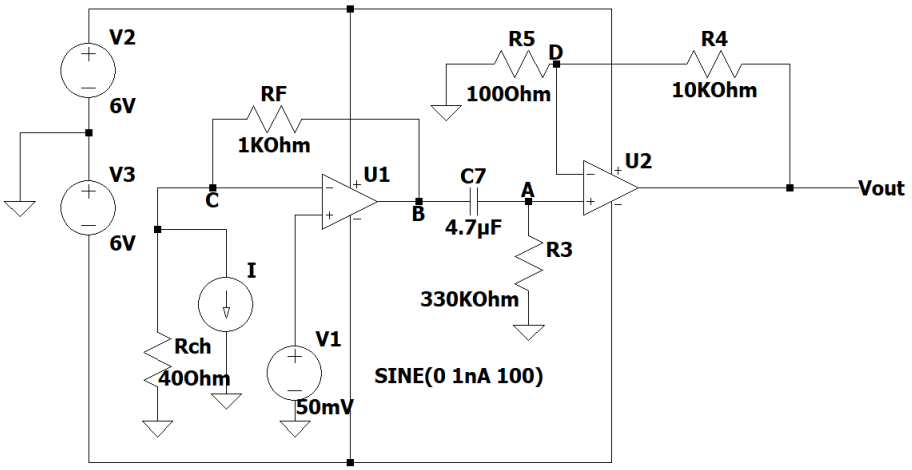



**Figure 4.6.28: Electric circuit used in LTspice of the entire amplification module designed to simulate small signals.**

# 4.6.1 The low frequency noise studied from the point of view of the approximate entropy of the tested SiC power MOSFETs

In chapter 3.7, we introduced the concept of entropy of stochastic processes in order to better and easier analyse the noise signals. In particular, we focused our attention on the approximate entropy parameter introduced by Pincus to classify noises based on their complexity and irregularity. The approximate entropy is obtained from Eq. (3.7.16) and it is a simple procedure to understand if the noise signals have a deterministic, chaotic or purely random behaviour to better monitor their regularity. In particular, the greater the approximate entropy value, the greater the randomness of the signal and, thus, the disorder of the system. It can be a useful tool when comparing the approximate entropies obtained from different signals. In fact, as first test of our analysis to be carried out on the study of flicker noises obtained from the tested SiC power MOSFETs, it is possible to use the approximation entropy to evaluate if the noise from the transistor has the same regularity as other signals or if it shows the same behaviour as a purely random signal. The approximate entropy data obtained from the samples of both type A and type B devices by MATLAB are summarized in tab. 4.6.1.1 for the $V_{GS}$ which varies from 3.4 V to 5.0 V. The first analysis compare statistically if the random signals of figure 4.6.1.1 have the same approximate entropy as the observed noise signals. The analysis was implemented through Statex open source software by applying the ANOVA test (ANalysis Of VAriance) and the Kruskal-Wallis test. The ANOVA test can be successfully applied when the data to be compared are normally distributed. Instead, the Kruskal-Wallis test is a test that can be successfully applied to data that present any type of distribution. The results of this analysis are shown in figure 4.6.1.2 and figure 4.6.1.3. Both method have shown statistically that the noise signals obtained by the SiC power MOSFETs have lower values than the random signals of figure 4.6.1.1 and, thus, show greater regularity and less chaoticity. In practice, signal noises coming from tested power MOSFETs show a certain deterministic behaviour over time which will be studied in the next two chapters. The same analysis performed by comparing both samples of the SiC power MOSFET families does not highlight any statistically significant difference in the approximate entropy as shown in figure 4.6.1.4 and figure 4.6.1.5. Even the analysis performed on the tested devices divided into groups for each $V_{GS}$ value does not show any statistically significant difference in the approximate entropy as shown in figure 4.6.1.6 and figure 4.6.1.7. In these latter cases, therefore, only an in-depth time-domain analysis of the noise signals will be able to highlight more details of the phenomenon as will be shown in chapter 4.6.3.

**Tab. 4.6.1.1: Approximate entropies obtained from samples of both tested SiC power MOSFET families and random signals.**

| type A device | $V_{GS}$ | Entropy | type A device | $V_{GS}$ | Entropy | type A device | $V_{GS}$ | Entropy |
|---|---|---|---|---|---|---|---|---|
| device 1 | 3.4 V | 1.6401 | device 4 | 3.4 V | 1.5179 | device 7 | 3.4 V | 1.6136 |
| device 1 | 3.8V | 1.5934 | device 4 | 3.8V | 1.517 | device 7 | 3.8V | 1.4803 |
| device 1 | 4.2V | 1.5226 | device 4 | 4.2V | 1.634 | device 7 | 4.2V | 1.5938 |
| device 1 | 4.6V | 1.5987 | device 4 | 4.6V | 1.5338 | device 7 | 4.6V | 1.5457 |
| device 1 | 5.0V | 1.5197 | device 4 | 5.0V | 1.5024 | device 7 | 5.0V | 1.5937 |
| | | | | | | | | |
| device 2 | 3.4 V | 1.6481 | device 5 | 3.4 V | 1.5686 | device 8 | 3.4 V | 1.5872 |
| device 2 | 3.8V | 1.5018 | device 5 | 3.8V | 1.4876 | device 8 | 3.8V | 1.6419 |
| device 2 | 4.2V | 1.5724 | device 5 | 4.2V | 1.4873 | device 8 | 4.2V | 1.5588 |
| device 2 | 4.6V | 1.5477 | device 5 | 4.6V | 1.5002 | device 8 | 4.6V | 1.5697 |
| device 2 | 5.0V | 1.5438 | device 5 | 5.0V | 1.5199 | device 8 | 5.0V | 1.4125 |
| | | | | | | | | |
| device 3 | 3.4 V | 1.5104 | device 6 | 3.4 V | 1.5553 | ***random 1*** | | 1.7348 |
| device 3 | 3.8V | 1.4718 | device 6 | 3.8V | 1.5072 | ***random 2*** | | 1.8013 |
| device 3 | 4.2V | 1.5247 | device 6 | 4.2V | 1.6157 | ***random 3*** | | 1.7748 |
| device 3 | 4.6V | 1.5946 | device 6 | 4.6V | 1.5852 | | | |
| device 3 | 5.0V | 1.5785 | device 6 | 5.0V | 1.5236 | | | |

| type B device | $V_{GS}$ | Entropy |
|---|---|---|
| device 1 | 3.4 V | 1.4495 |
| device 1 | 3.8V | 1.5893 |
| device 1 | 4.2V | 1.6614 |
| device 1 | 4.6V | 1.5742 |
| device 1 | 5.0V | 1.5497 |
| | | |
| device 2 | 3.4 V | 1.581 |
| device 2 | 3.8V | 1.5636 |
| device 2 | 4.2V | 1.574 |
| device 2 | 4.6V | 1.5676 |
| device 2 | 5.0V | 1.5233 |
| | | |
| device 3 | 3.4 V | 1.519 |
| device 3 | 3.8V | 1.5774 |
| device 3 | 4.2V | 1.513 |
| device 3 | 4.6V | 1.5513 |
| device 3 | 5.0V | 1.5978 |

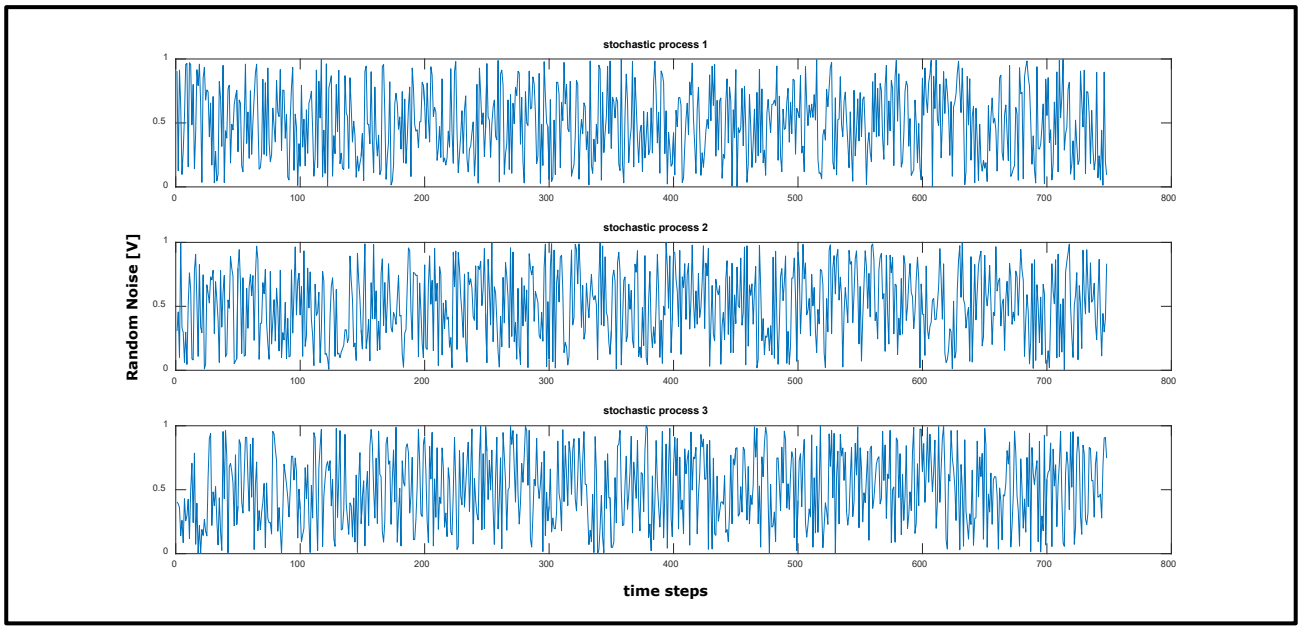



**Figure 4.6.1.1: Three random signals obtained by MATLAB having the same duration as the analysed noise signals.**

```
ONE-WAY ANALYSIS OF VARIANCE (ANOVA)

  HO: NO DIFFERENCES BETWEEEN THE MEANS OF THE 2 GROUPS
  HA: AT LEAST ONE OF THE MEANS IS NOT THE SAME AS OTHER MEANS
      (ALPHA = 0.05)

  SOURCE           SS    DF      MS       F   P(>F)
  ------------------------------------------------
  BETWEEN TR     0.13     1    0.13   51.72    0.00
  WITHIN  TR     0.15    56    0.00
  ------------------------------------------------
  TOTAL          0.28    57

  REJECT HO AT ALPHA = 0.05
  AT LEAST ONE OF THE MEANS IS NOT THE SAME AS OTHER MEANS


95% CONFIDENCE INTERVAL DIAGRAM

  +----------------------+----------------------+
      (-*-)                                        All SIC power MOSFETs samples and measurements
                        (----------*----------)    Random stochastic processes
  +----------------------+----------------------+
  1.51                    1.70                   1.88


SCHEFFE TEST (POST HOC COMPARISONS AMONG PAIRS OF MEANS)
  (ALPHA = 0.05)

   S - S       F   P(>F)    COMMENTS
  ------------------------------------
   1 - 2   51.72    0.00    MEAN 1 < MEAN 2
  ------------------------------------
```

**Figure 4.6.1.2: Results of the ANOVA analysis resulting from the comparison of the approximate entropies obtained from the noise data of the tested SiC power MOSFETs and the random signals of figure 4.6.1.1.**

```
KRUSKAL-WALLIS H TEST

  HO: SAMPLES CAME FROM THE SAME DISTRIBUTION
  HA: NOT HO  (ALPHA = 0.05)


   All noise measurements        Random data

   SUM     85.41 1540.0          5.31  171.0
   MEAN     1.55   28.0          1.77   57.0
   MED      1.56                 1.77
  ------------------------------------------


  H      = 8.39
  DF     = 1
  P(>H)  = 0.0038

  REJECT HO (SAMPLES DID NOT COME FROM THE SAME DISTRIBUTION)
  (ALPHA = 0.05)
```

**Figure 4.6.1.3: Results of the Kruskal-Wallis analysis resulting from the comparison of the approximate entropies obtained from the noise data of the tested SiC power MOSFETs and the random signals of figure 4.6.1.1.**

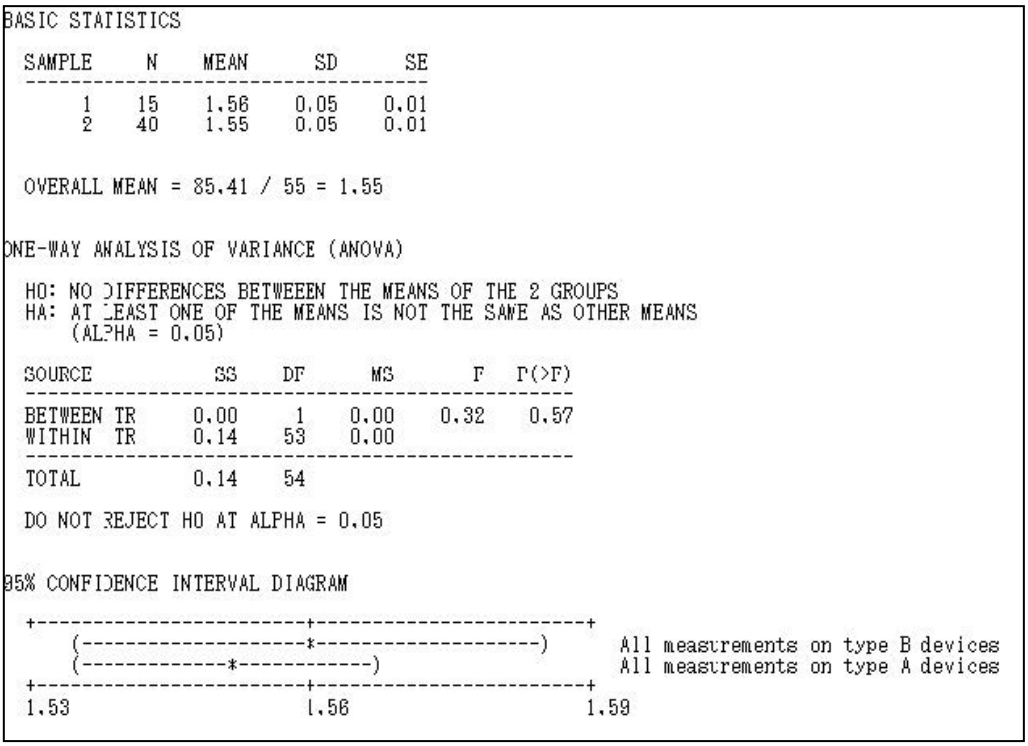



**Figure 4.6.1.4: Results of the ANOVA analysis resulting from the comparison of the approximate entropies obtained from the noise data of the tested SiC power MOSFETs of type A and type B.**

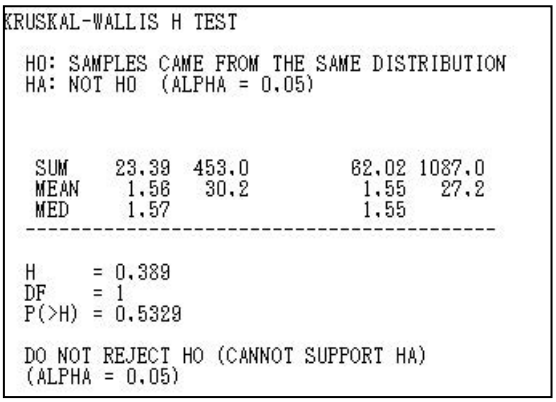
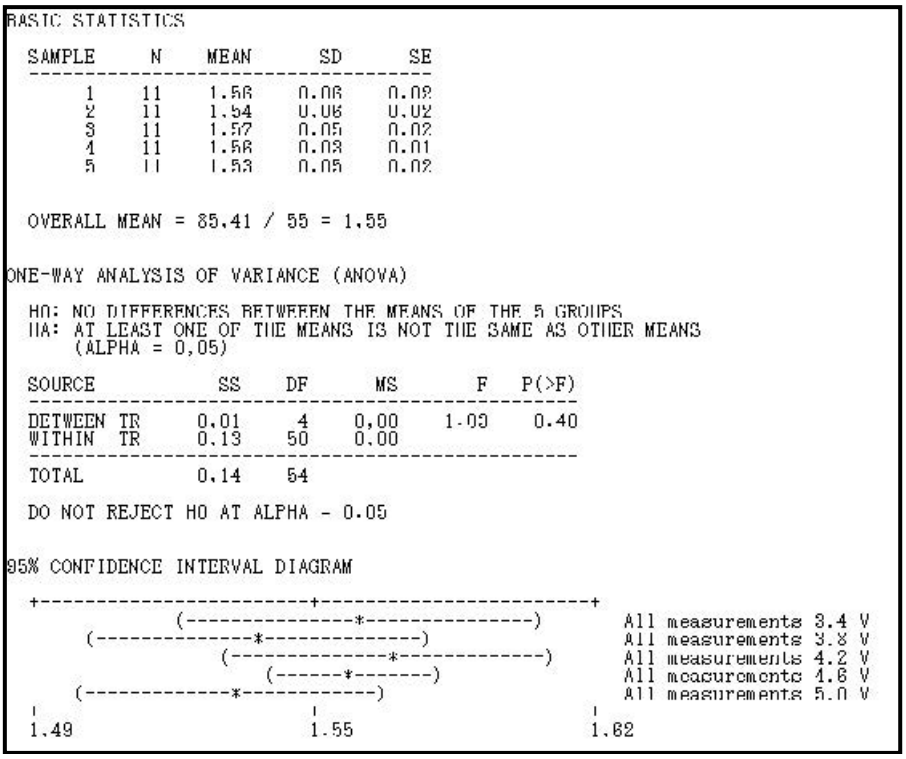



**Figure 4.6.1.5: Results of the Kruskal-Wallis analysis resulting from the comparison of the approximate entropies obtained from the noise data of the tested SiC power MOSFETs of type A and type B.**



BASIC STATISTICS

| SAMPLE | N | MEAN | SD | SE |
|---|---|---|---|---|
| 1 | 11 | 1.56 | 0.06 | 0.02 |
| 2 | 11 | 1.54 | 0.06 | 0.02 |
| 3 | 11 | 1.57 | 0.05 | 0.02 |
| 4 | 11 | 1.56 | 0.03 | 0.01 |
| 5 | 11 | 1.53 | 0.05 | 0.02 |

OVERALL MEAN = 85.41 / 55 = 1.55

ONE-WAY ANALYSIS OF VARIANCE (ANOVA)

H0: NO DIFFERENCES BETWEEN THE MEANS OF THE 5 GROUPS
HA: AT LEAST ONE OF THE MEANS IS NOT THE SAME AS OTHER MEANS
(ALPHA = 0.05)

| SOURCE | SS | DF | MS | F | P(>F) |
|---|---|---|---|---|---|
| BETWEEN TR | 0.01 | 4 | 0.00 | 1.03 | 0.40 |
| WITHIN TR | 0.13 | 50 | 0.00 | | |
| TOTAL | 0.14 | 54 | | | |

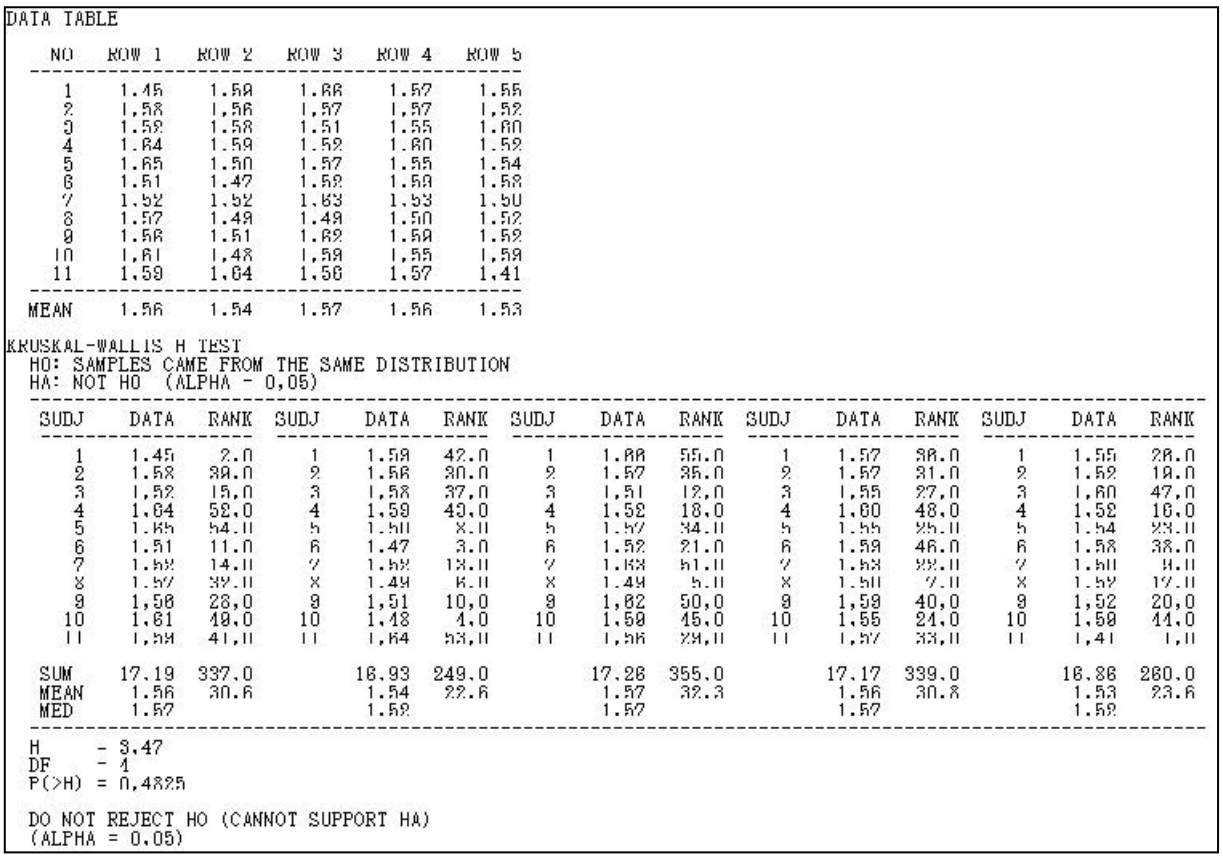
DO NOT REJECT H0 AT ALPHA = 0.05

95% CONFIDENCE INTERVAL DIAGRAM

All measurements 3.4 V
All measurements 3.8 V
All measurements 4.2 V
All measurements 4.6 V
All measurements 5.0 V

1.49 1.55 1.62

**Figure 4.6.1.6: Results of the ANOVA analysis resulting from the comparison of the approximate entropies obtained from the noise data of the tested SiC power MOSFETs by varying the $V_{GS}$.**



DATA TABLE

| NO | ROW 1 | ROW 2 | ROW 3 | ROW 4 | ROW 5 |
|---|---|---|---|---|---|
| 1 | 1.45 | 1.59 | 1.88 | 1.57 | 1.55 |
| 2 | 1.58 | 1.56 | 1.57 | 1.57 | 1.52 |
| 3 | 1.52 | 1.58 | 1.51 | 1.55 | 1.60 |
| 4 | 1.64 | 1.59 | 1.52 | 1.60 | 1.52 |
| 5 | 1.65 | 1.50 | 1.57 | 1.55 | 1.54 |
| 6 | 1.51 | 1.47 | 1.52 | 1.59 | 1.58 |
| 7 | 1.52 | 1.52 | 1.63 | 1.53 | 1.50 |
| 8 | 1.57 | 1.49 | 1.49 | 1.50 | 1.52 |
| 9 | 1.56 | 1.51 | 1.62 | 1.59 | 1.52 |
| 10 | 1.61 | 1.48 | 1.59 | 1.55 | 1.59 |
| 11 | 1.59 | 1.64 | 1.56 | 1.57 | 1.41 |
| MEAN | 1.56 | 1.54 | 1.57 | 1.56 | 1.53 |

KRUSKAL-WALLIS H TEST
H0: SAMPLES CAME FROM THE SAME DISTRIBUTION
HA: NOT H0 (ALPHA = 0.05)

| SUBJ | DATA | RANK | SUBJ | DATA | RANK | SUBJ | DATA | RANK | SUBJ | DATA | RANK | SUBJ | DATA | RANK |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1.45 | 2.0 | 1 | 1.59 | 42.0 | 1 | 1.88 | 55.0 | 1 | 1.57 | 38.0 | 1 | 1.55 | 28.0 |
| 2 | 1.58 | 38.0 | 2 | 1.56 | 30.0 | 2 | 1.57 | 35.0 | 2 | 1.57 | 31.0 | 2 | 1.52 | 19.0 |
| 3 | 1.52 | 15.0 | 3 | 1.58 | 37.0 | 3 | 1.51 | 12.0 | 3 | 1.55 | 27.0 | 3 | 1.60 | 47.0 |
| 4 | 1.64 | 52.0 | 4 | 1.59 | 43.0 | 4 | 1.52 | 18.0 | 4 | 1.60 | 48.0 | 4 | 1.52 | 16.0 |
| 5 | 1.65 | 54.0 | 5 | 1.50 | 8.0 | 5 | 1.57 | 34.0 | 5 | 1.55 | 25.0 | 5 | 1.54 | 23.0 |
| 6 | 1.51 | 11.0 | 6 | 1.47 | 3.0 | 6 | 1.52 | 21.0 | 6 | 1.59 | 46.0 | 6 | 1.58 | 33.0 |
| 7 | 1.52 | 14.0 | 7 | 1.52 | 13.0 | 7 | 1.63 | 51.0 | 7 | 1.53 | 32.0 | 7 | 1.50 | 8.0 |
| 8 | 1.57 | 32.0 | 8 | 1.49 | 6.0 | 8 | 1.49 | 5.0 | 8 | 1.50 | 7.0 | 8 | 1.52 | 17.0 |
| 9 | 1.56 | 28.0 | 9 | 1.51 | 10.0 | 9 | 1.62 | 50.0 | 9 | 1.59 | 40.0 | 9 | 1.52 | 20.0 |
| 10 | 1.61 | 49.0 | 10 | 1.48 | 4.0 | 10 | 1.59 | 45.0 | 10 | 1.55 | 24.0 | 10 | 1.59 | 44.0 |
| 11 | 1.59 | 41.0 | 11 | 1.64 | 53.0 | 11 | 1.56 | 29.0 | 11 | 1.57 | 33.0 | 11 | 1.41 | 1.0 |
| SUM | 17.19 | 337.0 | | 16.93 | 249.0 | | 17.26 | 355.0 | | 17.17 | 339.0 | | 16.86 | 260.0 |
| MEAN | 1.56 | 30.6 | | 1.54 | 22.6 | | 1.57 | 32.3 | | 1.56 | 30.8 | | 1.53 | 23.6 |
| MED | 1.57 | | | 1.52 | | | 1.57 | | | 1.57 | | | 1.52 | |

H = 3.47
DF = 4
P(>H) = 0.4825

DO NOT REJECT H0 (CANNOT SUPPORT HA)
(ALPHA = 0.05)

**Figure 4.6.1.7: Results of the Kruskal-Wallis analysis resulting from the comparison of the approximate entropies obtained from the noise data of the tested SiC power MOSFETs by varying the $V_{GS}$.**

## 4.6.2 Experimental results obtained from low frequency noise measurements carried out on the tested SiC power MOSFETs

After discussing the method of how to perform low frequency measurements of the devices to be tested and descripting in detail the amplifier module, which is the heart of the experiment, we will introduce and analyse the experimental results obtained by the tested devices belonging to the two families of SiC power MOSFETs previously studied in chapter 4.2 and chapter 4.3. Once again, it is important to highlight that all the precautions indicated in chapter 4.6 have been taken in the noise tests performed on the analysed devices. First of all, it is important to underline that preliminary analyses were performed on the board by disconnecting the device under test in order to measure the noise level of the amplifier module and subsequently evaluate if this level is rather lower than noise signal coming from the SiC power MOSFETs analysed. The results of the preliminary analyses have shown that effectively the noise level coming from the board is some orders of magnitude lower than the noise signal coming from the SiC power MOSFETs and this guarantees that the analyses carried out on the tested devices are not significantly influenced. It is important to highlight that the most important contribution of noise coming from the amplifier module is due to the feedback resistance of the transimpedance stage, as underlined by Magnone [299]. In fact, the PSD observed in the spectrum analyser is a white noise due to the thermal noise of the feedback resistance. The observed thermal noise level changes its average value as the value of the feedback resistance varies and, in particular, it increases as the resistance increases and this demonstrates that it is the main cause of the observed phenomenon. Instead, by shorting the feedback resistance, it is possible to observe the PSD of the noise signal coming manly from the low noise OP AMPs which is significantly lower than the PSD of the feedback resistance. The PSD of the noise signal observed during this last preliminary test was compared with the PSD of the signal indicated in the TLC2201 datasheet confirming the origin of the noise. This consideration is based on the assumption that, as will be seen later by studying the signal in the time domain, the electrical noise of the $V_{DS}$ of the device is ergodic and there are statistically relevant autocorrelation values up to times of 1ms, that is, up to frequencies of $10^3$ Hz. Furthermore, it will be demonstrated by the graphs that will be shown below that, taking into account that the signal will be analyzed for frequency intervals up to $10^4$ Hz and for $V_{GS}$ higher than 3V, the background noise is certainly negligible compared to the noise emitted by the Power MOSFET in SiC. Therefore, to simplify the whole analysis, the results of these preliminary experiments will not be shown in this chapter because we will focus the attention on the experimental results obtained from the tested power devices. In our experiments, different measurements were carried out by varying the gate voltage applied on the devices under test from 3 V to 5 V in steps of 400 mV while the drain voltage was set at 50 mV. Furthermore, we optimized the width of the DSA spectrum analyser window function by setting it to 1 s, which includes 4096 measuring points. The noise measurements were obtained after a time interval of 80 s, thus, the PSD values were averaged in 80 different and subsequent detections. Before introducing the results obtained from these tests, it is necessary once to underline what kinds of answers we would like to obtain from the questions that can be asked by observing the experiments. Does the PSD measured in the SiC power MOSFETs effectively look like pink noise? Does the PSD level, which measures the amount of interface defects, increases as the gate voltage increases as observed in PBTI and threshold voltage instability measurements? What is the main mechanism causing the noise signal observed in SiC power MOSFETs? First of all, it is important to note that the measurements obtained from all samples of the two families of SiC power MOSFET devices analysed showed the same behaviour in terms of PSD and that only small differences in PSD levels were observed considering the same polarization conditions.

The latter observed behaviour demonstrates that the mechanism, or mechanisms, involved in the creation of the noise signal is the same but, in this process, different quantities of defects are involved in the interface depending on the tested device. However, it is necessary to consider that the threshold voltage of each device is slightly different from the others, thus, the response of each of these devices to the same gate polarization can be affected. In any case, the purpose of this analysis is not to compare exactly the defect levels between the tested devices but, rather, to understand if there are different mechanisms involved in the observed phenomenon between the analysed devices. By a way of example, in figure 4.6.2.1 the spectrum of the drain voltage noise signal expressed by $V^2Hz^{-1}$ of piece 6 of the type A device working in the triode operating condition carried out at room temperature for the different polarization conditions of the gate as previously explained is shown. Based on the experimental results obtained from piece 6 of the type A device, which is similar to the other components tested, it is possible to answer to two previous questions, that is, the spectrum as a function of frequency effectively resembles a pink noise and, moreover, increasing the gate bias also increases the PSD level as expected. In fact, referring to the PSD level as the $V_{GS}$ changes, it was seen, for example in chapter 3.2, that the voltage spectrum in the McWhorter model, as expressed in Eq. (3.2.15), depends on the number of the traps involved in the process. Therefore, the greater the number of traps that charge and discharge, the higher the spectrum noise signal. As already shown in chapter 2.2.5, referring to figure 2.2.5.1, Afanasev has demonstrated that the involved defects in the phenomenon in the interface between the SiC and oxide layers increases strongly when $E_F$ approaching the $E_C$ edge. Furthermore, in chapter 4.4, referring to figure 4.4.4, we simulated the same phenomenon by means of a TCAD analysis on the basis of the experimental results obtained by implementing our hysteresis and PBTI tests. Considering that the greater the gate bias the more $E_F$ approaches the $E_C$, then, we can confirm that the results observed in low frequency analysis carried out on the piece 6 of the type A device are consistent with what was expected and with what experimentally observed in our previous tests.

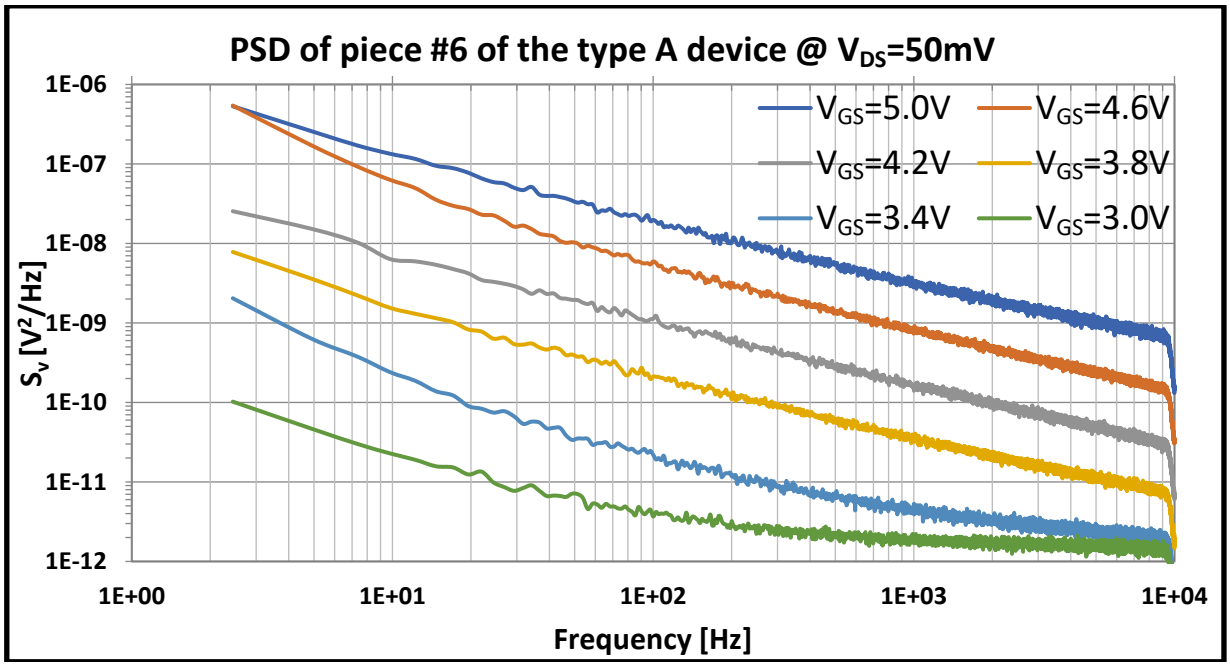



**Figure 4.6.2.1: PSD of the drain voltage noise signals of piece 6 of the type A device carried out at room temperature for various polarizations of the $V_{GS}$ setting the $V_{DS}$ to 50 mV (The signal is detected at the output of the second AC amplification stage as shown in figure 4.6.9 and can be mathematically obtained from the expression (4.6.74).**

Furthermore, in chapter 4.2, from the point of view of the border traps, it has been shown that the capture and emission events of electrons from the oxide traps depend on the respective energy barriers as indicated in Eq. (4.2.9) and Eq.(4.2.10) and, thus, the greater the gate bias, the greater the energy available which allows to increase the quantity of the charges that is exchanged between the dielectric and the channel of the MOSFET. And again, even if the spectrum of the noise signal resembles a pink noise, it is very important to estimate the slope of the lines drawn in figure 4.6.2.1 to evaluate exactly some aspects of the interface characteristics. With reference to Eq. (3.1.4.8), applying the logarithmic function to the spectrum of a flicker noise, we see how the PSD depends linearly on the frequency and that the slope can be easily extrapolated. Therefore, by way of example, as shown in figure 4.6.2.2, from figure 4.6.2.1 we have extrapolated the characteristic to $V_{GS}$ equal to 5 V and, thus, we evaluated the slope of the line in the frequency range of 20 Hz – 4000 Hz. In this frequency range the curve looks more like a straight line. In fact, as will be better shown later, the noise signal for very low frequencies is influenced by the discharge effect of the capacitors placed in the amplifier module while, at higher frequencies, the noise signal may begin to be affected by other mechanisms such as thermal noise and shot noise. From this figure, it is possible to observe that in the frequency range indicated above the curve appears as a straight line and its estimated slope is 0.74 lower than 1 as expected for a pure pink noise signal. Haartman in his studies [235] states that when the slope is equal to 1, the traps are uniformly distributed within the oxide starting from the interface going deeper and deeper. When the estimated slope is less than 1, as in our case, the traps are not uniformly distributed and their density is greater close the interface rather than going deep in the oxide. Finally, if the slope is higher than 1, the traps are not uniformly distributed in the oxide and their density increases by going deeper and deeper into the oxide. As already seen in chapter 3.2, in accordance with the theory of WKB [250] and also explained by Haartman [235], the noise signal observed in the range from $10^{-2}$ Hz to $10^{6}$ Hz is due to traps that charge and discharge within a depth ranging from 0.7 nm to about 2.6 nm and this is also the thickness of the transition layer estimated in the SiC power MOSFETs tested in this work (see figure 4.5.1 in chapter 4.5 extrapolated from the Fiorenza et al. work [296]).

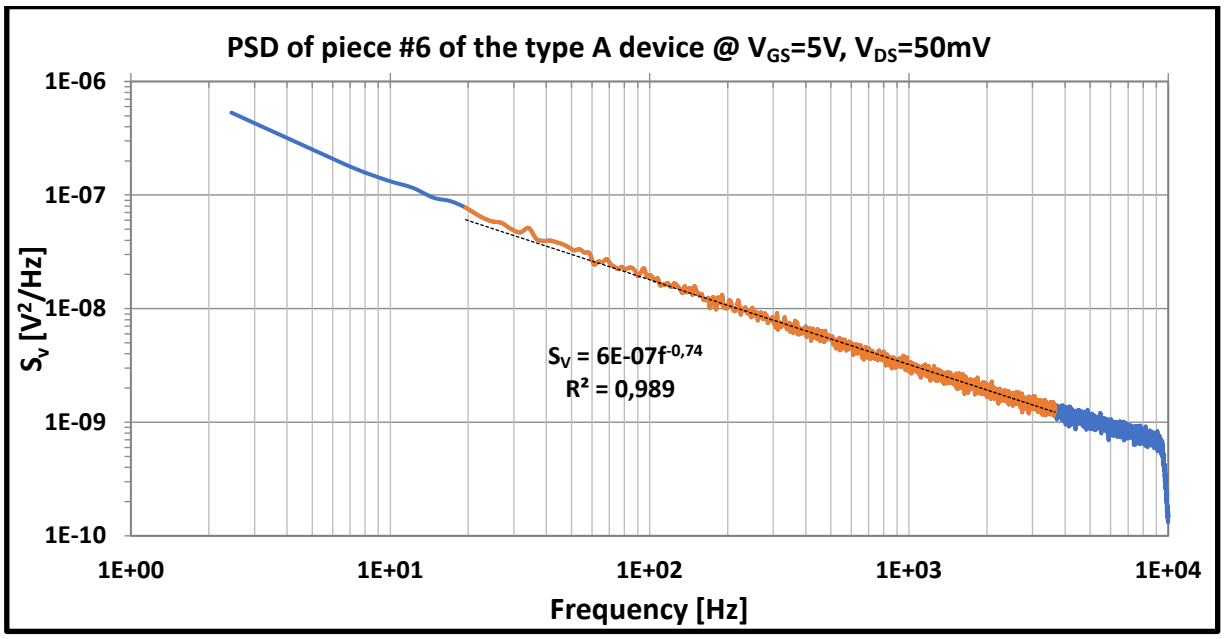



**Figure 4.6.2.2: PSD of the voltage noise signal of piece 6 of the type A device obtained at room temperature by setting the $V_{GS}$ to 5 V and the $V_{DS}$ to 50 mV which highlights the linear trend of the curve in the frequency range from 33 Hz to 3300 Hz.**

However, in our test the frequency bandwidth is contained within $10^4$ Hz because the time of the window function has been set to 1 s. Thus, we can predict the spectrum even beyond $10^4$ Hz since it is rather linear with increasing frequency. Again, according Haartman's experiments [235], traps placed too close to the interface are too fast to be observed in flicker noise, while traps located more than about 3 nm away from the interface are too slow to contribute to the noise signal. It is important to underline that the estimated current flowing in the MOSFET channel of the analysed sample in the operating condition represented in figure 4.6.2.2 and passing through $R_F$ is equal to 1.01 mA. It has been estimated considering the DC voltage at the output of the transimpedance stage as (where 0.05 is the voltage offset):

$$I_{R_F} = \frac{V_{out} - 0.05}{R_F} \qquad (4.6.2.1)$$

This latter was measured by the second amplification stage connected in the voltage follower configuration, taking into account that the OP AMP present in this stage has an offset voltage of 1 mV estimated short circuiting the input terminals of the amplifier.
The noise spectrum can also be shown in terms of the current flowing in the MOSFET and this is obtained by dividing the PSD in terms of voltage with the gain square of the entire amplifier module which is equal to 101000 (see figure 4.6.2.3). Finally, by way of example, the graph of the PSD normalized as a function of the gate voltage overdrive in the log-log scales for piece 6 of the type A device by setting the frequency at 100 Hz is shown in figure 4.6.2.4. From this figure it is possible to observe that the curve is very similar to a straight line having a slope equal to about -2. In chapter 3.2, with reference to Eq. (3.2.12), by applying the logarithmic function, it is possible to obtain:

$$\ln\left(\frac{S_I}{{I_{ds}}^2}\right) = \ln\left(\frac{q^2\lambda^* KTN_t(E_F)}{f^{\gamma^*} WLC_{ox}{}^2}\right) - 2\ln(V_{GS} - V_{th}) \qquad (4.6.2.2)$$

The Eq. (3.2.12) refers to the normalized PSD of the number fluctuation model.

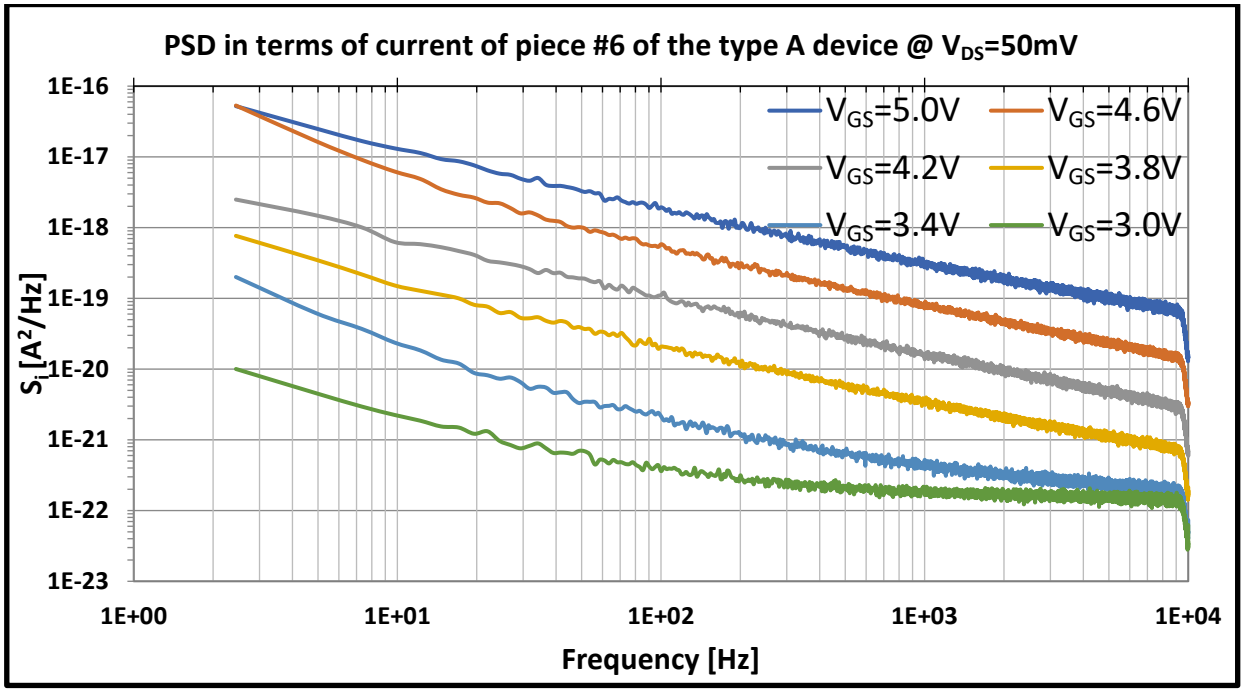



**Figure 4.6.2.3: PSD in terms of current of the noise signal of piece 6 of the type A device carried out at room temperature for various polarizations of the $V_{GS}$ setting the $V_{DS}$ to 50 mV.**

Therefore, considering that the estimated slope of the straight line in figure 4.6.2.4 is equal to -2 as well as the coefficient of the logarithmic term of the gate voltage overdrive in Eq. (4.6.2.2), it is possible to state that the main mechanism involved in detecting the flicker noise of the tested SiC power MOSFETs is due to the exchange of charges between the oxide traps and the device channel as theorized in the McWhorter model. In fact, similar slopes have been obtained in all tested devices as shown in figure 4.6.2.5 where the graph reports other examples of type A devices. However, based on these experimental results, one might wonder why the fluctuation of the electron mobility, as theorized in the Hooge model, is not primarily involved in the explanation of this phenomenon. Given an answer to this question is very difficult even if Fiorenza et al. in their work [296] argue that the electron mobility in the channel of the SiC power MOSFETs is strongly reduced also because it depends on the compressive stress produced in the interface during the growth of the $SiO_2$ on the 4H-SiC substrate. In fact, these materials have very different temperature expansion coefficients and the compressive stress applied on the 4H-SiC reticule reduces the average atom folding distance and this leads to a decrease in the average time between two electron impacts with the crystalline structure and, thus, this greatly influences the mobility of the carriers. It is important to note that the graphs of figure 4.6.2.4 and of figure 4.6.2.5 can be obtained after $V_{th}$ has been carefully estimated for each device analysed.

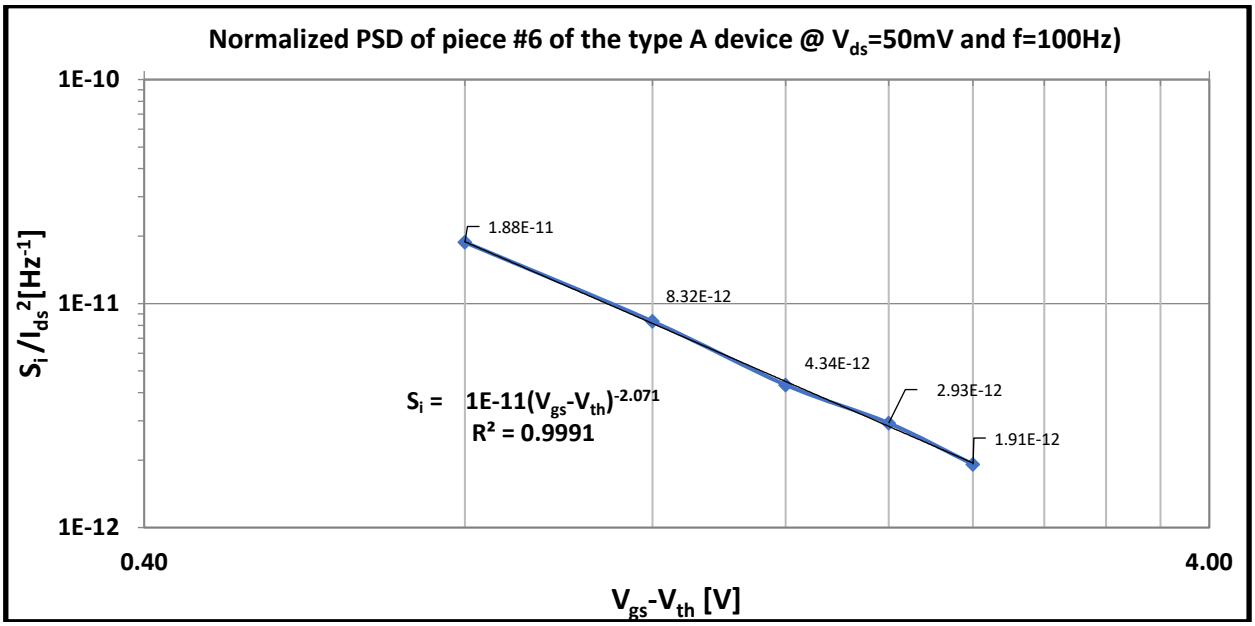



**Figure 4.6.2.4: Normalized PSD of the noise signal as a function of the gate voltage overdrive of piece 6 of the type A device carried out at room temperature by setting the $V_{DS}$ to 50 mV and the f to 100 Hz.**

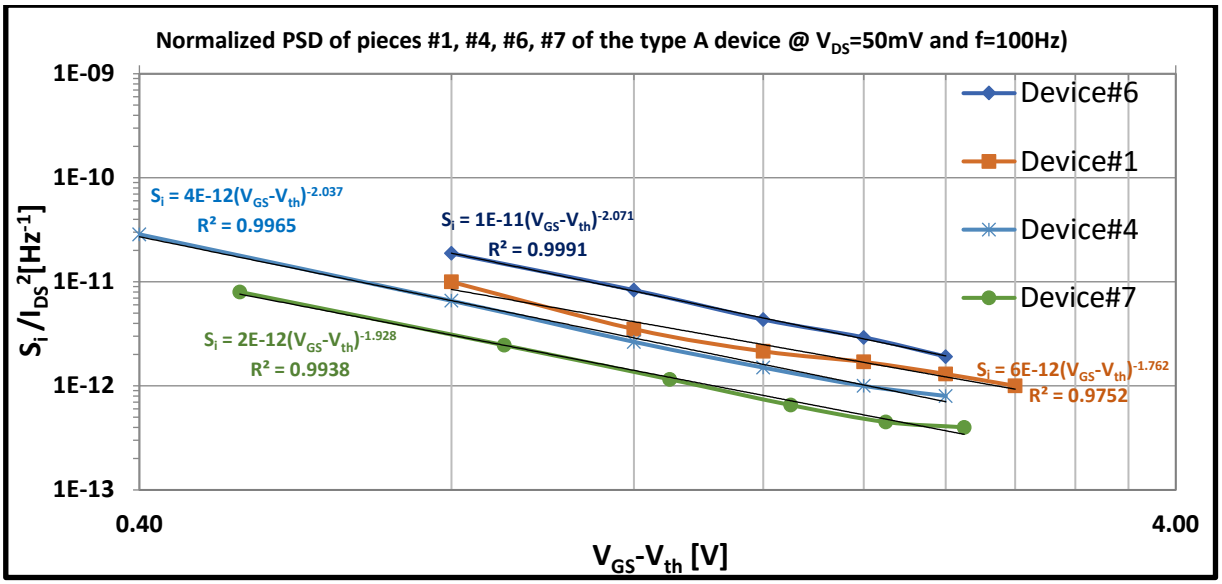



**Figure 4.6.2.5: Normalized PSD of the noise signal as a function of the gate voltage overdrive of piece 1, 4, 6 and 7 of the type A device carried out at room temperature by setting the $V_{DS}$ to 50 mV and the f to 100 Hz.**

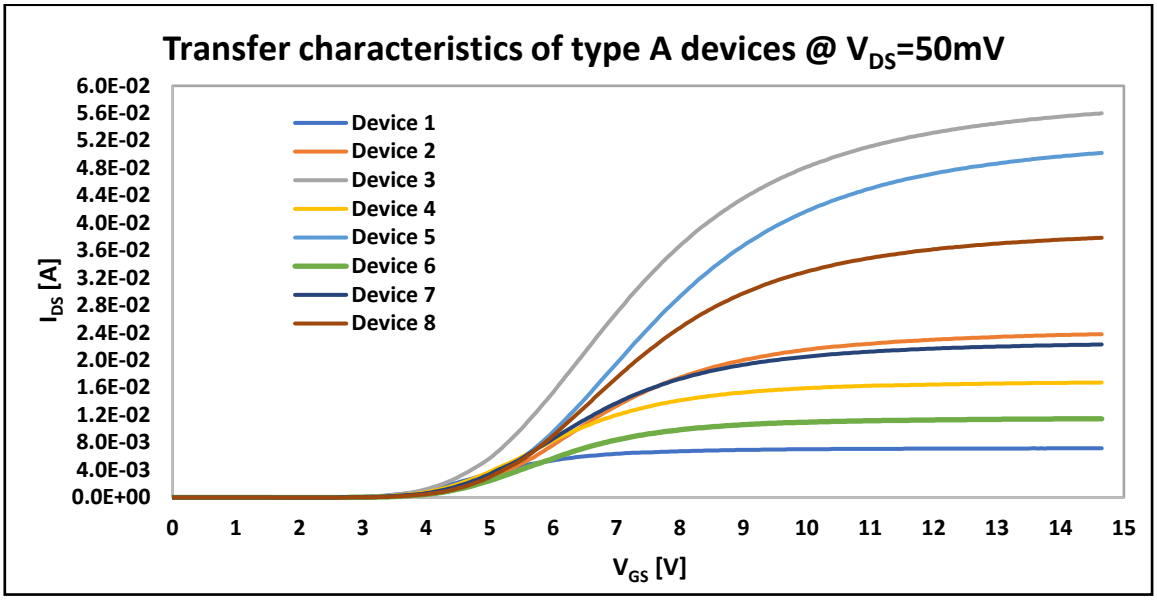



**Figure 4.6.2.6: Transfer characteristics of type A devices by setting $V_{DS}$ to 50 mV.**

In fact, even changing the estimated $V_{th}$ slightly, the straight lines begins to becomes curves and the mechanism that explains the observed phenomenon cannot longer be classified. In order to accurately estimate the $V_{th}$ of the tested devices, the Williams method [123] were used as described in chapter 4.2. It is a good method to use when, in particular, it is necessary to extrapolate the threshold voltage of the power MOSFETs. In the Williams method, the graph of $g_{fs}$ as a function of $V_{GS}$ is obtained for each tested device. From these graphs, it is important to identify the point where $g_{fs}$ starts to grow exponentially with the growth of the $V_{GS}$, thus, this point on the x axis is the $V_{th}$. By a way of example, in figure 4.6.2.6 and figure 4.6.2.7, the transfer characteristics of the whole set of samples of the type A family and of the type B family analysed in these tests are shown.

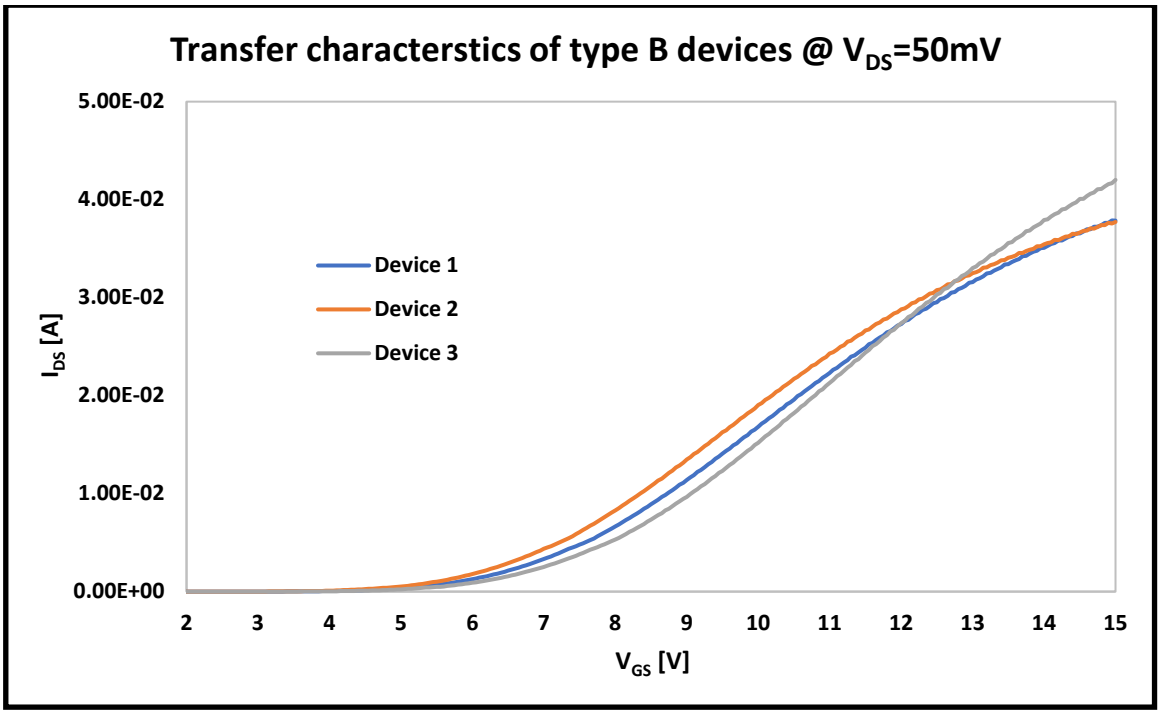



**Figure 4.6.2.7: Transfer characteristics of type B devices by setting $V_{DS}$ to 50 mV.**

On the other hand, in figure 4.6.2.8 and figure 4.6.2.9, the graphs of the $g_{fs}$ as a function of $V_{GS}$ are shown for both the families of devices in question whose data have been extrapolated from the respective transfer characteristics. From the latter graphs, it is possible to estimate that for type A devices the $V_{th}$ is in a small range of 2.5 V while, for the type B devices, the $V_{th}$ is in a small range of 3.0 V.

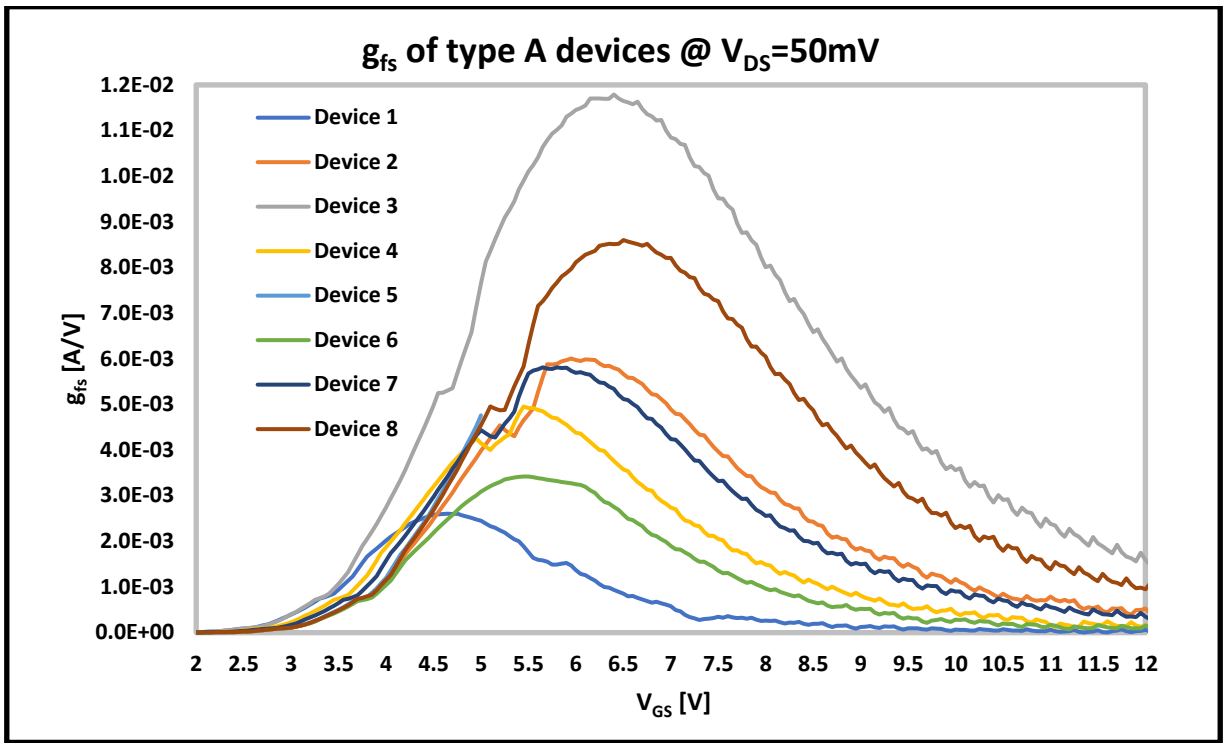



**Figure 4.6.2.8: $g_{fs}$ of type A devices by setting $V_{DS}$ to 50 mV.**

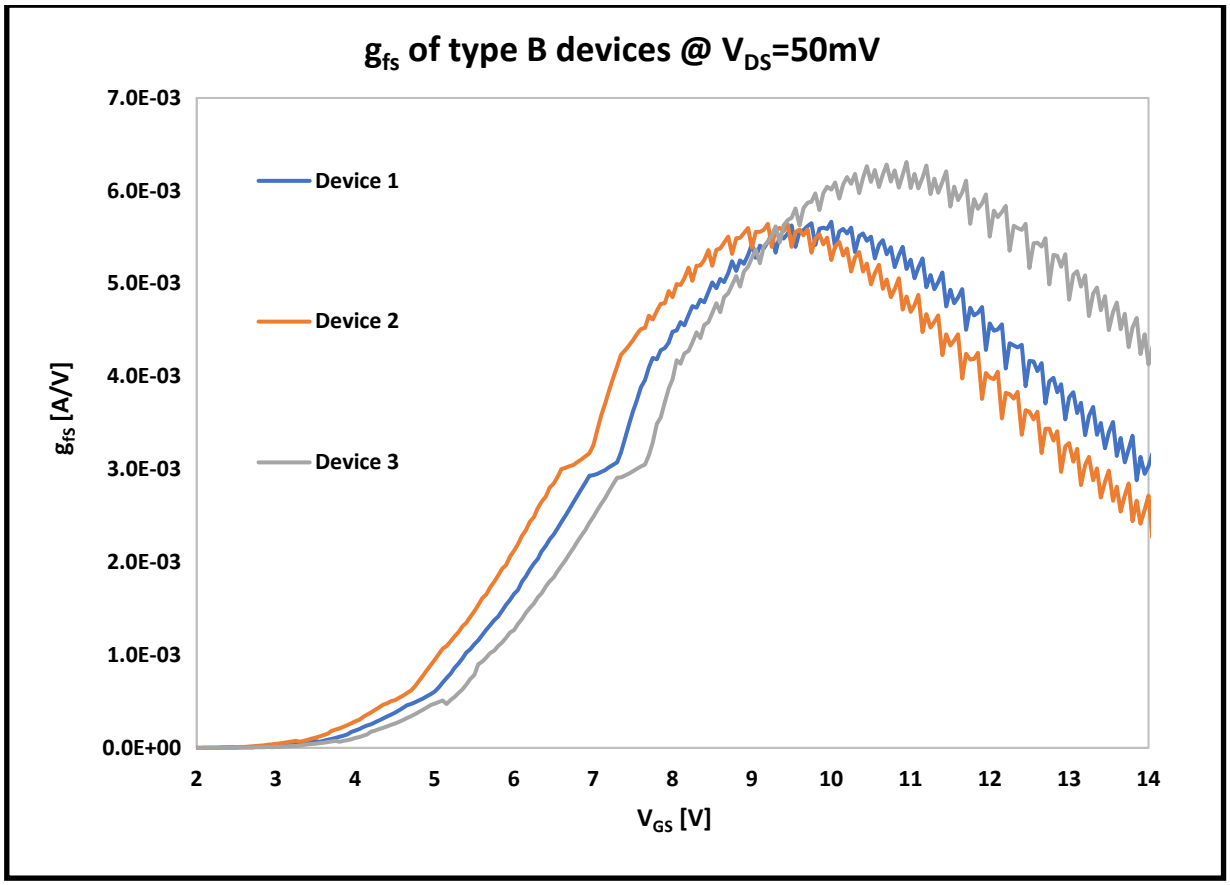



**Figure 4.6.2.9: $g_{fs}$ of type B devices by setting $V_{DS}$ to 50 mV.**

## 4.6.3 The low frequency noise studied from the point of view of the time analysis of the tested SiC power MOSFETs

After studying the low frequency noise observed in SiC power MOSFETs tested in the frequency domain, we will now focus our attention on the same signals analysed in the time domain to try to obtain further insights that have not been observed previously. As already mentioned, we have analysed the noise coming from the tested devices with an NI software called DSA which is equipped with a graphical interface where it is possible to observe the signals both the frequency and time domain. As will become clear later in this chapter, from this analysis it is possible to estimate the depth inside the oxide within which the process of capture and release of electrons influences the noise signal. However, while the time domain signal is detected in real time, the frequency domain signal is averaged after each window function frame consisting of 4096 measuring points for 1 s. This allows us to more effectively detect any persistence events of the noise signal. The DSA software allows us to extrapolate and save in a file the data of the averaged noise signal in the frequency domain, but from that is not possible to extrapolate the raw data of the signal in the time domain. Therefore, we can only obtain data in the time domain from the same data in the frequency domain via the latter's FFT. These latter data in the time domain will not be in real time but averaged like those in the frequency domain. This FFT transformation was performed using the MATLAB software taking into account the fact that in the time domain the signal will be periodic with a period equal to 1s, consisting of 4096 measuring points, and perfectly symmetrical at 0.5s with reference to point 2048 of the measurement. By way of example, in figure 4.6.3.1 the noise signal averaged in 80 window function frames in the time domain for piece 6 of type A device is shown by setting the $V_{GS}$ at 5 V and the $V_{DS}$ at 50 mV for the first 2048 measuring points. From this graph, it is possible to observe that the signal is strongly influenced in the very first moments by transient phenomena also related to the discharging of the intrinsic capacitances of the MOSFET when the buttons P1 and P2 in figure 4.6.8 are switched on to polarize the gate and the drain terminal of the devices. However, subsequently, the signal shows a slight tendency to decrease over time due to the discharge of the capacitances and batteries present in the amplifier module. In any case, to better highlight the noise signal coming from the charge and discharge events of the electrons from the oxide traps due to the mechanism described by the number fluctuation model as shown in chapter 4.6.2, we consider figure 4.6.3.2 where the same signal of the figure 4.6.3.1 is represented in the time interval between the measuring points 1300 and 2048. The amplitude of the noise signal shown in figure 4.6.3.2 is similar to that observed in the graph of the interface of the DSA in real time and is in the order of few $10^{-4}$ V and the time scale in the x-axis is shown as a function of the increasing number of measurement events. Furthermore, the signal shows a slight offset voltage due to the output stage of the amplifier module which, however, does not influence the analysis that will performed later. It is important to highlight that the analysis performed in the time domain of the noise signal will be performed using the open source software GRETEL which provides graphical user interface. By way of example, for the signal shown in figure 4.6.3.2, a AR(1) model has been Implemented through the GRETEL software, as described in chapter 3.6.2. The results of the comparison between the AR(1) function, as described in Eq. (3.6.2.5), obtained by applying the statistical package X-13 ARIMA, and the real noise signal is shown in figure 4.6.3.3. Furthermore, the estimated parameters of the AR(1) process obtained by GRETEL is shown in figure 4.6.3.4. Now, it is necessary to better explain the results of this simulation to understand the phenomenon.

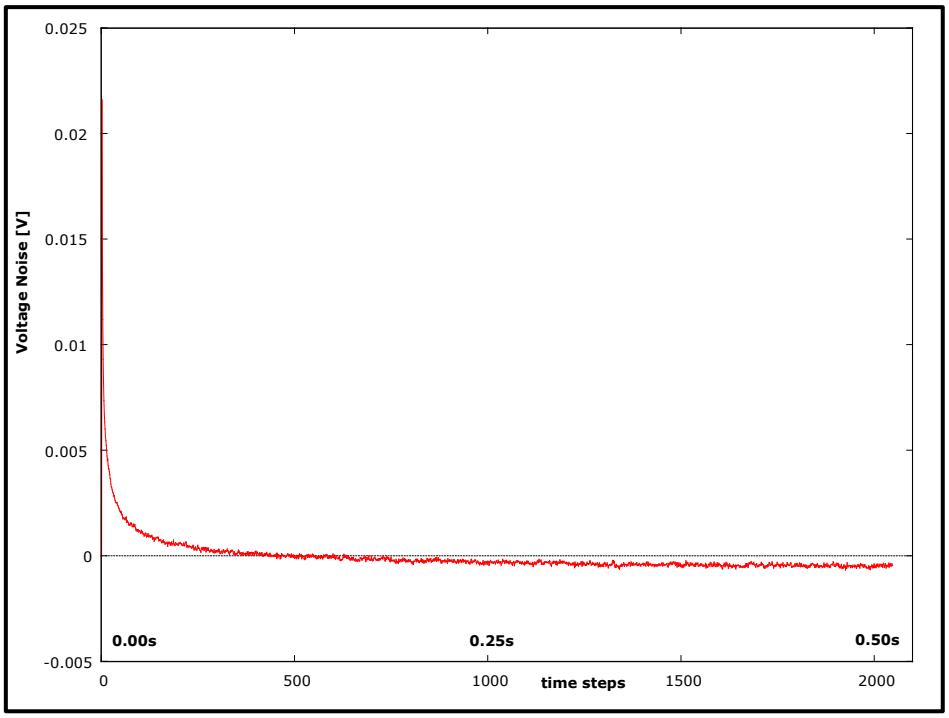



**Figure 4.6.3.1: Noise signal averaged in 80 window function frames in the time domain for piece 6 of type A device by setting the $V_{GS}$ at 5 V and the $V_{DS}$ at 50 mV for the first 2048 measuring points.**

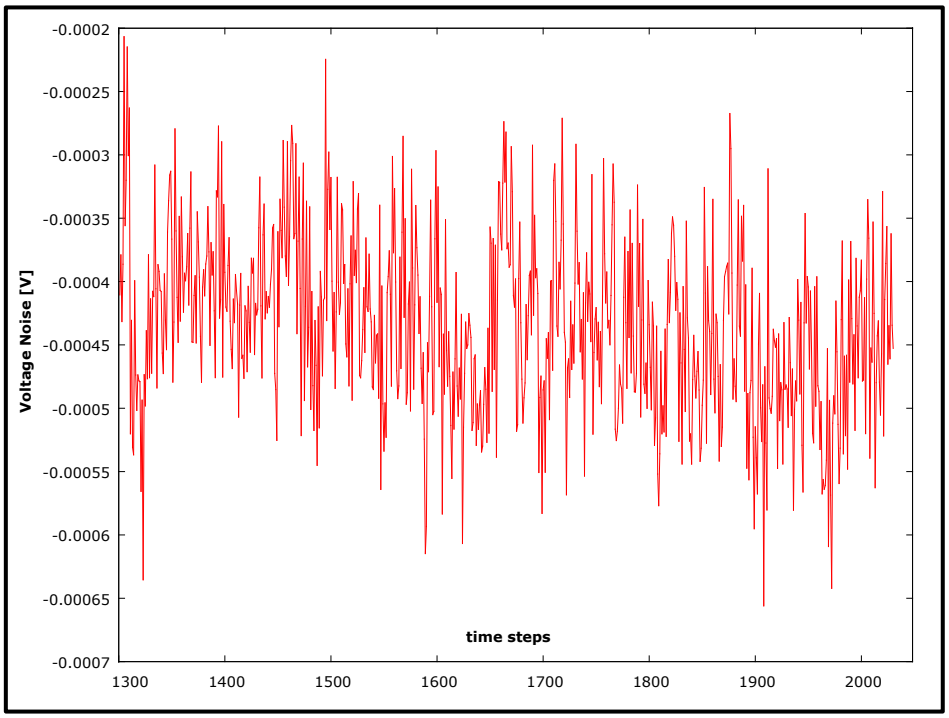



**Figure 4.6.3.2: Noise signal averaged in 80 window function frames in the time domain for piece 6 of type A device by setting the $V_{GS}$ to 5 V and the $V_{DS}$ to 50 mV in the time interval between the measuring points 1300 and 2048 (stationary conditions).**

The model AR(1), as described in Eq. (3.6.2.5), is composed of the sum of a deterministic part, which depends on the product between the value assumed by the variable in the instant immediately before and its linear regression coefficient, and a stochastic part which is represented by a stochastic variable determined by independent events that has a normal distribution with average value equal to zero and a certain variance typical of the phenomenon that is observed.

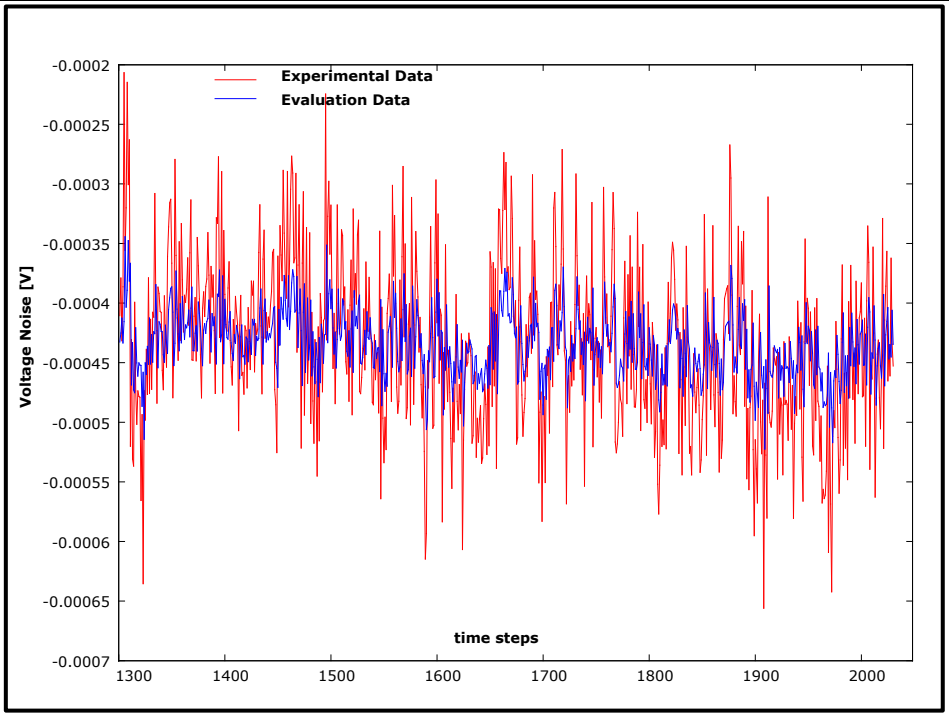



**Figure 4.6.3.3: Comparison between the real noise signal coming from the tested SiC power MOSFET and the AR(1) function obtained by the GRETEL software and optimized with X-13 ARIMA (stationary conditions).**

gretl: model

File Modifica Test Salva Grafici Analisi LaTeX

Model X-13-ARIMA

| | coefficient | errore std. | z | p-value | |
|---|---|---|---|---|---|
| const | -2.94251e-08 | 4.66763e-06 | -0.006304 | 0.9950 | |
| phi_1 | 0.259822 | 0.0367114 | 7.077 | 1.47e-012 | *** |
| phi_2 | 0.129287 | 0.0376492 | 3.434 | 0.0006 | *** |
| phi_3 | 0.125838 | 0.0367782 | 3.422 | 0.0006 | *** |

| | | | |
|---|---|---|---|
| dependent variable mean | -1.04e-07 | E.S. var. dipendent | 0.000067 |
| Average-likelihood | 1,03e-08 | E.S. innovations | 0.000061 |
| Log-likelihood | 6044,559 | Akaike criterion | -12079,12 |
| Schwarz criterion | -12056.15 | Hannan-Quinn | -12070.26 |

E.S. = errore standard

| | | Real | Immaginary | Modul | Freq |
|---|---|---|---|---|---|
| AR | | | | | |
| Root | 1 | 1.4272 | 0.0000 | 1.4272 | 0.0000 |
| Root | 2 | -1.2273 | 2.0154 | 2.3597 | 0.3371 |
| Root | 3 | -1.2273 | -2.0154 | 2.3597 | -0.3371 |

**Figure 4.6.3.4: Table summarizing the results of the parameters estimated with the AR(1) model via X-13 ARIMA for the noise signal from the tested SiC power MOSFET.**

Therefore, the expected value of Eq. (3.6.2.5) is given by Eq. (3.6.2.6) and should be equal to zero in a zero average stochastic process even if, in our case, it is equal to $-4.3 \times 10^{-4}$ due to the voltage offset of the output stage of the amplifier module as estimated by the parameter “const” shown in figure 4.6.3.4. By a way of example, if in Eq. (3.6.2.5) we eliminate the stochastic part, the equation will be represented only by the deterministic part which represents a curve similar to a discharge event having a power law tendency if the linear regression coefficient is less than 1 as we have estimated in our example.

However, when the stochastic part is introduced, which is a combination of many independent events with zero mean, the process becomes completely random as shown in figure 4.6.3.3. In chapter 3.6, we saw that Granger [259] describes a flicker noise as a sum of infinite AR(1) processes or, at least, an adequate number of finite AR(1) processes [260]. The Granger's conclusions are the same as those mathematically obtained by Bernamont [245], discussed in chapter 3.1.4, and by Pobegen and Grasser in their experiments [273], discussed in chapter 4.3. Therefore, only an AR(1) process, as introduced in our preliminary analysis, cannot explains the observed phenomenon well unless there is a predominant number of oxide traps placed at the same distance from the interface with similar time constants. However, this is not the case, also because the p-values of the estimated "const" parameter and, in particular, "phi_1" parameter, the latter is the linear regression coefficient, are very low even if the parameter "Root 1", the root of the matrix A(**L**) in Eq. (3.6.2.4), is greater than 1, thus, the process should be stationary. Therefore, to accurately model the phenomena of charging and discharging electrons from the oxide traps towards the MOSFET channel, we should estimate the parameters of many AR(1)-type processes and add them together. In fact, even if, at least graphically, figure 4.6.3.3 shows a good matching between the real and modeled data, the latter conclusion can be confirmed from the following analysis. First of all, we calculate the residues obtained from the difference between the real data and that simulated by the AR(1) process (see figure 4.6.3.5). Subsequently, we analyse the distribution of these residues to verify if they are randomly distributed according to a normal one and considering a statistical significance level equal to 95% (see figure 4.6.3.6). The statistical test $\chi^2$ was carried out to check if the residues have a normal distribution while, to check if there are correlations over time between the events observed, the Auto-Correlation Function, ACF, and Partial Auto-Correlation Function, PACF, were obtained (see figure 4.6.3.7). It is important to understand the difference between ACF and PACF functions. The ACF function estimates the correlation between two different events shifted over time of the original signal while the PACF performs the same analysis on the modify original signal eliminating any trend effects observed from it. From figure 4.6.3.6, based on $\chi^2$ test, it is possible to observe that statistically the residues are normally distributed with zero mean and a variance equal to $6.41 \times 10^{-5}[V^2]$. Unfortunately, both the similar ACF and PACF graphs represented in figure 4.6.3.7 show that residues are statistically correlated with each other, thus, it is necessary to consider another model to better simulate the real data observed. To understand which model best simulates the experimental results, the graphs of the ACF and PACF functions of the previous noise signal were obtained as shown in figure 4.6.3.8. The latter graphs show that autocorrelations of the functions ACF and PACF differ because there is a trend in the signal. However, considering the PACF graph that does not take into account the presence of a trend in the signal, it is possible to observe that the noise shows a persistence and that the process is ergodic. It is important to underline that there is a statistically significant correlation up to the third event after the observe data and, thus, the outcome of each data was conditioned by the three events that occurred previously. In terms of time interval, there is a significant correlation up to events that occurs within about 1 ms. Therefore, the very fast events due to the capture and emission of electrons from the oxide traps placed within one nanometer are mainly involved (based on the Lelis method and considering figure 4.3.13, within 0.7-1.0 nm from the interface). On the basis of the latter results, it is possible to assume that a AR(3) process could be used successfully to simulate the noise signal as shown in figure 4.6.3.9. It is important to underline that a stochastic process AR(3) could be thought of as the sum of three AR process having a lag of 1, 2 and 3 sampling time intervals respectively and a white noise with mean equal to zero and a certain variance. The estimated parameters of the AR(3) process are shown in figure 4.6.3.10. Based on the results summarized in figure 4.6.3.10, the AR(3) model that describes the noise signal can be written as:

$$x_t = 0.286\, x_{t-1} + 0.152\, x_{t-2} + 0.153\, x_{t-3} - 0.00043 + \varepsilon_t \qquad (4.6.3.1)$$

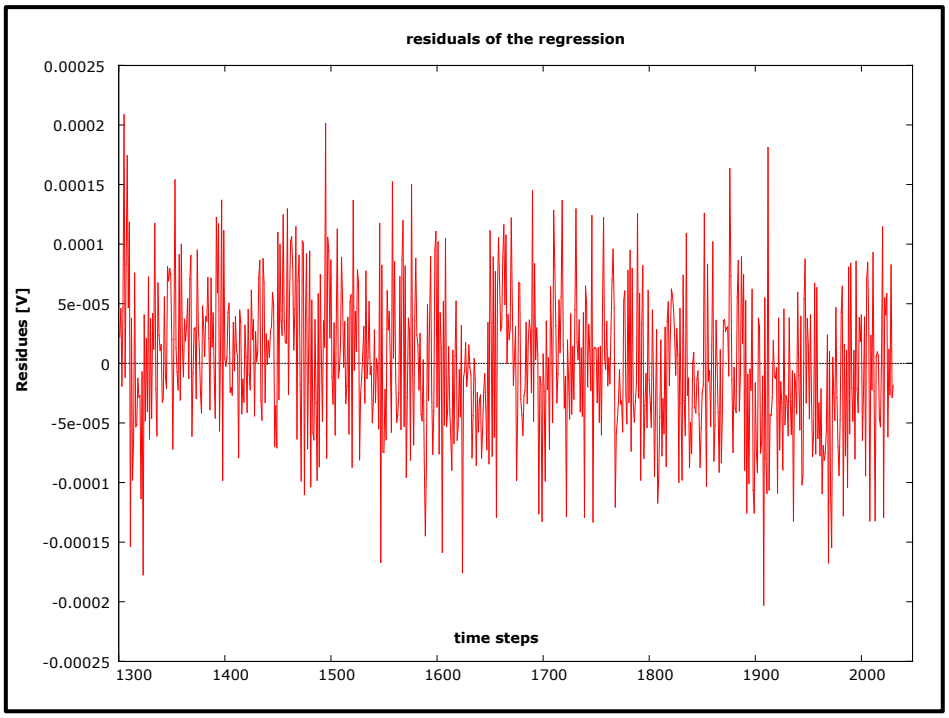



**Figure 4.6.3.5: Graph of the residues given by the difference between the data of the real noise signal and the simulated stochastic process AR(1) for piece 6 of type A device by setting $V_{GS}$ to 5 V and $V_{DS}$ to 50 mV in the time interval between the measuring points 1300 and 2048 obtained through GRETEL software (stationary conditions).**

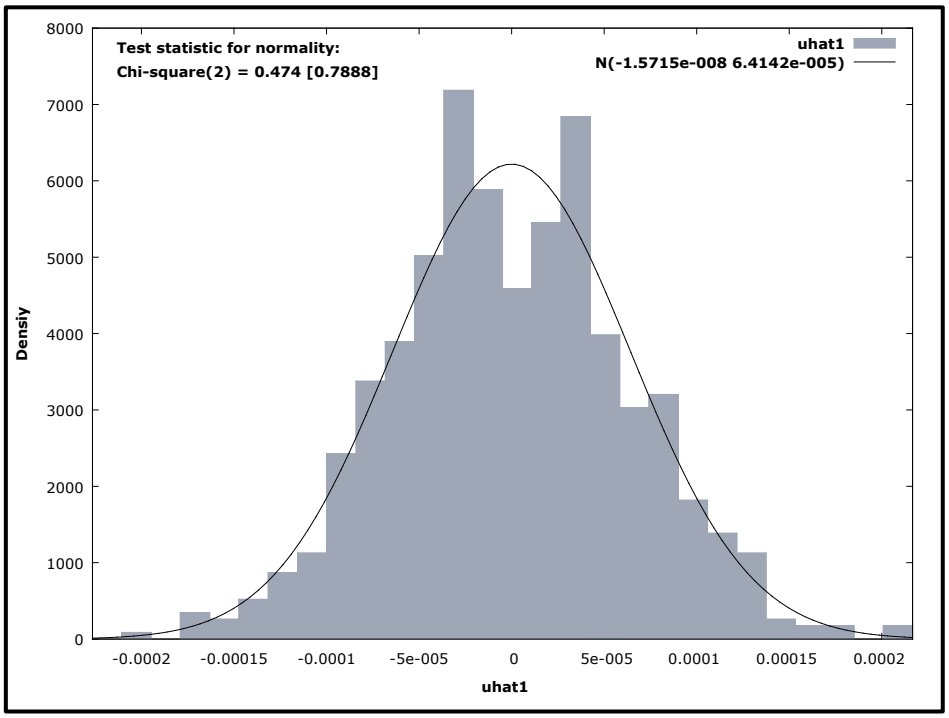



**Figure 4.6.3.6: $\chi^2$ test applied on the residues shown in figure 4.6.3.5 considering a statistical significance level equal to 95% to evaluate if its distribution is normal.**

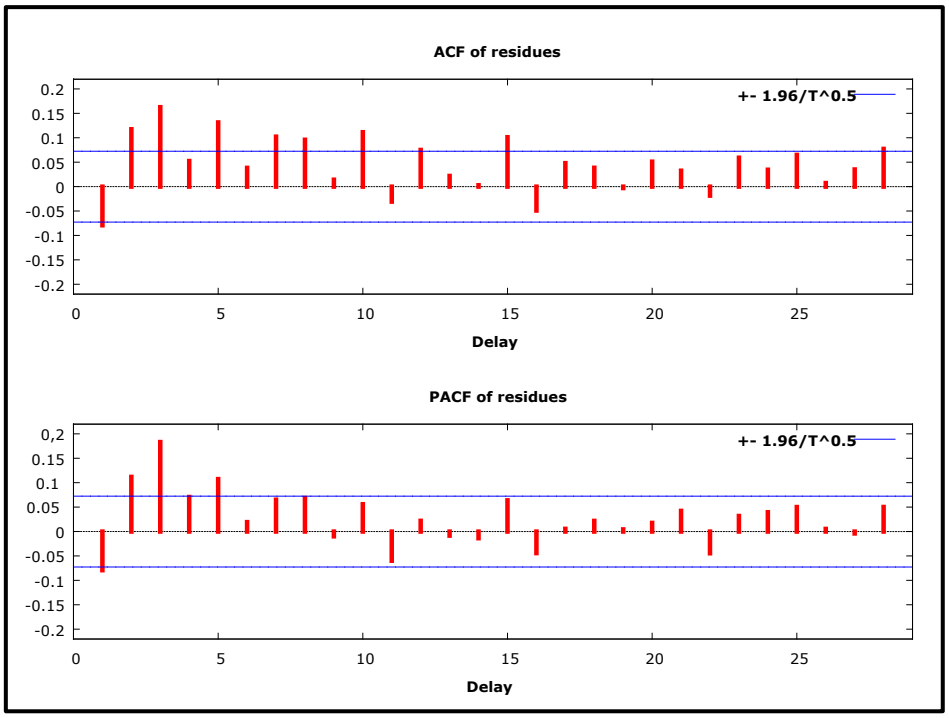



**Figure 4.6.3.7: ACF and PACF functions of the residues shown in figure 4.6.3.5 considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

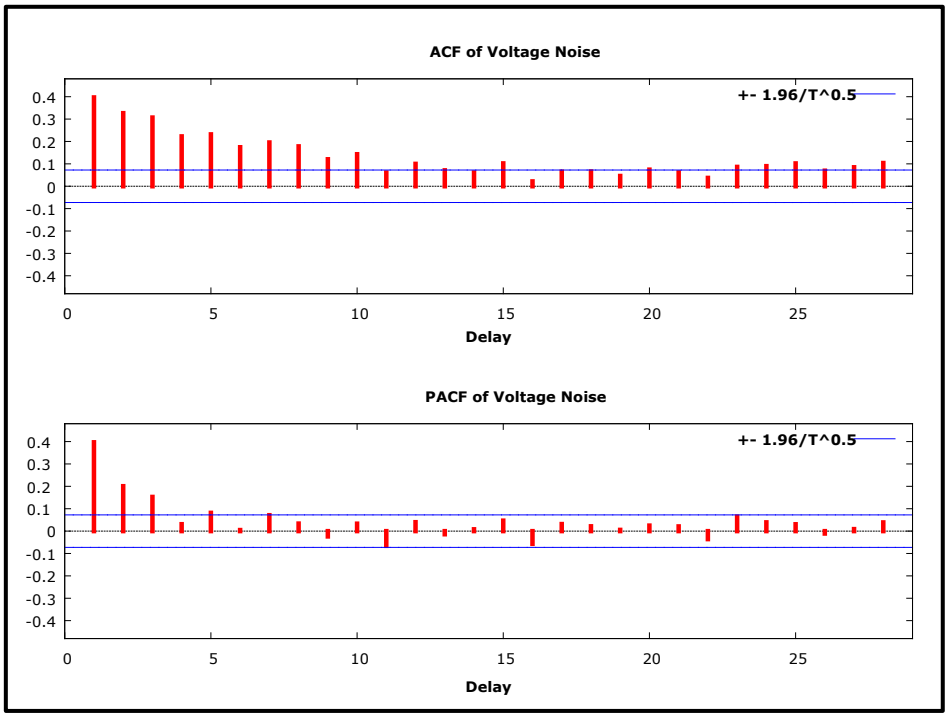



**Figure 4.6.3.8: ACF and PACF functions of the noise signal shown in figure 4.6.3.2.**

However, it is necessary to highlight again that the p-values associated with the linear regression coefficients are very low due to the trend present in the signal due to the slow discharge of the batteries and capacitors and the presence of other factors that will be shown later. The graph of the residues is shown in figure 4.6.3.11 while the graph of their distribution and the graphs of the ACF and PACF functions are shown respectively in figure 4.6.3.12 and figure 4.6.3.13. From figure 4.6.3.12, based on $\chi^2$ test, it is possible to observe that statistically the residues are normally distributed with zero mean and a variance equal to $6.22 \times 10^{-5}$. Instead, this time the ACF and PACF functions do not show any correlation between events observed at different events, thus, this model could be successfully chosen to simulate the noise signal. In any case, to better simulate the noise, we could eliminate the trend observed in the signal shown in figure 4.6.3.14. By subtracting from each observed event the corresponding value from the straight line whose equation is shown in figure 4.6.3.14, it is possible to obtain the noise signal without its trend (see figure 4.6.3.15). In the latter graph the noise signal again shows a slight linear trend but the coefficient of the straight line of correlation is in the order of $10^{-11}$ instead of $10^{-7}$. In fact, a small trend still persists because the discharge of the batteries and capacitances located in the amplifier module cannot be modelled simply by a linear function. The comparison between the real and the simulated data without the trend effect is shown in figure 4.6.3.16. Instead, in the figure 4.6.3.17 and in the figure 4.6.3.18 the table of the estimated parameters of the process AR(3) and the graphs ACF and PACF are shown. From the figure 4.6.3.17 it is possible to observe that the estimated values of the parameters of the modified AR(3) process are quite similar to those obtained in figure 4.6.3.10 and that their associated p-value grows a lot even if they still remain low because the amplitude of the simulated oscillations are too small compared to the real ones as shown in figure 4.6.3.16. In fact, the amplitude of the oscillations is related to the sum of many charge and discharges events that occur simultaneously. Instead, figure 4.6.3.18 still shows a small difference in ACF and PACF autocorrelations due to the presence of other charge and discharge events that occurs and have larger time constants as observed in figure 4.6.3.15 although the values PACF still confirms that an important correlation exists up to events that occur in the time interval within 1ms. However, in order to extend the analysis to all samples of the two families of SiC power MOSFETs, we carry out the following studies. First, we normalized all data by eliminating the linear trend effect as previously done and then adding the minimum value observed in the set of measurements and dividing by the amplitude of the noise signal. Therefore, the transformed noise signal becomes a signal that has an amplitude between 0 and 1 for all measurements performed on the whole series of samples and $V_{GS}$ values. The graphs of the normalized noise signals are shown from figure 4.6.3.19. As can be seen from these figures, in many cases, by varying the $V_{GS}$ from 3.4 V to 5.0 V the signals become more predictable because for higher gate voltages a sinusoidal trend is added. From these figures, it is possible to even describe two different types of behaviour between type A and type B devices. By way of example, considering piece 3 of the type B device, it is possible to observe the 3.8 V, 4.6 V and 5.0 V signals and extrapolate the ACF and PACF graphs as shown in figure 4.6.3.30, figure 4.6.3.31, figure 4.6.3.32 and figure 4.6.3.33. For example, in figure 4.6.3.33 it is possible to observe that the PACF autocorrelations have significant values up to the three subsequent events as observed in piece 6 of the type A device. However, the ACF autocorrelations show significant values for very long times highlighting a rather long persistence phenomenon. Instead, in figure 4.6.3.32, when a $V_{GS}$ of 4.6 V is applied, even if the PACF autocorrelations remain significant up to 3 or 4 successive events, the ACF autocorrelations become significant only for the next 8 events. Finally, in figure 4.6.3.31, when a $V_{GS}$ of 3.8 V is applied, both the ACF and the PACF become rather uncorrelated. These observed phenomena can be explained considering that the higher the $V_{GS}$, the greater the number of traps that respond to the signal even at greater depth in the oxide. Now consider the example of piece 5 of the type A device.

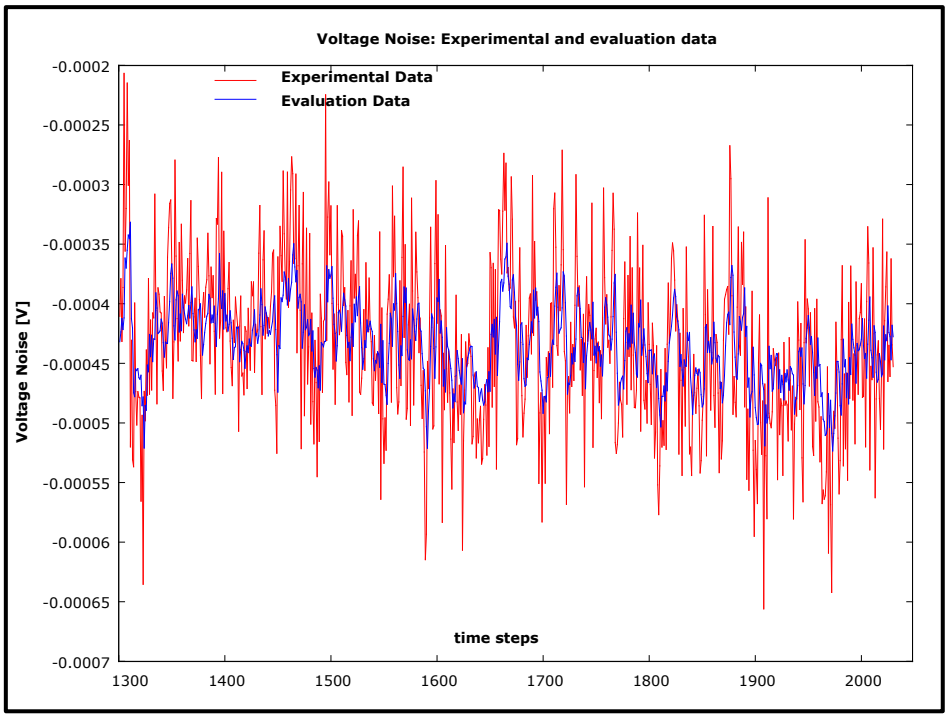



**Figure 4.6.3.9: Comparison between the real noise signal coming from the tested SiC power MOSFET and the AR(3) function obtained by the GRETEL software and optimized with X-13 ARIMA (stationary conditions).**

gretl: model

File Modifica Test Salva Grafici Analisi LaTeX

Model X-13-ARIMA

| | coefficient | errore std. | z | p-value | |
|---|---|---|---|---|---|
| const | -0.000434452 | 5.58814e-06 | -77.75 | 0.0000 | *** |
| phi_1 | 0.285987 | 0.0365743 | 7.819 | 5.31e-015 | *** |
| phi_2 | 0.152154 | 0.0376553 | 4.041 | 5.33e-05 | *** |
| phi_3 | 0.152597 | 0.0366062 | 4.169 | 3.06e-05 | *** |

| | | | |
|---|---|---|---|
| dependent variable mean | -0.000435 | E.S. var. dipendent | 0.000070 |
| Average-likelihood | -5.59e-08 | E.S. innovations | 0.000062 |
| Log-likelihood | 6036.432 | Akaike criterion | -12062.86 |
| Schwarz criterion | -12039.90 | Hannan-Quinn | -12054.00 |

E.S. = errore standard

| | | Real | Immaginary | Modul | Freq |
|---|---|---|---|---|---|
| AR | | | | | |
| Root | 1 | 1.3243 | 0.0000 | 1.3243 | 0.0000 |
| Root | 2 | -1.1607 | 1.8977 | 2.2245 | 0.3374 |
| Root | 3 | -1.1607 | -1.8977 | 2.2245 | -0.3374 |

**Figure 4.6.3.10: Table summarizing the results of the parameters estimated with the AR(3) model via X-13 ARIMA for the noise signal from the tested SiC power MOSFET.**

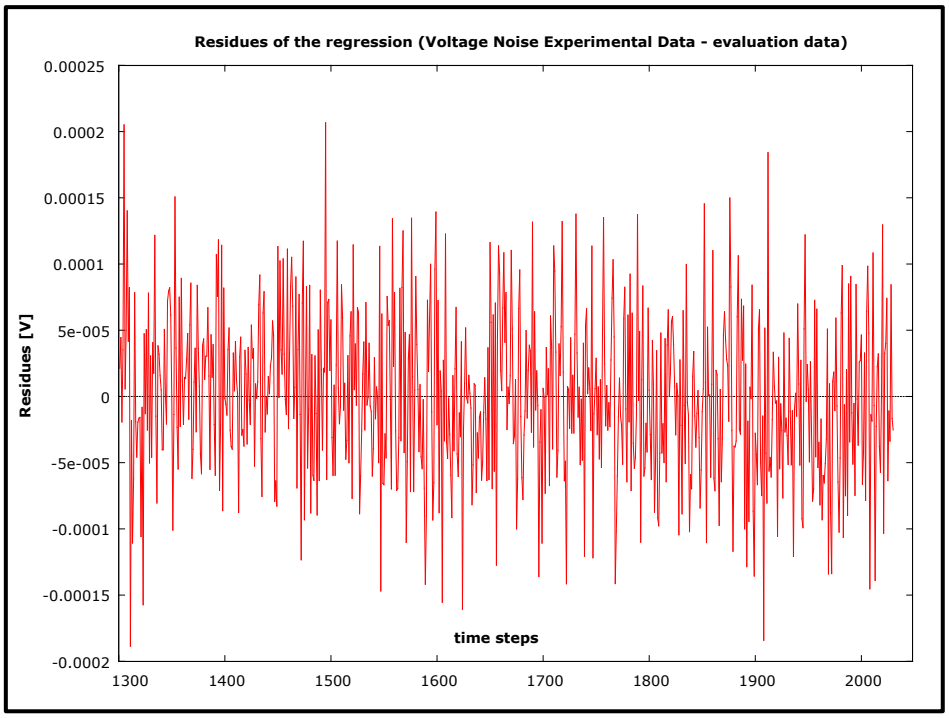



**Figure 4.6.3.11: Graph of the residues given by the difference between the data of the real noise signal and the simulated stochastic process AR(3) for piece 6 of type A device by setting $V_{GS}$ to 5 V and $V_{DS}$ to 50 mV in the time interval between the measuring points 1300 and 2048 obtained through GRETEL software (stationary conditions).**

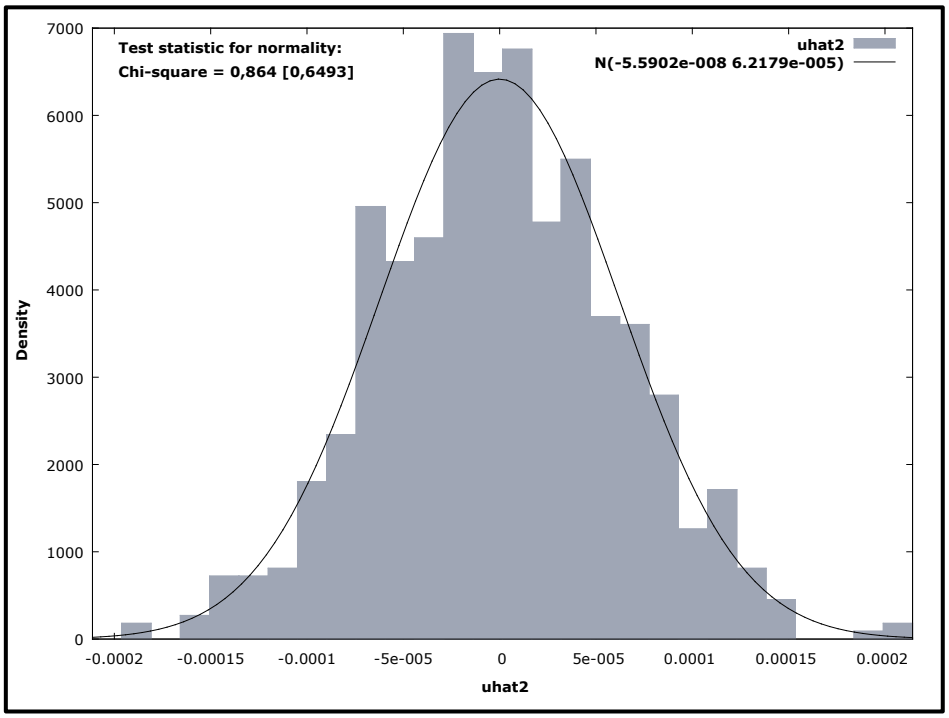



**Figure 4.6.3.12: $\chi^2$ test applied on the residues shown in figure 4.6.3.10 considering a statistical significance level equal to 95% to evaluate if its distribution is normal.**

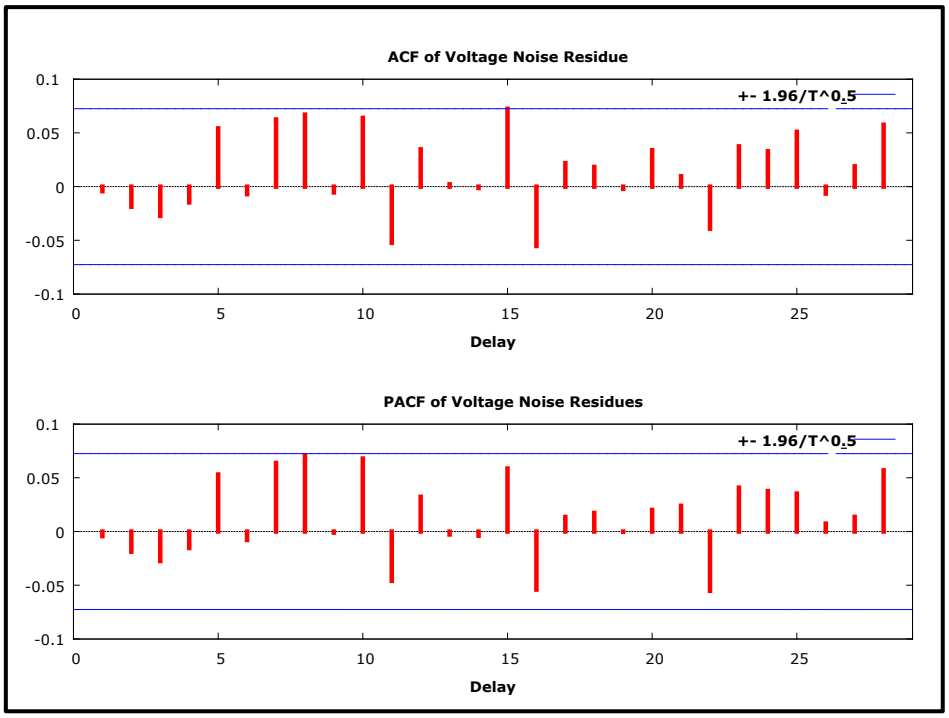



**Figure 4.6.3.13: ACF and PACF functions of the residues shown in figure 4.6.3.11 considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

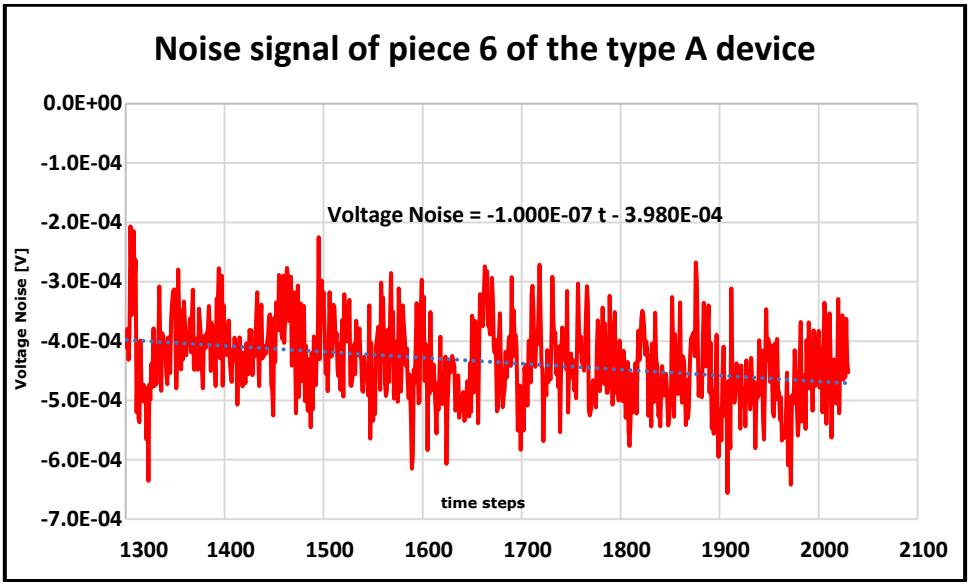



**Figure 4.6.3.14: Noise signal averaged in 80 window function frames in the time domain for piece 6 of type A device by setting the $V_{GS}$ to 5 V and the $V_{DS}$ to 50 mV in the time interval between the measuring points 1300 and 2048 showing the linear trend (stationary conditions).**

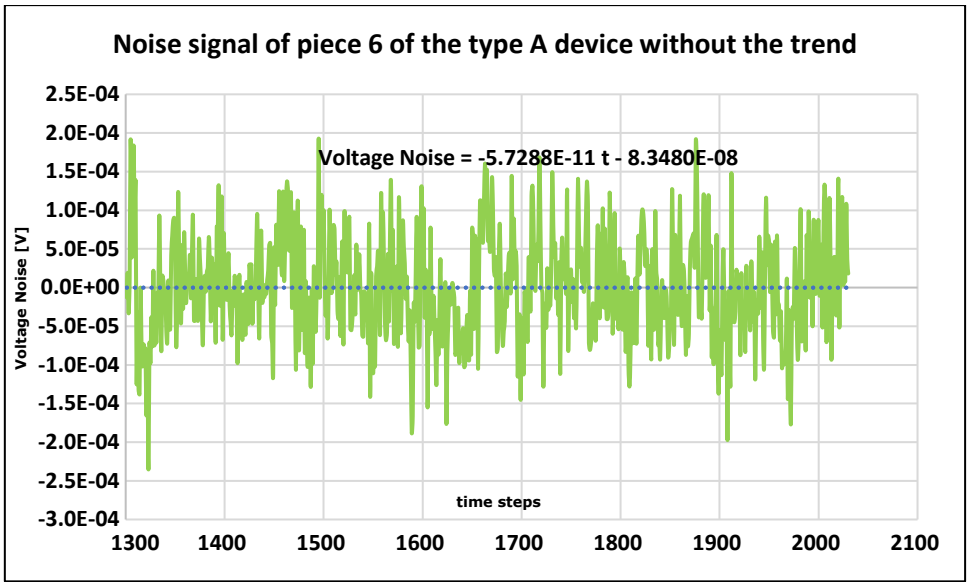



**Figure 4.6.3.15: Noise signal averaged in 80 window function frames in the time domain for piece 6 of type A device by setting the $V_{GS}$ to 5 V and the $V_{DS}$ to 50 mV in the time interval between the measuring points 1300 and 2048 without the linear trend (stationary conditions).**

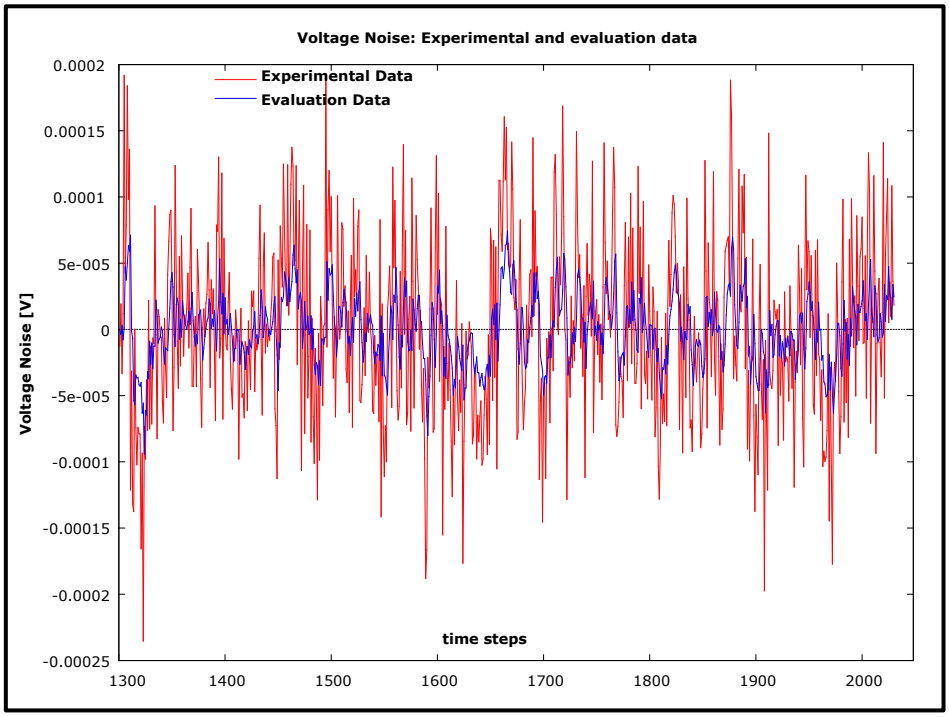



**Figure 4.6.3.16: Comparison between the real noise signal from the tested SiC power MOSFET and the AR(3) function obtained by eliminating the trend effect carried out using the GRETEL software and optimized with X-13 ARIMA (stationary conditions).**

gretl: modello 2

File Modifica Test Salva Grafici Analisi LaTeX

Model X-13-ARIMA

| | coefficient | errore std. | z | p-value | |
|---|---|---|---|---|---|
| const | -2.94251e-08 | 4.66763e-06 | -0.006304 | 0.9950 | |
| phi_1 | 0.259822 | 0.0367114 | 7.077 | 1.47e-012 | *** |
| phi_2 | 0.129287 | 0.0376492 | 3.434 | 0.0006 | *** |
| phi_3 | 0.125838 | 0.0367782 | 3.422 | 0.0006 | *** |

| | | | |
|---|---|---|---|
| dependent variable mean | -1.04e-07 | E.S. var. dipendent | 0.000067 |
| Average-likelihood | 1.03e-08 | E.S. innovations | 0.000061 |
| Log-likelihood | 6044.559 | Akaike criterion | -12079.12 |
| Schwarz criterion | -12056.15 | Hannan-Quinn | -12070.26 |

E.S. = errore standard

| | Real | Immaginary | Modul | Freq |
|---|---|---|---|---|
| AR | | | | |
| Root | 1.4272 | 0.0000 | 1.4272 | 0.0000 |
| Root | -1.2273 | 2.0154 | 2.3597 | 0.3371 |
| Root | -1.2273 | -2.0154 | 2.3597 | -0.3371 |

**Figure 4.6.3.17: Table summarizing the results of the parameters estimated with the AR(3) model via X-13 ARIMA obtained by eliminating the trend effect for the noise signal from the tested SiC power MOSFET.**

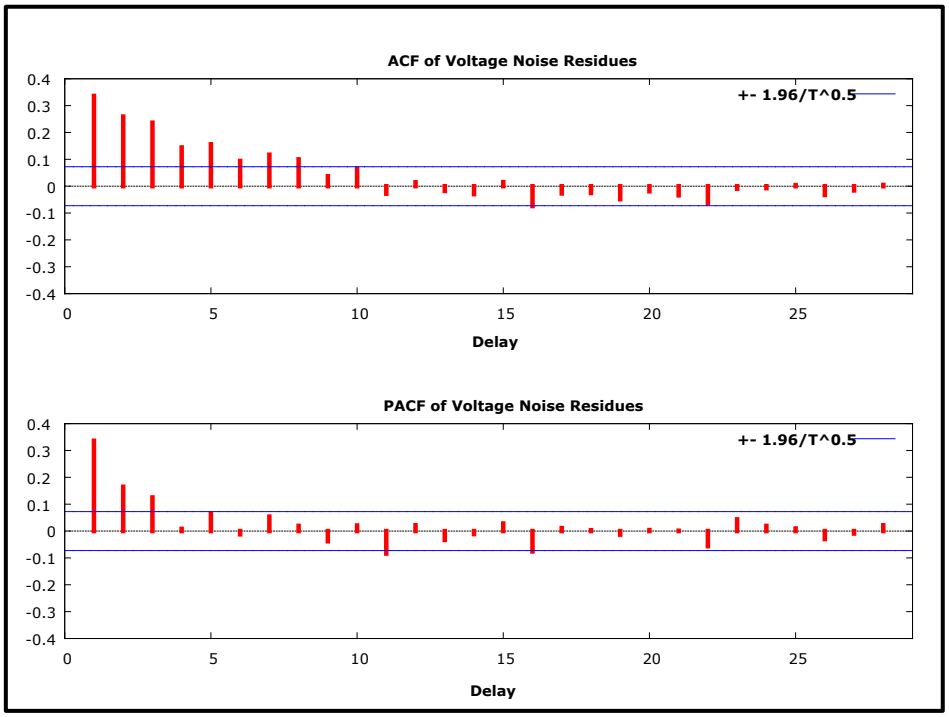



**Figure 4.6.3.18: ACF and PACF functions of the residues obtained by eliminating the trend effect in the noise signal shown in figure 4.6.3.16 considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

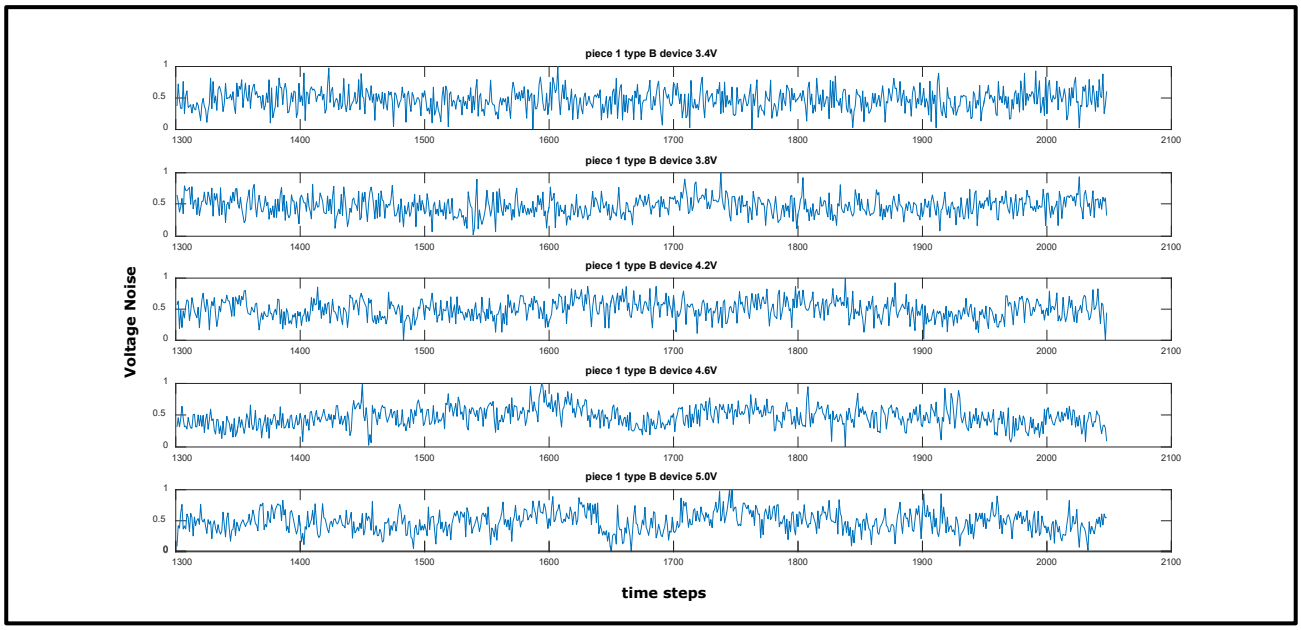



**Figure 4.6.3.19: Normalized noise signals for piece 1 of the type B device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

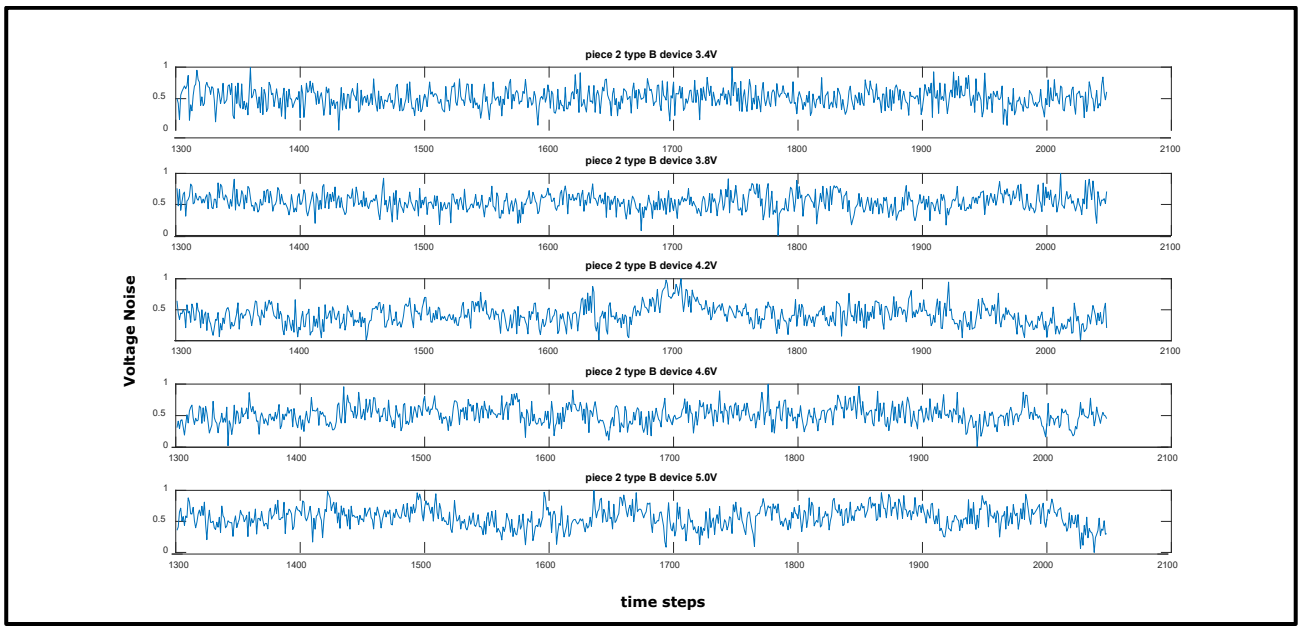



**Figure 4.6.3.20: Normalized noise signals for piece 2 of the type B device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

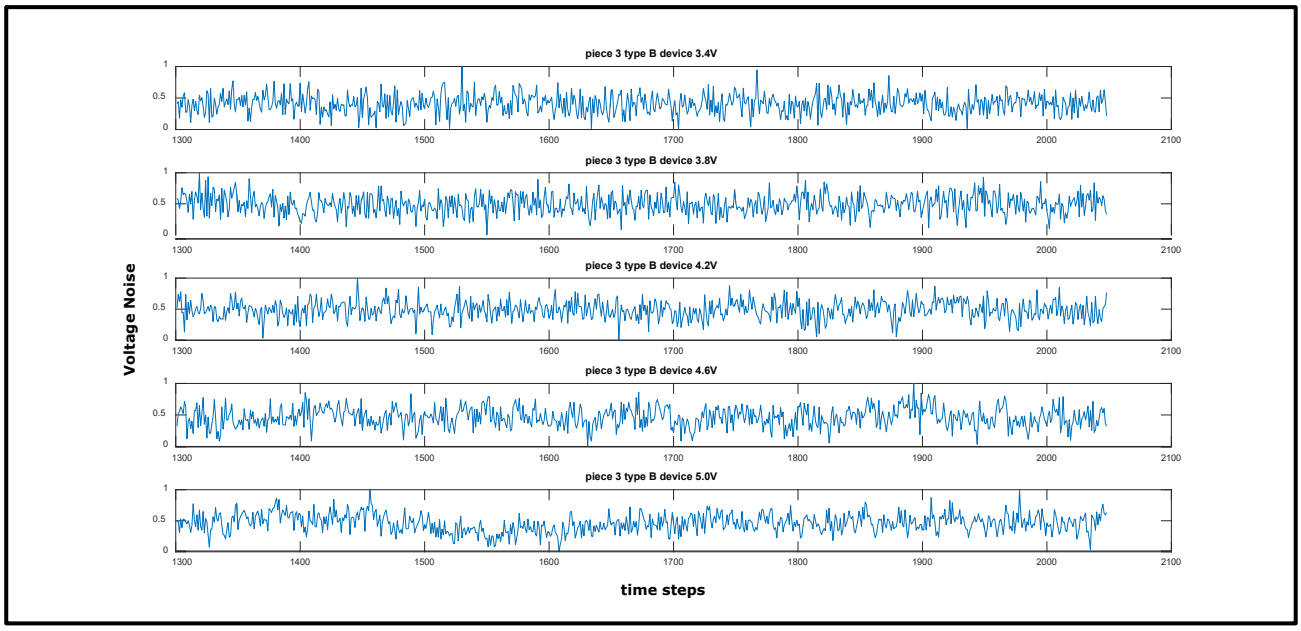



**Figure 4.6.3.21: Normalized noise signals for piece 3 of the type B device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

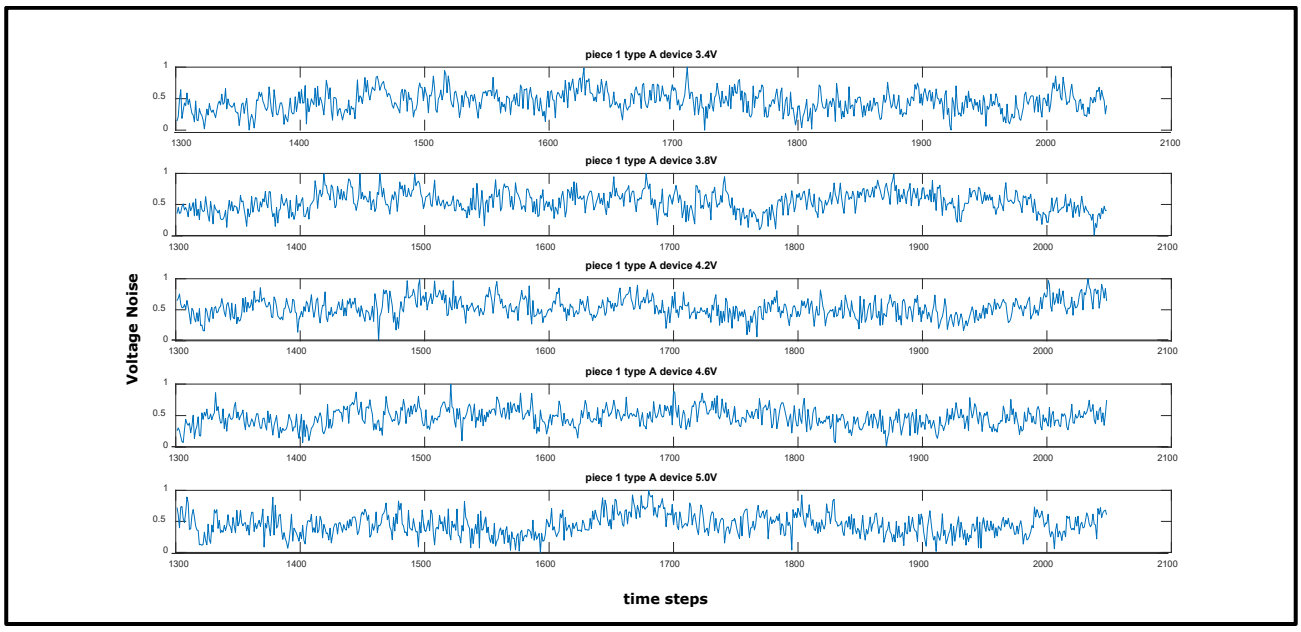



**Figure 4.6.3.22: Normalized noise signals for piece 1 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

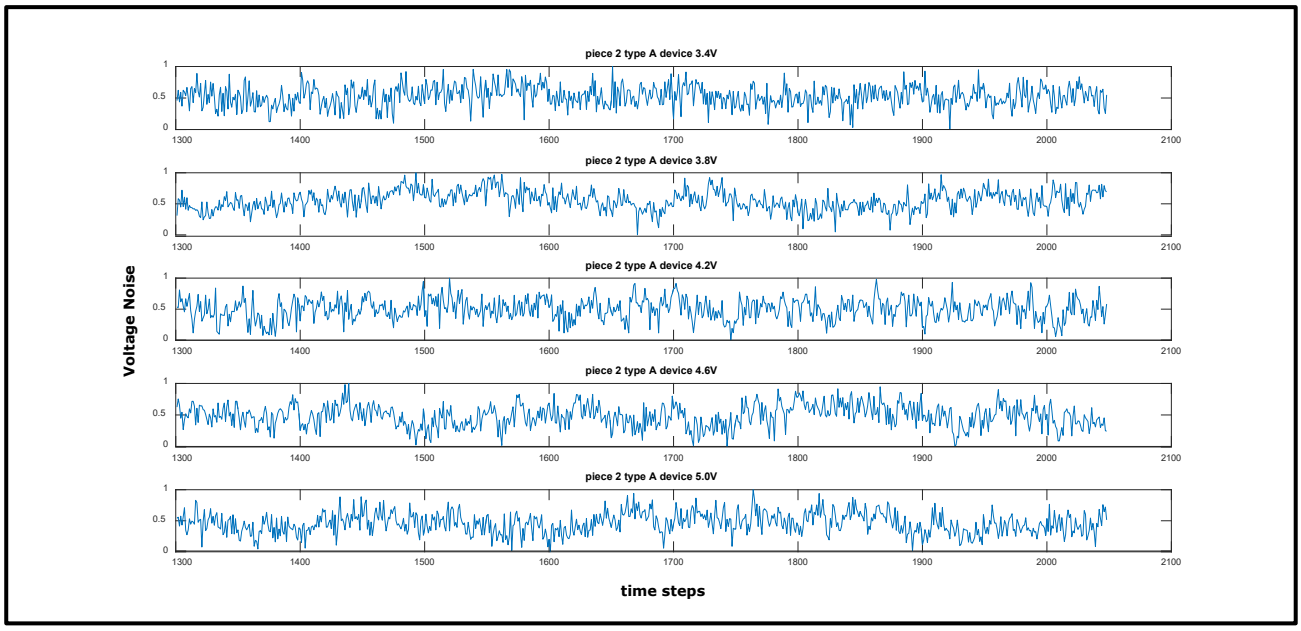



**Figure 4.6.3.23: Normalized noise signals for piece 2 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

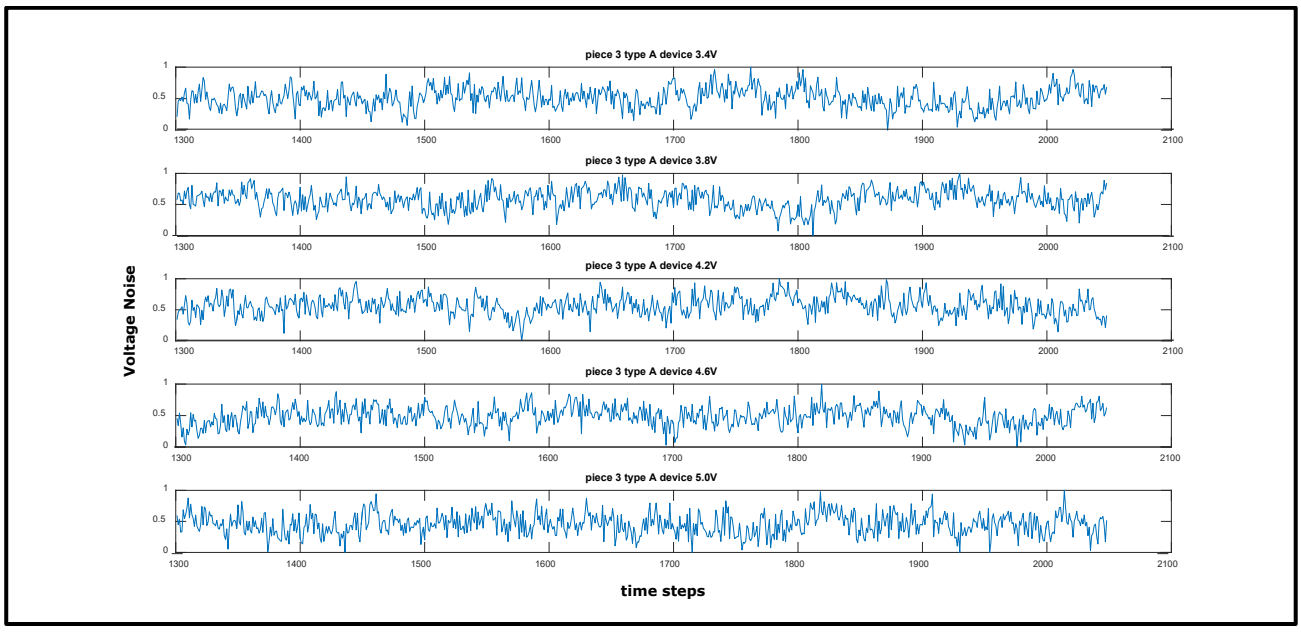



**Figure 4.6.3.24: Normalized noise signals for piece 3 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

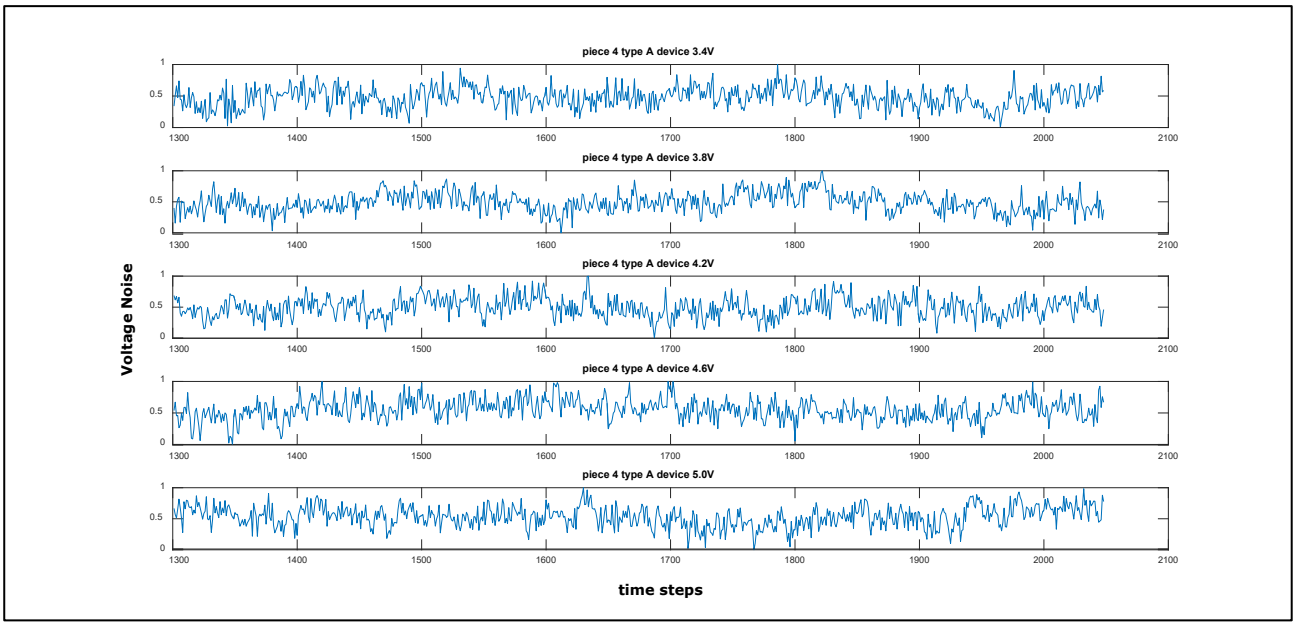



**Figure 4.6.3.25: Normalized noise signals for piece 4 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

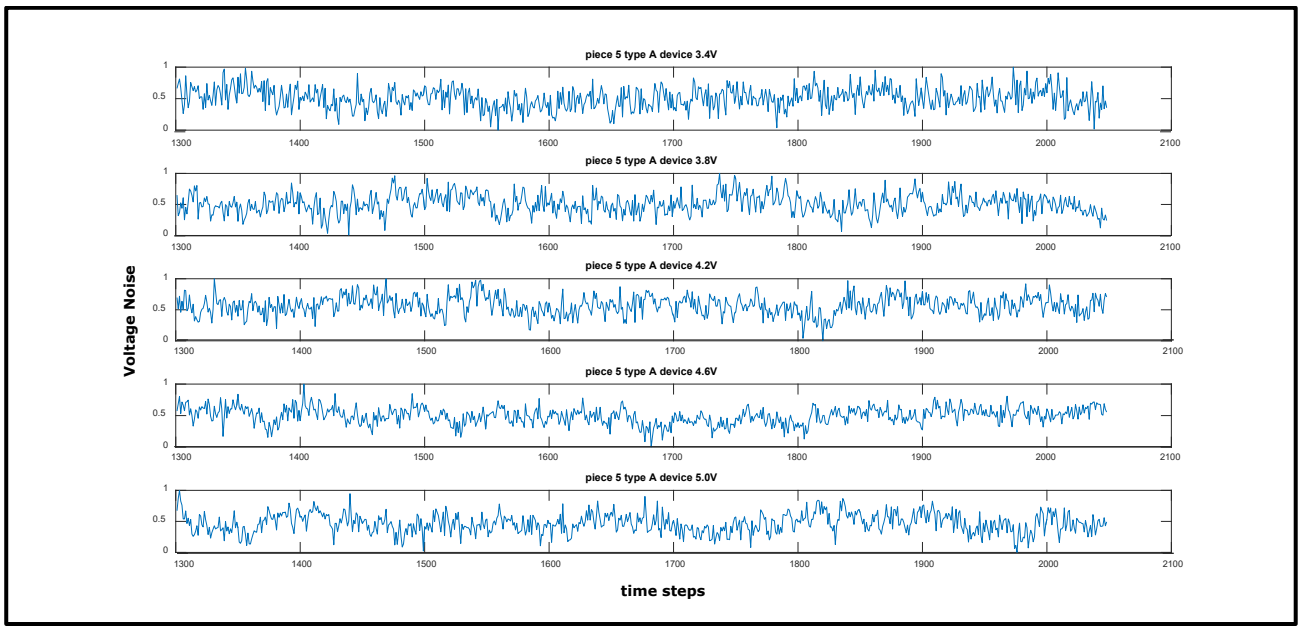



**Figure 4.6.3.26: Normalized noise signals for piece 5 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

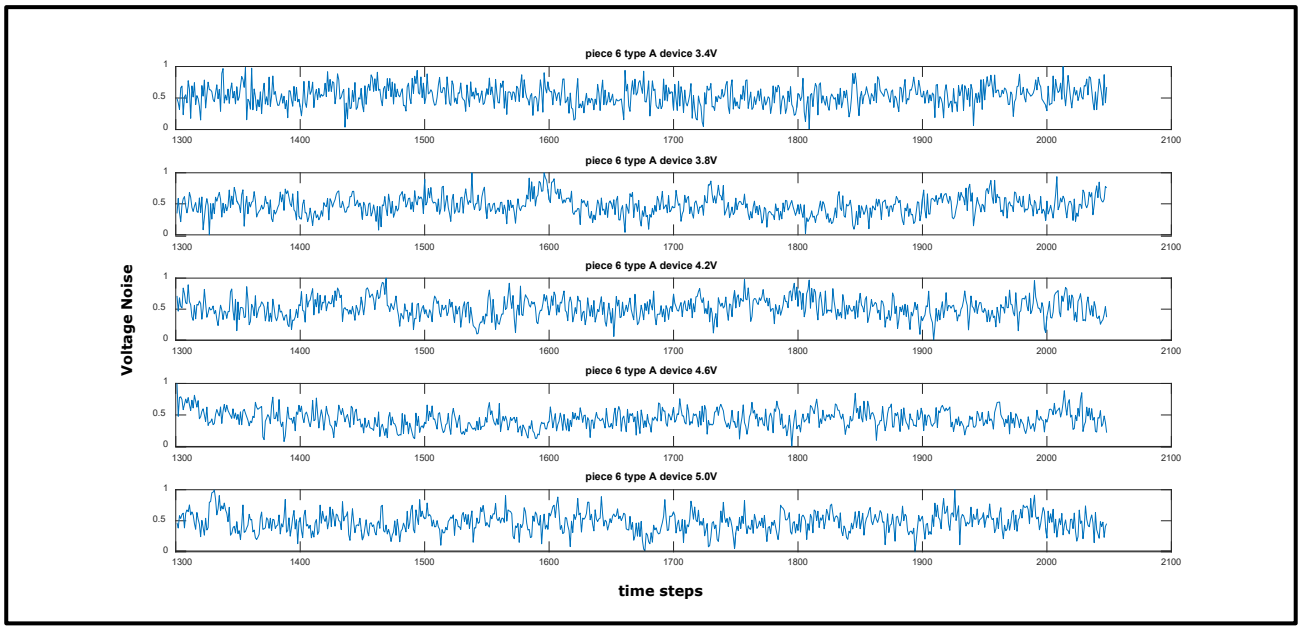



**Figure 4.6.3.27: Normalized noise signals for piece 6 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

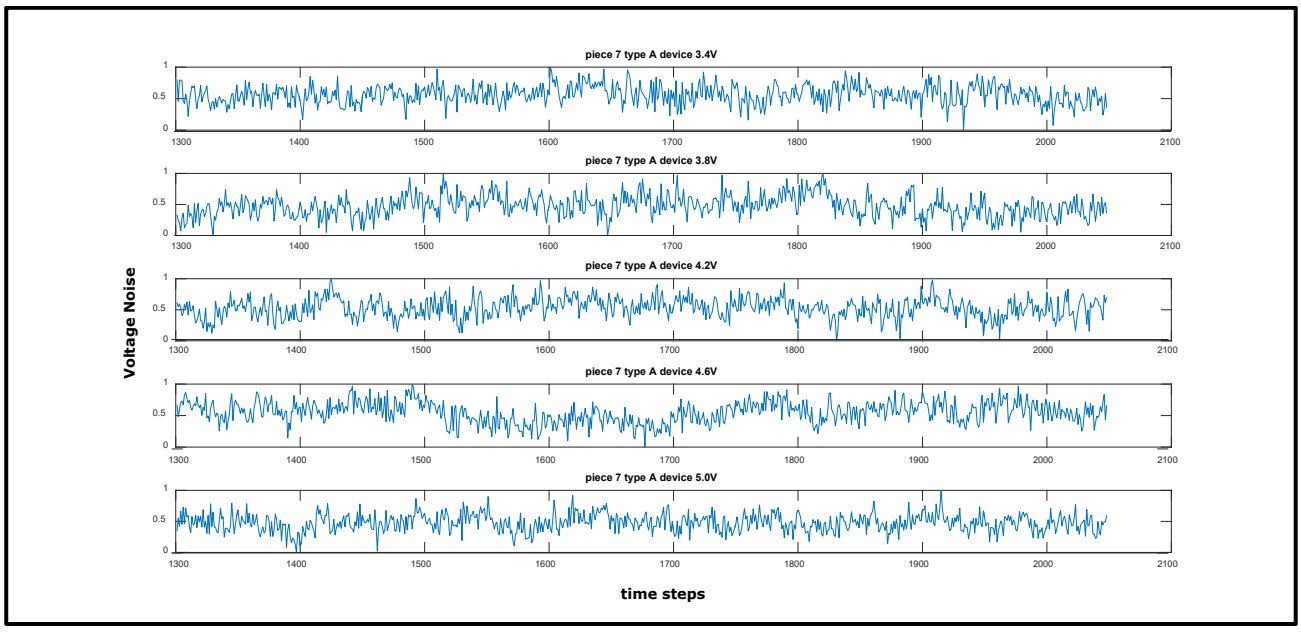



**Figure 4.6.3.28: Normalized noise signals for piece 7 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

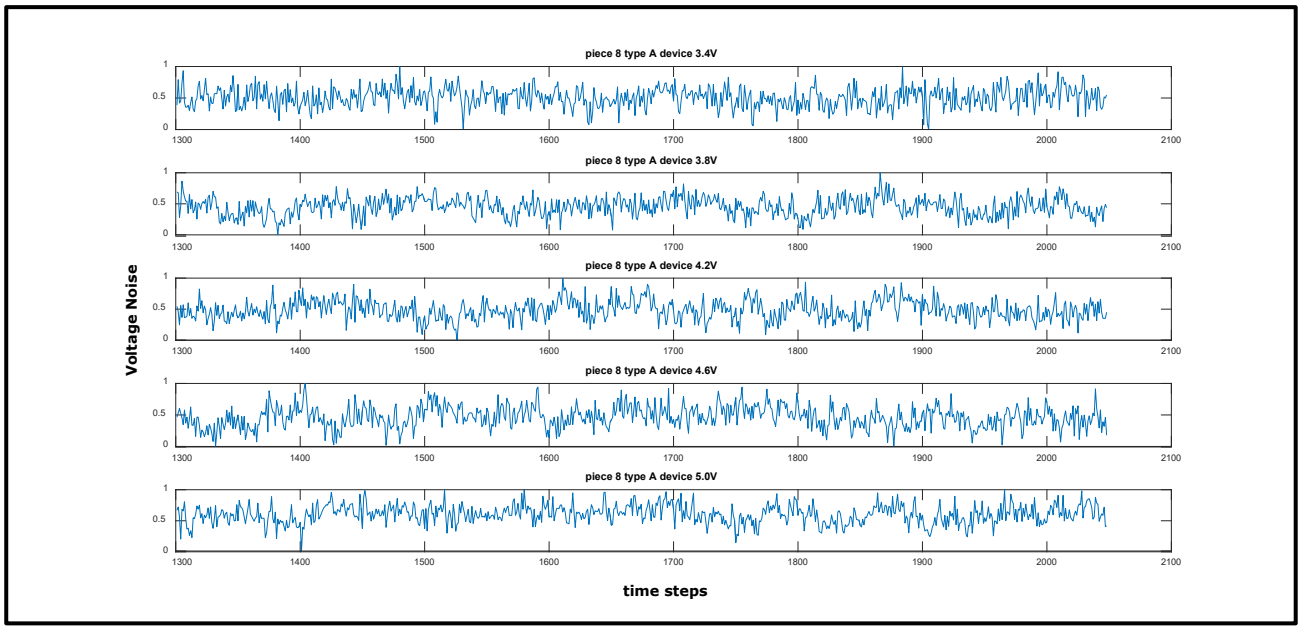



**Figure 4.6.3.29: Normalized noise signals for piece 8 of the type A device for $V_{GS}$ which varies from 3.4 V to 5.0 V.**

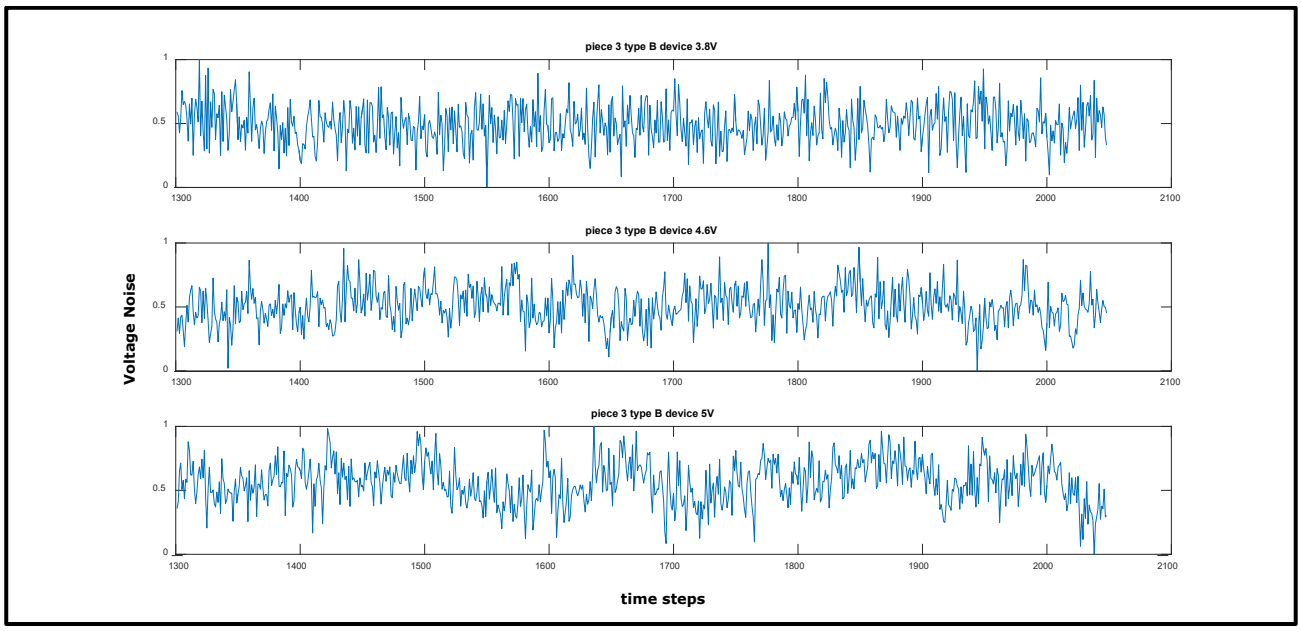



**Figure 4.6.3.30: Normalized noise signals for piece 3 of the type B device for $V_{GS}$ equal to 3.8 V, 4.6 V and 5.0 V.**

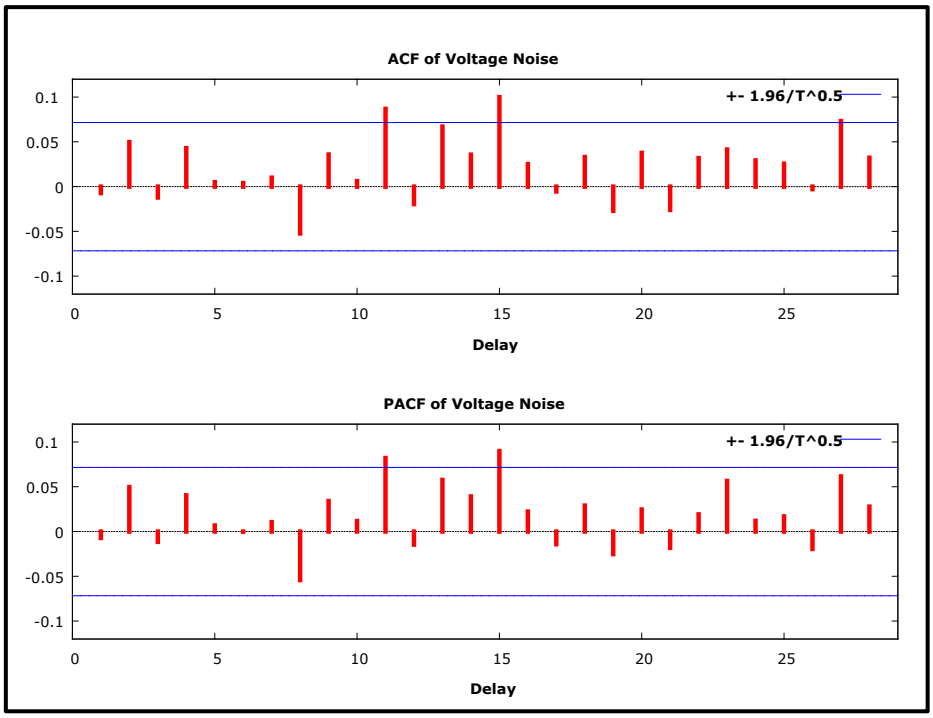



**Figure 4.6.3.31: ACF and PACF functions of the noise signal shown in figure 4.6.3.30 of piece 3 of the type B device with $V_{GS}$ equal to 3.8 V considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

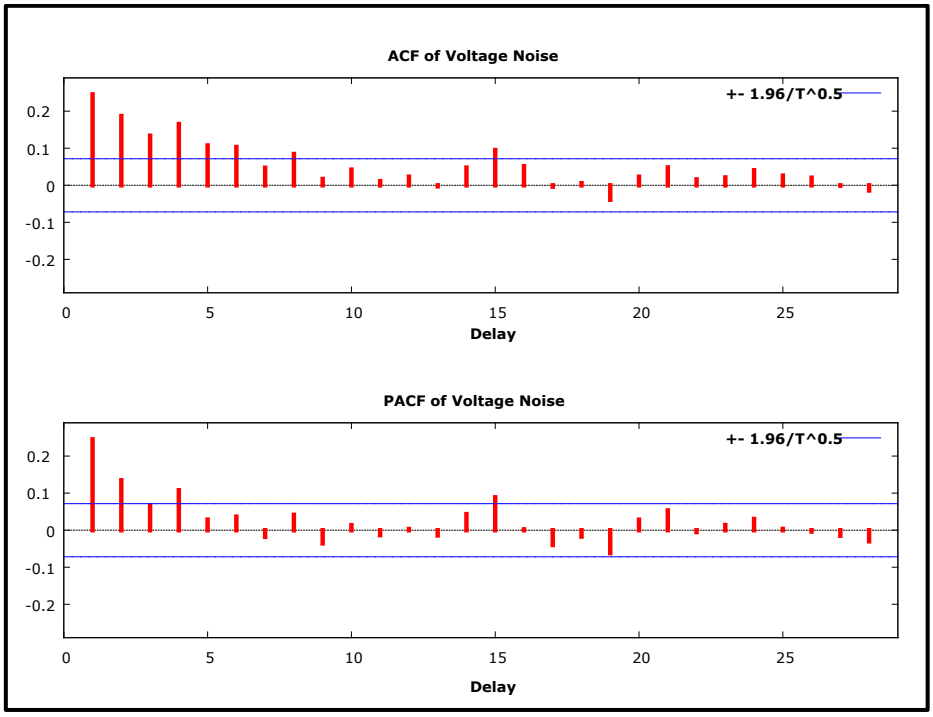



**Figure 4.6.3.32: ACF and PACF functions of the noise signal shown in figure 4.6.3.30 of piece 3 of the type B device with $V_{GS}$ equal to 4.6 V considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

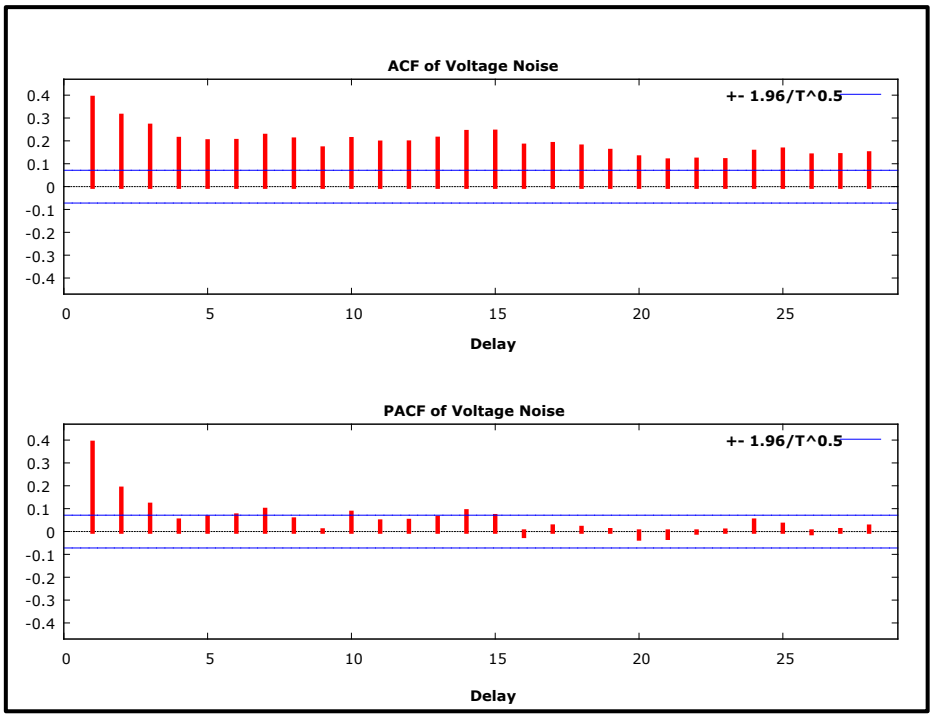



**Figure 4.6.3.33: ACF and PACF functions of the noise signal shown in figure 4.6.3.30 of piece 3 of the type B device with $V_{GS}$ equal to 5.0 V considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

In figure 4.6.3.34, figure 4.6.3.35, figure 4.6.3.36 and figure 4.6.3.37, it is possible to observe the 3.4 V, 4.2 V and 5.0 V signals and extrapolate the ACF and PACF for this last device. As can be seen in these last graphs, a main sine wave of about 15 ms of period overlaps in the noise signals and this means that there is a strong contribution of slower traps in the stochastic process. In the latter case, even at 3.4 V a small autocorrelation remains until a few subsequently events in contrast to what was observed in piece 3 of the type B device. For further analysis, it is possible to obtain a set of random numbers of values between 0 and 1 with MATLAB to compare the ACF and PACF autocorrelations with the previous data obtained from the noise signals as shown in figure 4.6.3.38 and figure 4.6.3.39. It is possible to observe from figure 4.6.3.39 that there is no correlation between the events in contrast with what has been seen for the analysed noise signals.

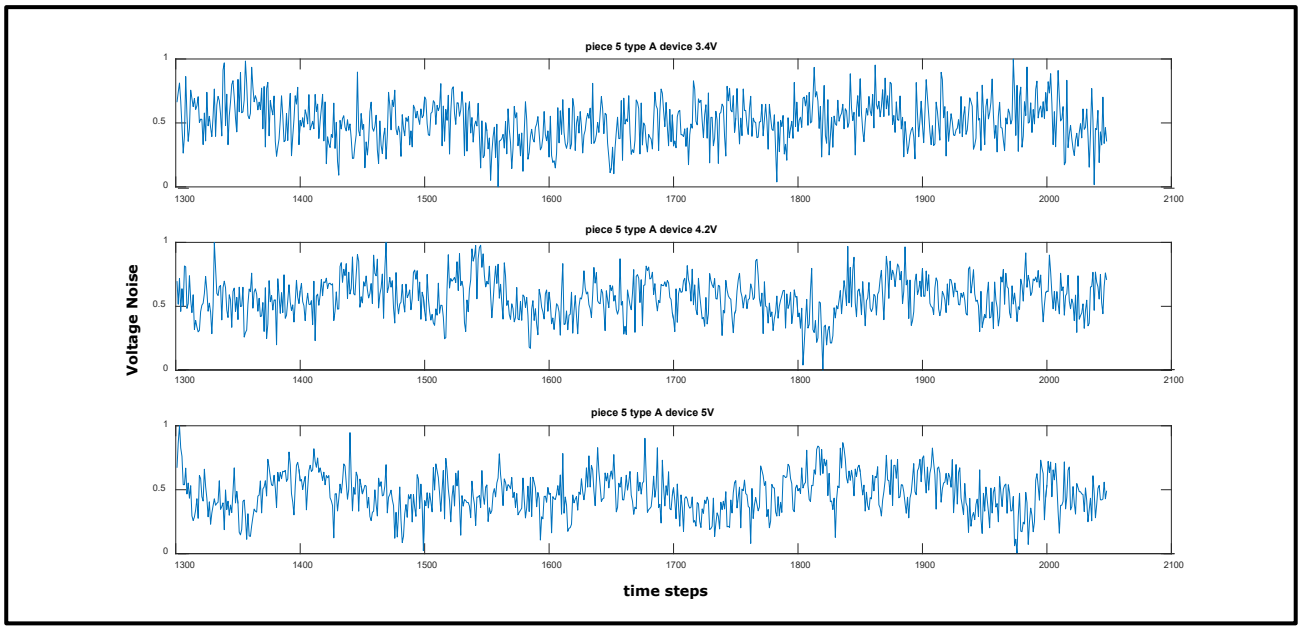



**Figure 4.6.3.34: Normalized noise signals for piece 5 of the type A device for $V_{GS}$ equal to 3.4 V, 4.2 V and 5.0 V.**

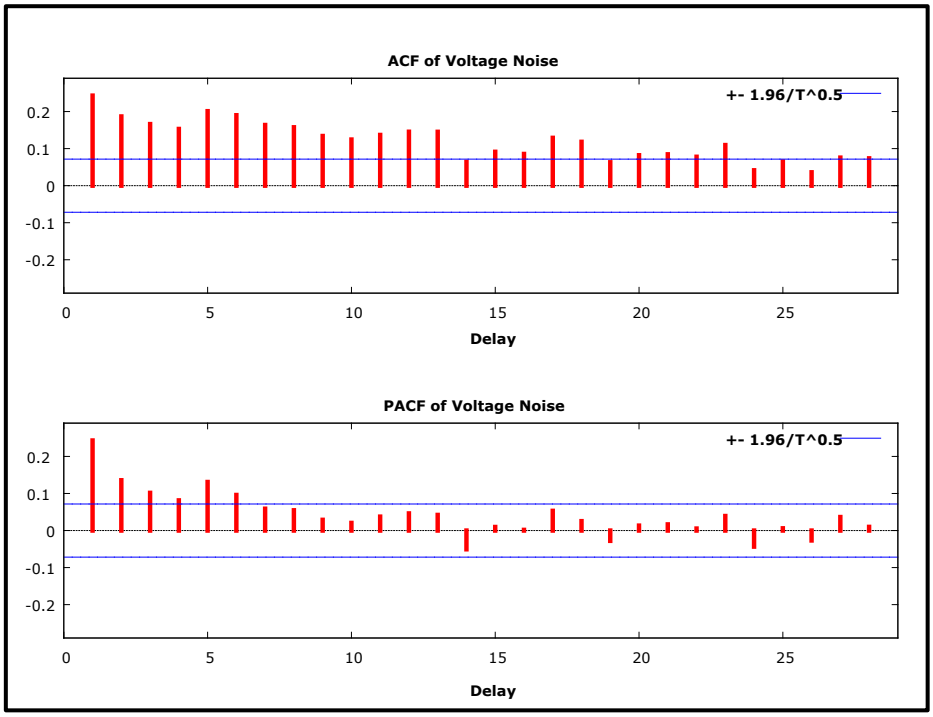



**Figure 4.6.3.35: ACF and PACF functions of the noise signal shown in figure 4.6.3.34 of piece 5 of the type A device with $V_{GS}$ equal to 3.4 V considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

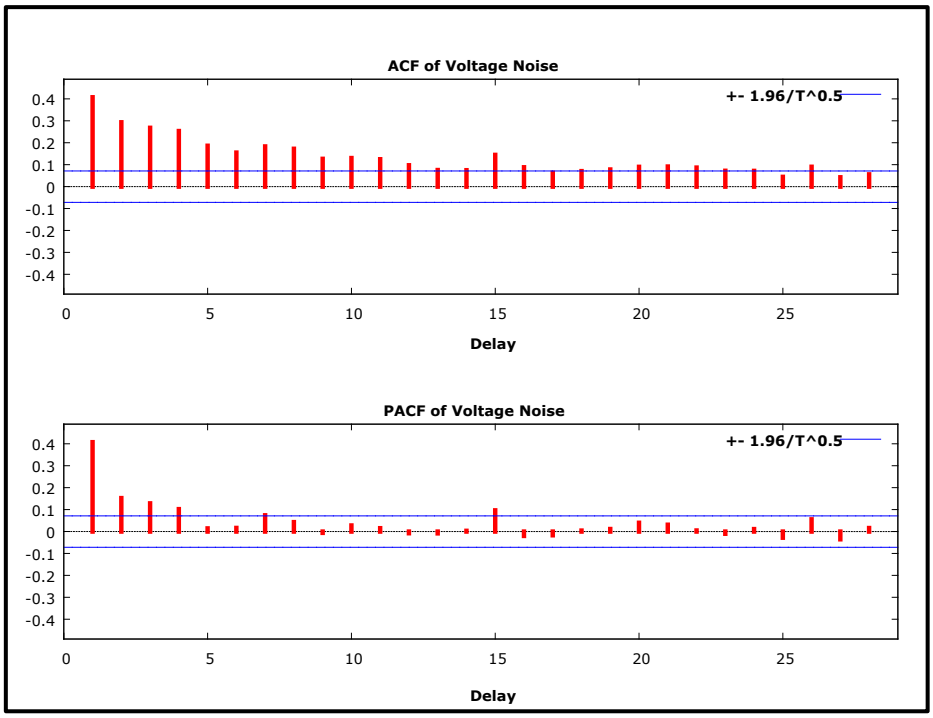



**Figure 4.6.3.36: ACF and PACF functions of the noise signal shown in figure 4.6.3.34 of piece 5 of the type A device with $V_{GS}$ equal to 4.2 V considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

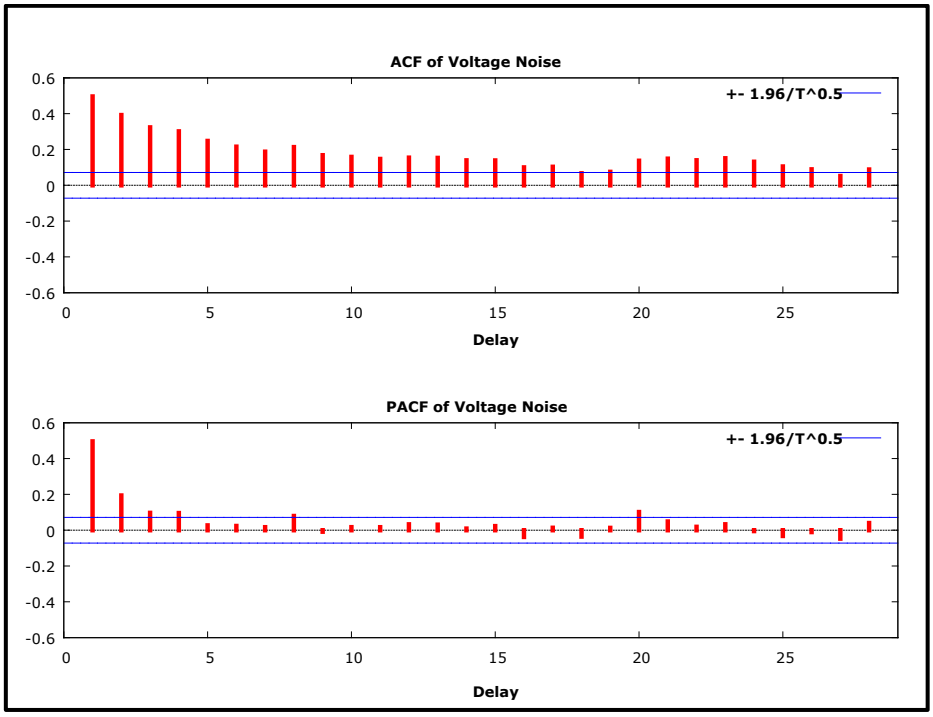



**Figure 4.6.3.37: ACF and PACF functions of the noise signal shown in figure 4.6.4.34 of piece 5 of the type A device with $V_{GS}$ equal to 5.0 V considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

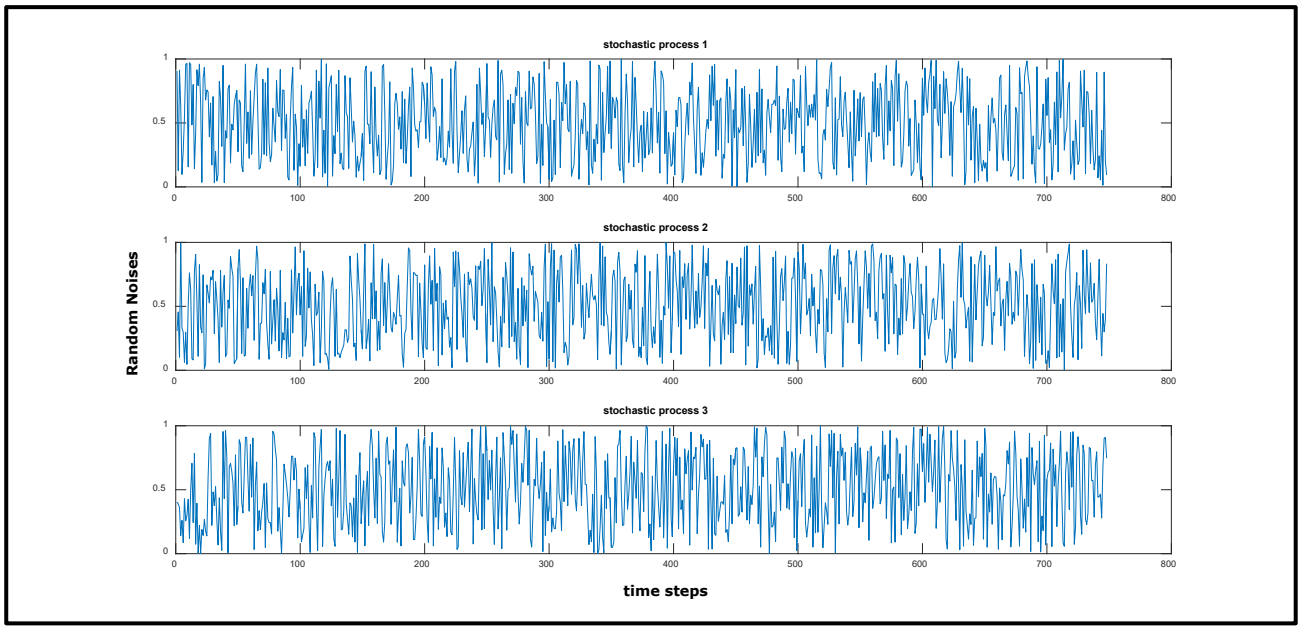



**Figure 4.6.3.38: Three random signals obtained by MATLAB having the same duration as the analysed noise signals.**

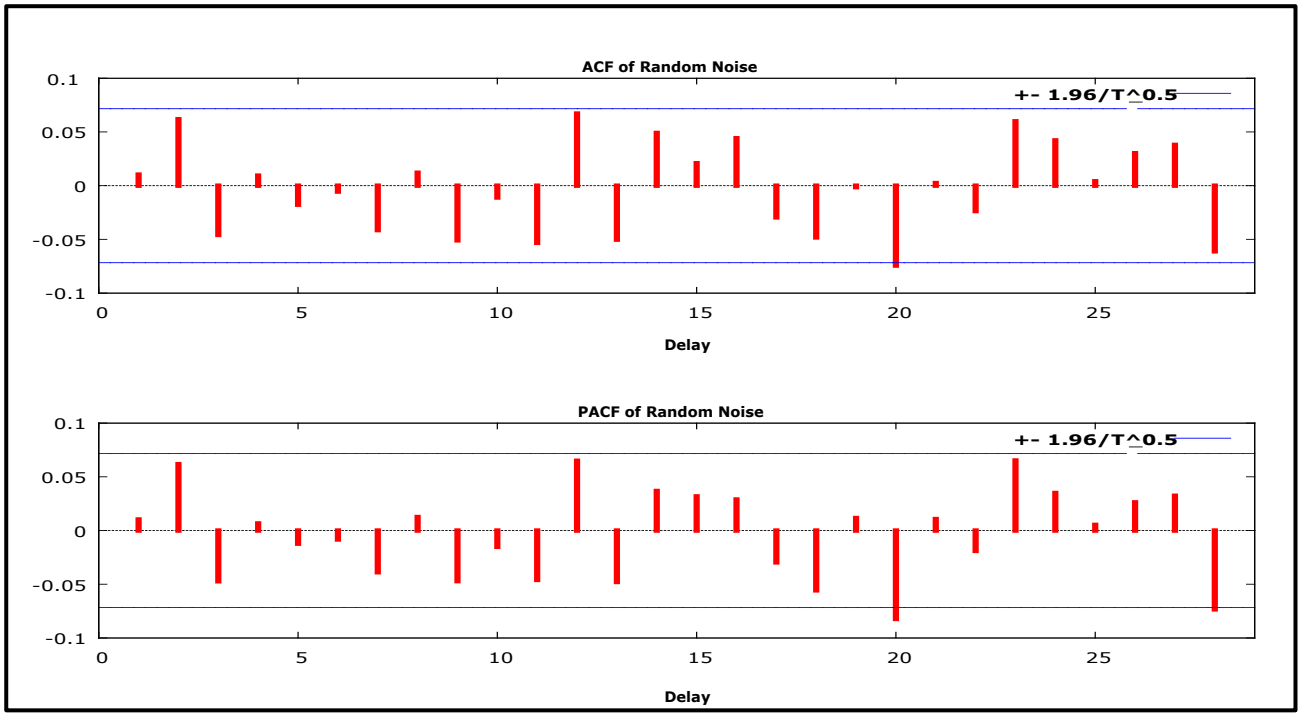



**Figure 4.6.3.39: ACF and PACF functions of random signal 1 considering a statistical significance level equal to 95% to evaluate any correlation between events that occurs at different times.**

# 5 Conclusions

This PhD thesis focused on the study and characterization of the defectiveness observed in the interface between the substrate and the oxide of modern SiC power MOSFETs. In particular, all analyses carried out in this work have been implemented on two different families of devices having the same planar technology, different die size and having a breakdown voltage equal to 1200 V. After a brief introduction in chapter 1, where the role of power MOSFETs in the power applications scenario and the importance of introducing new WBG materials such as SiC to improve the device performances was discussed, this PhD thesis was divided in two parts. The first part, chapter 2 and chapter 3, describes in detail the known art of power MOSFETs while the second part of the PhD thesis, chapter 4, explains what type of experimental tests have been performed to characterize the defectiveness observed in the interface region of the tested SiC power MOSFETs and what type of information can be deducted from the results. The analyses that were performed on the devices under test to characterize the defectiveness of the interface region and, thus, their reliability level were the threshold-voltage instability measurements, the PBTI and the low frequency noise analysis. Furthermore, based on the PBTI and the threshold-voltage instability measurements, the behaviour of these devices were simulated with suitable TCAD tool in order to extrapolate the $D_{it}$ profile as a function of the energy within the SiC bandgap. To complete the characterisation study, further experimental analyses on the physical nature of the interface performed on comparable devices families were extrapolated from the works of P. Fiorenza et al. These analyses concerns both the characterization of the transition layer in the interface region implemented with the EELS (Electron Energy Loss Spectroscopy) technique and the characterization of the gate current to understand the conduction mechanism within the dielectric. These analyses were carried out in the framework of European project WInSiC4AP (Wide Band Gap Innovative SiC for Advanced Power) as well as the work of this PhD thesis. The threshold-voltage instability phenomenon is mainly due to the interface traps even if it also depends on the oxide traps which are close enough to the interface so that they can exchange charges with the inversion layer present in the device channel. In fact, the short-term effects of the threshold voltage instability can be mainly due to interface traps while the long-term effects, mainly due to oxide traps, can be better monitored by PBTI tests. Instead, the low frequency noise analysis is a suitable characterisation tool that allow us to understand if the interface traps and, in particular, the border traps affect the noise observed in the currents and voltages of power MOSFETs.

The hysteresis measurements were obtained considering three different conditions by sweeping the $V_{GS}$ from -5 V up to the maximum voltages of 5 V, 10 V and 15 V. Applying a positive voltage to the gate will result in a positive shift in $V_{th}$. Conversely, applying a negative voltage to the gate will result in a negative shift in $V_{th}$. These effects can be explained by filling or emptying the near-interface oxide traps with electrons in response to the electric field. The current value used to estimate the $V_{th}$ has been set to 100 μA. The shift of the $V_{th}$ is obtained as the difference between the values of the $V_{th}$ estimated during the descending phase, $V_{th}^{down}$, and the ascending phase of the trans-characteristic, $V_{th}^{up}$. From the experimental results it has been found that the $V_{th}$ instability increases by increasing the gate voltage because the higher the gate voltage, the more effectively the tunneling process occurs inside the oxide. Furthermore, the higher the gate voltage, the greater the number of interface traps swept within the SiC bandgap. It is important to point out that the threshold-voltage instability increases slightly for a faster variation of the $V_{GS}$ because the $V_{th}^{down}$ remains stable while the $V_{th}^{up}$ decreases.

It is also important to underline that the hysteresis of $V_{th}$ due to interface traps during the threshold-voltage instability measurements is typically fully reversible. The threshold-voltage instability analysis performed in quasi-static conditions was also implemented in pulsed conditions using the ultra-fast I–V module of the pulse-measure-unit (PMU). Pulsed $I_{DS}$-$V_{GS}$ curves were obtained by applying a train of pulses with a period of 300 µs and a width of 30 µs at the gate terminal. It has been observed that in the pulsed regime the $V_{th}$ shift is lower than the quasi-static condition because the interface traps immediately respond to a fast transient in the $V_{GS}$ while that part of the border traps involved in the quasi-static regime do not respond to the signal.

Another phenomenon that has been studied in these experiments has been how $V_{th}$ changes as the temperature changes. In fact, due to the greater energy bandgap in SiC compared to silicon devices, the intrinsic concentration of carriers that can be thermally activated should be very low and, thus, $V_{th}$ should changes slightly with the temperature. Instead, unlike what is theoretically hypothesized, the $V_{th}$ shift with temperature is approximately the same as observed in silicon devices. This experimental result can be explained by assuming that a smaller and smaller number of interface traps remains filled as the temperature increases.

Border traps cause long-term effects on $V_{th}$ and can be better characterized only with PBTI analyses. The various stress pulses over time are applied with a logarithmic increases in the stress time while the detection of $V_{th}$ is immediately performed after each stress pulse (after 60 ms). The observed decrease of the drain current during the sense phase is converted into the $V_{th}$ shift from the initial measured $I_{DS}$-$V_{GS}$ reference curve. Immediately after the stress phase, the recovery phase is performed similarly to the stress phase. The recovery pulses over time are applied both by short-circuiting the gate and source terminals and by applying a negative voltage on the gate. Immediately after each recovery pulse, the observed increase in the drain current is converted into the $V_{th}$ shift through the previously measured $I_{DS}$-$V_{GS}$ reference curve. From these tests, it has been observed experimentally that applying a positive polarization to the gate, negative charges are captured inside the oxide and this leads to a positive $\Delta V_{th}$. This effect is accelerated by increasing the gate voltage. During the recovery phase, the electrons captured in the stress phase are released from the oxide and this leads a negative $V_{th}$ shift. This effect is accelerated with the reduction of the gate voltage which is also fixed at negative values during the recovery phase. Furthermore, the recovery of a substantial part of $V_{th}$ occurs immediately when the voltage applied to the gate is removed after the stress phase and still the $\Delta V_{th}$ can be completely recovered and this indicates that no permanent damage has been introduced during the stress phase. By implementing PBTI at various temperatures, it has been seen that there is a surprising dependence of the $\Delta V_{th}$ on T during the stress phase. In fact, the $\Delta V_{th}$ becomes smaller by increasing the temperature and a similar phenomenon has been also observed during the recovery phase. It is important even to underline that the $\Delta V_{th}$ for both the stress and recovery phases roughly follows a power law as function of the stress time in the BTI tests as theoretically assumed and that the $\Delta V_{th}$ curves saturate for stress times up to about $10^4$ s. Furthermore, based on the Lelis, McLean and Oldham works, it is possible to affirm that the observed BTI phenomena are due to the directly tunneling of electrons from the channel towards the border traps that penetrate inside the dielectric layer for about 2 Å every decade of time. Therefore, electrons can penetrate inside the oxide to fill the border traps up to about 25 Å after 10000 s due to the effect of the stress applied on the gate of the device and, thus, it is possible to estimate the thickness of the transition layer.

Another important point to highlight from the experiments is that it has been observed that the capture and emission processes of electrons from traps are thermally activated. In practice, the higher the temperature, the shorter the capture and emission constant times and this phenomenon explains the surprising dependence on $\Delta V_{th}$ from temperature during the stress phase. In fact, if a part of the electrons captured during the stress phase are released before the instrumentation detects the $\Delta V_{th}$ they cannot be monitored, thus, the measurement of the threshold voltage shift is less than the real correct value. The phenomenon can be modeled using RD theory and considering Arrhenius' activation method of the individual defects time constants. Subsequently, considering that the $\Delta V_{th}$ in BTI tests is determined by the collective response of a very large number of defects, based on the Pobegen and Grasser model, which considers the energy barriers of traps distributed according to a Gaussian, the $V_{th}$ shift over time can be estimated. In our work, we have been demonstrated that the same $\Delta V_{th}$ function can be simulated with a semi-empirical method proposed by Zafar. The experimetal results obtained by carrying out the PBTI tests and the threshold voltage hysteresys measurements were modeled using the TCAD tool. From the simulations, the profile of the interface traps was extracted by comparing the transfer characteristics simulated and measured at two different $V_{DS}$ with reference to the density of the traps in the upper half of the SiC bandgap. The analyses carried out by the CNR team are based on Scanning Transmission Electron Microscopy (STEM) and sub-nm resolution Electron Energy Loss Spectroscopy (EELS) which allow to highlight the chemical composition of the $SiO_2$/4H-SiC interface region. The experiment showed the profile of the chemical elements highlighting a sub-stoichiometric transition layer of oxycarbide compounds ($SiO_xC_y$) which has a thickness of about 2.5 nm in accordance with what is estimated in our BTI experiments using the method proposed by Lelis.

Finally, we have performed flicker noise measurements on the tested SiC power MOSFETs. We have analysed the experimental results in both the time domain and the frequency domain. In our tests, different measurements were carried out by varying the gate voltage applied on the devices under test from 3 V to 5 V in steps of 400 mV while the drain voltage was set at 50 mV. The spectrum observed in the devices under test as a function of frequency effectively is similar a pink noise and, moreover, increasing the gate bias also increases the PSD level as expected. This last observation confirms that the greater the number of traps that charge and discharge, the higher the spectrum noise signal. However, from the graphs of the spectrum as a function of the frequency is has been obtained that the estimated slope is 0.74 lower than 1 as expected for a pure pink noise signal. By Haartman studies, when the estimated slope is less than 1, as in our case, the traps are not uniformly distributed and their density is greater close the interface rather than going deep in the oxide. Again, the graph of the PSD normalized as a function of the gate voltage overdrive in the log-log scales by setting the frequency at 100 Hz has shown that the curve is very similar to a straight line having a slope equal to about -2. Based on this observation, it is possible to affirm that the main mechanism involved in detecting the flicker noise of the tested SiC power MOSFETs is due to the exchange of charges between the oxide traps and the device channel as theorized in the McWhorter model. From the time domain point of view, it was been observed that the noise signal can be modeled by a AR(3) stochastic process. In fact, by performing the autocorrelations analyses studying the ACF and PACF functions, it is possible to observe that the noise shows a persistence and that the process is ergodic and, still, there is a statistically significant correlation up to the third event after the observed data. In terms of time interval, there is a significant correlation up to events that occurs within about 1 ms (within 0.7-1.0 nm from the interface). Therefore, the very fast events due to the capture and emission of electrons from the oxide traps placed within one nanometer from the interface are mainly involved.

# List of symbols

| | |
|---|---|
| $A$ | area of the oxide surfaces |
| $A^{\#}$ | constant growth rate in the oxidation process |
| *ADC* | Analog to Digital Converter |
| *ApEn* | approximated entropy |
| *APF* | atomic packing factor |
| *AR* | autoregressive stochastic process |
| $\boldsymbol{b}$ | trapping rate parameter |
| $B^{\#}$ | growth rate during the parabolic phase in the oxidation process |
| *BFOM* | figure of merit of Baliga |
| *BJT* | bipolar junction transistor |
| *BTI* | bias temperature instability |
| $BV_{DS}$ | drain-source breakdown voltage of the power MOSFETs |
| $\underline{c}$ | base vector along the z-axis |
| $C$ | thermal conductivity |
| $C^{\#}$ | equilibrium coefficient of concentration of oxygen in the oxide |
| *CCS* | constant current stress |
| $C_{DS}$ | capacitance measured between the drain and source terminals |
| $C_{eq}$ | equivalent capacitance of a MOS |
| $C_{FB}$ | flat band capacitance |
| $C_{GD}$ | capacitance measured between the gate and drain terminals |
| $C_{GS}$ | capacitance measured between the gate and source terminals |
| $C_{iss}$ | input capacitance of power MOSFETs |
| $C_{it}$ | capacitance per unit area due to traps in the interface |
| $c_n$ | electron capture coefficient in the SRH phenomenon |
| $C_{oss}$ | output capacitance of power MOSFETs |
| $C_{ox}$ | gate oxide capacitance per unit area |
| $C_{OX}$ | gate oxide capacitance |

| | |
|---|---|
| $c_p$ | holes capture coefficient in the SRH phenomenon |
| $C_{RSS}$ | inverse capacitance of power MOSFETs |
| $C_s$ | capacitance per unit area in the depletion region of a MOS |
| $C_{Si}$ | carbon antisite defect |
| $C_{Si}V_C$ | carbon antisite vacancies pair defect |
| *CTL* | transition level of the carboxyl defects |
| *CVD* | chemical vapor deposition process |
| *C1* | capacitor 1 present in the figure 4.6.8 |
| *C2* | capacitor 2 present in the figure 4.6.8 |
| *C3* | capacitor 3 present in the figure 4.6.8 |
| *C5* | capacitor 5 present in the figure 4.6.15 |
| *C6* | capacitor 6 present in the figure 4.6.15 |
| $\overline{D}$ | defect diffusivity coefficient |
| $\widehat{D}$ | diffusivity coefficient independent of the temperature of the defects |
| $D_{BD}$ | intrinsic body-drift junction diode of power MOSFETs |
| $D_{CO}$ | diffusion coefficient of CO |
| *DFT* | Density Functional Theory |
| *DIBL* | Drain Induced Barrier Lowering effect in MOSFETs |
| $D_{it}$ | number of traps at the interface for unit of area and energy level |
| $\overline{D_{it}}$ | average density of trapping states |
| $D_n$ | diffusion coefficient of electrons in the substrate |
| *DOS* | Density Of States |
| $D_{O2}$ | diffusion coefficients of $O_2$ |
| *dP* | probability associated with the occurrence of the event in dX |
| *DSP* | digital signal processing |
| *DUT* | device under test |
| $DUT_{noise}$ | noise introduced by the device under test |
| ***E*** | electron energy |
| *E* | energy level |
| *E** | electric field |
| ***E*** | kinetic energy |

| | |
|---|---|
| $E_a$ | activation energy |
| $E_{BD}$ | breakdown electrical field when a junction is reversed polarized |
| $\boldsymbol{E_c}$ | critical electric field |
| $E_c$ | conduction band edge |
| $E_{cn}$ | energy barrier for capturing of electrons in border traps |
| $E_{en}$ | energy barrier for emission of electrons from border traps |
| $E_F$ | Fermi energy level |
| $E_{F,m}$ | Fermi energy level in the metal |
| $E_{F,s}$ | Fermi energy level in the substrate |
| $E_g$ | semiconductor energy bandgap |
| $E_{g0}$ | zero Kelvin bandgap |
| $E_i$ | energy level in the middle of the bandgap |
| $E_i(x)$ | energy level in the middle of the bandgap along the x-axis |
| $e_n$ | electron emission coefficient in the SRH phenomenon |
| $E_{OX}$ | electric field in the oxide |
| $e_p$ | hole emission coefficient in the SRH phenomenon |
| *EPR* | electron paramagnetic resonance |
| *E-R* | metric entropy algorithm of Eckmann and Ruelle |
| $E_s$ | electric field in the interface |
| *ESR* | electron spin resonance |
| $E_t$ | energy level of traps |
| $E_v$ | valence band edge |
| $E_{VTH,ep}$ | energy level within the SiC bandgap to establish the $V_{th}$ shift |
| $E_0$ | reference level of the energy of the traps in the oxide |
| $f$ | AC signal frequency |
| $f_A(E_t)$ | probability of finding a hole in an energy level $E_t$ of a trap |
| $f_D(E_t)$ | probability to find an electron in an energy level $E_t$ of a trap |
| *FBSOA* | forward bias safe operating area of power MOSFETs |
| *FFT* | Fast Fourier Transform algorithm |
| $f(E)$ | probability of finding an electron in an established energy level E |
| $F_{metal}$ | distribution of Fermi-Dirac in metal |

| | |
|---|---|
| *FOM* | figure of merit |
| *G* | concentration of the chemical specie |
| $g_A$ | acceptor number of ground degenerate states |
| *GaAs* | gallium arsenide semiconductor |
| *GaN* | gallium nitride semiconductor |
| *G(E)* | density of states |
| $g(E_{cn}, E_{en})$ | charged trap density of the activation energies |
| $g_d$ | conductance of a MOSFET |
| $g_{d0}$ | conductance of a MOSFET due only to $R_{ch}$ |
| $g_{fs}$ | transconductance of MOSFETs |
| $g_D$ | donor number of ground degenerate states |
| *GGA* | generalized gradient approximation functional |
| *GIDL* | Gate Induced Drain Current effect in MOSFETs |
| *G-R* | generation and recombination phenomena in a semiconductor |
| *h* | Plank constant |
| *H* | entropy of a stochastic process |
| $\widehat{H}$ | Hamiltonian associated with a particle |
| *HPC* | hexagonal close-packed |
| *i* | small signal current |
| *I* | current |
| $I_{bc}$ | interstitial defect centered in the bond |
| $I_{DS}$ | drain-source current |
| $I_{DSmax}$ | maximum drain-source current flowing in a power MOSFET |
| $I_{DSsat}$ | drain saturation current in the MOSFET |
| $I_{FN}$ | tunneling current Fowler-Nordheim |
| $I_G$ | gate displacement current in the power MOSFETs |
| *IGBT* | insulated gate bipolar transistor |
| $I_{TC}$ | interstitial carbon defect |
| $I_{TSi}$ | interstitial silicon defect |
| $i_1$ | current that flows in the circuit shown in figure 4.6.10b |
| $i_2$ | current that flows in the circuit shown in figure 4.6.10b |

| | |
|---|---|
| $i_3$ | current that flows in the circuit shown in figure 4.6.10b |
| $K$ | Boltzmann constant |
| $K^{\#}$ | constant associated with the PSD of a flicker noise |
| $\vec{k}$ | wave vector associated with a wavefunction |
| $\hat{k}$ | direction of propagation of the vector $\vec{\mathrm{k}}$ |
| $k_f$ | forward constant growth rate of the reaction |
| $K_r$ | constant growth rate of the reverse reaction |
| $K_1$ | Kolmogorov's metric entropy |
| $\boldsymbol{J}$ | flow of defects |
| $J$ | current density |
| $J_0$ | zero-time current density |
| *JFET* | junction gate field effect transistor |
| $J_{FN}$ | current density Fowler-Nordheim tunneling |
| $J_t$ | tunneling current density |
| *JTE* | Jahn-Teller effect |
| $\boldsymbol{L}$ | length of the MOSFET channel |
| $L$ | lag operator |
| $L_d$ | inductance of the wire of the package connecting the drain |
| $L_D$ | Debye length |
| *LDA* | local density functional |
| *LDMOS* | light doped metal oxide semiconductor |
| *LF* | low frequency signal |
| *LKI* | Kirchhoff's law for currents |
| *LKV* | Kirchhoff's law for voltages |
| $L_g$ | inductance of the wire of the package connecting the gate |
| *LNA* | low-noise amplifier |
| $LNA_{background\ noise}$ | input noise of LNA |
| $L_s$ | inductance of the wire of the package connecting the source |
| $m$ | mass of free electron |
| $m^*$ | effective mass of electrons |
| $m^{\#}$ | integer number in the E-R algorithm |

| | |
|---|---|
| *M* | network shown in the figure 4.6.16b |
| *M1* | network shown in the figure 4.6.10b |
| *M2* | network shown in the figure 4.6.10b |
| *MA* | stochastic moving average process |
| *MOS* | metal oxide semiconductor |
| *MOSFET* | metal oxide semiconductor field effect transistor |
| *n* | electron concentration in the substrate |
| *n** | average rate of increase of the noise pulse |
| $\dot{n}$ | discrete number |
| $n^+$ | electron concentration in the deeply doped layer of the substrate |
| ***N*** | carrier density in the inversion or accumulation layer |
| $N^{\#}$ | number of oxygen molecules in a unit volume present in the oxide |
| *N** | number of free electrons available for conduction |
| $N_A$ | concentration of acceptors in the substrate |
| $N_{AB}$ | concentration of acceptors in the substrate |
| *NBTI* | negative bias temperature instability |
| $N_{bulk}$ | density of states in the substrate |
| $N_c$ | number of states available for electrons in the conduction band |
| $N_D$ | concentration of donors in the substrate |
| $N_{epy}$ | concentration of the doping in the epitaxial layer |
| *N(E, ΔE)* | number of energy levels between E and E+ΔE |
| $n_i$ | intrinsic concentration of carriers in the substrate |
| *NIOTs* | near interface oxide traps |
| $N_{it}$ | density of traps at the interface per unit of potential |
| $N_{gate}$ | doping concentration of the polysilicon |
| $N_{metal}$ | density of states in the metal |
| $n_s$ | electron concentration in the oxide-semiconductor interface |
| $N_{sub}$ | substrate doping concentration |
| $n_t$ | number of states filled by electrons in the forbidden bandgap |
| $N_t$ | number of traps |
| $N_v$ | number of states available for holes in the valence band |

| | |
|---|---|
| *OLS* | ordinary least squares technique |
| *OP AMP* | operational amplifier |
| *OP AMP 01* | operational amplifier 1 present in the figure 4.6.8 |
| *OP AMP 02* | operational amplifier 2 present in the figure 4.6.8 |
| *OP AMP 03* | operational amplifier 3 present in the figure 4.6.8 |
| *OP AMP 04* | operational amplifier 4 present in the figure 4.6.8 |
| *OP AMP 05* | operational amplifier 5 present in the figure 4.6.8 |
| $p$ | hole concentration in the substrate |
| $P$ | power function |
| *PBTI* | positive bias temperature instability |
| *PDF* | probability density function |
| *POA* | post-oxidation annealing processes |
| $p_s$ | hole concentration in the oxide-semiconductor interface |
| *PSD* | power spectral density |
| *PSG* | phosphosilicate glass |
| $p_t$ | number of states occupied by holes in the forbidden bandgap |
| $P_t$ | tunneling probability |
| $P_1$ | button 1 present in the circuit shown in figure 4.6.8 |
| $P_2$ | button 2 present in the circuit shown in figure 4.6.8 |
| $q$ | elementary charge |
| $Q$ | charge density |
| $Q_{BD}$ | charge to breakdown |
| $Q_c$ | charge density in the interface in a regime of strong inversion |
| $Q_{dmax}$ | maximum charge density during the depletion regime in a MOS |
| $Q_G$ | charge at the metal-oxide interface |
| $Q_{it}$ | charge density of the interface |
| $Q_{OX}$ | charge density in the oxide |
| $Q_s$ | charge per unit area in the oxide-substrate interface |
| $r$ | real number in the E-R algorithm |
| $\boldsymbol{r}$ | correlation parameter used to calculate the energy activation energy |
| $\vec{r}$ | direction of the wave function |

| | |
|---|---|
| $R$ | electrical resistance |
| $R_{acc}$ | resistance of the accumulation layer in VDMOS power MOSFETs |
| *RBSOA* | reverse bias safe operating area of power MOSFETs |
| $R_{ch}$ | resistance of the channel of the MOSFETs |
| *RD* | reaction diffusion theory |
| $R_{drift}$ | resistance of the drift layer in power MOSFETs |
| $R_{DSON}$ | MOSFET source-drain resistance measured during the on state |
| *RESURF* | reduced surface field technology in power MOSFETs |
| $R_g$ | resistance of the gate in power MOSFETs |
| $R_{JFET}$ | resistance of the JFET component in VDMOS power MOSFETs |
| $R_s$ | resistance of the source well |
| $R_{sub}$ | resistance of the epitaxial layer |
| $R_{thJC}$ | junction to case thermal resistance |
| $R_{wcml}$ | resistance due to the bond wire and metallization in power MOSFETs |
| *R1* | resistor 1 present in the figure 4.6.8 |
| *R2* | resistor 2 present in the figure 4.6.8 |
| *R6* | resistor 6 present in the figure 4.6.19 |
| *s* | generic string composed of elements of an alphabet |
| *S* | entropy |
| *S(f)* | spectrum of signals |
| *SJ* | super junction technology for power MOSFETs |
| *Si* | silicon semiconductor |
| $S_I$ | spectrum of the current signal |
| $Si_C$ | silicon antisite defect |
| *SiC* | silicon carbide semiconductor |
| $Si_CC_{Si}$ | antisite pairs defect |
| *SNR* | Signal to Noise Ratio of LNA amplifiers |
| *SOA* | safe operating area of the power MOSFETs |
| *SRH* | capture and emission processes of Shockley-Read-Hall of the carriers |
| $S_V$ | spectrum of the voltage signal |
| *t* | time |

| | |
|---|---|
| $T$ | temperature |
| $\boldsymbol{T}$ | period of time |
| $TBOX$ | thickness at the bottom of the gate oxide of Trench structures |
| $T_C$ | package temperature |
| $TDDS$ | time-dependent defect spectroscopy |
| $T_{Jmax}$ | maximum junction temperature allowed in power MOSFETs |
| $t_{ON}$ | period of time in the on state of the power MOSFETs |
| $t_{OX}$ | oxide thickness |
| $t_{poly}$ | thickness of the depletion layer in the gate polysilicon |
| $U$ | energy barrier level |
| $\boldsymbol{U}$ | potential energy of electrons |
| $UMOS$ | U-shape metal oxide semiconductor |
| $v$ | electron velocity |
| $\boldsymbol{v}$ | small voltage signal |
| $V$ | electrical potential |
| $V_c$ | voltage drop in the strong inversion layer |
| $V_C$ | carbon vacancy defect |
| $V_CV_{Si}$ | divacancy defect in SiC crystal |
| $V_{C1}$ | voltage present in the terminals of C1 as shown in figure 4.6.10b |
| $V_{C2}$ | voltage present in the terminals of C2 as shown in figure 4.6.10b |
| $VDMOS$ | vertical diffused metal oxide semiconductor |
| $V_{DS}$ | drain-source voltage |
| $V_{DSsat}$ | drain-source saturation voltage |
| $V_{FB}$ | flat band voltage |
| $V_G$ | gate potential |
| $V_{GS}$ | gate-source voltage |
| $V_{it}$ | gate voltage that compensates for the charge in the interface traps |
| $VMOS$ | vertical metal oxide semiconductor |
| $V_{OX}$ | voltage drop in the oxide |
| $V_Q$ | voltage drop due to traps in the oxide |
| $v_s$ | electron velocity in saturation regime |

| | |
|---|---|
| $V_{SB}$ | potential of source-body junction |
| $V_{Si}$ | silicon vacancy defect |
| $V_T$ | thermal voltage |
| $v_{th}$ | thermal velocity of the carriers in the substrate |
| $V_{th}$ | threshold voltage of the real MOS structure |
| $V_{th}^{down}$ | $V_{th}$ measured in the descending phase of hysteresis test |
| $V_{th}^{up}$ | $V_{th}$ measured in the ascending phase of hysteresis test |
| $V_{th0}$ | threshold voltage of the ideal MOS structure |
| $\boldsymbol{W}$ | perimeter of the MOSFET |
| *WBG* | wide bandgap semiconductor |
| *WKB* | Wentzel-Kramers-Brillouin tunneling theory |
| $X$ | thickness of the oxide grown |
| $x$ | random variable |
| $x_d$ | depth of the depleted region in a MOS |
| $x_{dmax}$ | maximum depth of the depleted region in a MOS |
| $X_S$ | energy difference between vacuum and $E_c$ |
| $X_{SiC}$ | electron affinity of the SiC substrate |
| $z$ | vectors of E-R algorithm |
| $Z_{thJC}$ | junction-case thermal impedance |
| $\alpha$ | experimental coefficient of the gate current power law of Zafar |
| $\alpha^*$ | inverse of the time constant of the captured electrons |
| $\alpha^\circ$ | scattering coefficient of the unified model |
| $\alpha^\#$ | fractal shot noise coefficient |
| $\alpha^+$ | coefficient of the correlated number-mobility fluctuation model |
| $\alpha_H$ | dimensionless Hooge's parameter in the mobility fluctuation model |
| $\beta^*$ | inverse of the time constant of the released electrons |
| $\beta^\#$ | coefficient associated to the PSD of a flicker noise |
| $\gamma$ | body effect coefficient |
| $\gamma$ | emperical parameters introduced in the Zafar model |
| $\gamma^*$ | coefficient associated with flicker noise |
| $\delta$ | depth of the inversion layer |

| | |
|---|---|
| $\boldsymbol{\delta}$ | duty cycle |
| $\Delta E$ | interval of energy |
| $\Delta T_{max}$ | maximum increases in the allowed junction temperature |
| $\Delta V_{th}$ | $V_{th}$ shift |
| $\Delta V_{th}^{\max}$ | maximum shift of the $V_{th}$ |
| $\Delta V_{TH}^{BTI}$ | amplitude of the BTI drift during the switching process |
| $\varepsilon_{OX}$ | permittivity of the oxide |
| $\varepsilon_r$ | relative permittivity |
| $\varepsilon_s$ | substrate permittivity |
| $\varepsilon_{Si}$ | silicon permittivity |
| $\varepsilon_{SiC}$ | silicon carbide permittivity |
| $\varepsilon_{sp}$ | polysilicon layer permittivity |
| $\eta_1$ | Paulsen coefficient used to derive tunnelling times |
| $\eta_2$ | Paulsen coefficient used to derive tunnelling times |
| $\lambda$ | wavelength associated with a wavefunction |
| $\lambda^*$ | waveform length attenuation parameter |
| $\lambda^{\#}$ | tunneling length attenuation parameter |
| $\mu$ | carriers mobility |
| $\boldsymbol{\mu_c}$ | mean value of the capture activation energies of the border traps |
| $\boldsymbol{\mu_e}$ | mean value of the emission activation energies of the border traps |
| $\mu_{eff}$ | effective mobility of carriers in the MOSFET channel |
| $\mu_{\mathrm{eff}\perp}$ | mobility of the carriers due to the transverse electric field |
| $\mu_{\mathrm{eff}\parallel}$ | mobility of the carriers due to the longitudinal electric field |
| $\mu_n$ | electron mobility in the substrate |
| $\mu_{n0}$ | electron mobility in the channel without the transverse electric field |
| $\mu_p$ | mobility of holes in the substrate |
| $\mu_{sat}$ | carrier mobility in the saturation regime |
| $v$ | frequency associated with a wavefunction |
| $\boldsymbol{\rho}$ | resistivity of the substrate surface |
| $\rho$ | autocorrelation values |
| $\varrho$ | charge density in the semiconductor |

| | |
|---|---|
| $\boldsymbol{\sigma^2}$ | variance of a stochastic process |
| $\boldsymbol{\sigma_c}$ | standard deviation of the capture activation energies of the traps |
| $\boldsymbol{\sigma_e}$ | standard deviation of the emission activation energies of the traps |
| $\sigma_n$ | cross section of electrons |
| $\sigma_p$ | cross section of holes |
| $\tau$ | time constant of a stochastic process G-R |
| $\tau$ | time needed to grow an initial oxide |
| $\tau_c$ | time constant of the electrons captured in the traps at the interface |
| $\tau_{cn}$ | time constant of the electrons captured in border raps |
| $\tau_{cn0}$ | time constant coefficient of the electrons captured in border raps |
| $\tau_e$ | time constant of the electrons emitted in the traps at the interface |
| $\tau_{en}$ | time constant of the electrons emitted in border traps |
| $\tau_{en0}$ | time constant coefficient of the electrons emitted in border traps |
| $\tau_h$ | time constant of the holes emitted in the traps at the interface |
| $\tau_{it}$ | time constant of the electron in the trap at the interface |
| $\tau_0$ | emperical parameters introduced in the Zafar model |
| $\theta$ | linear coefficient of a stochastic process MA |
| $\varphi_B$ | substrate Fermi potential |
| $\phi_F$ | inversion potential in a MOS |
| $\phi_h$ | voltage difference between $V_{OX}$ and $qE_c$ in the substrate |
| $\phi_m$ | metal work function |
| $\phi_{ms}$ | metal-semiconductor work function |
| $\phi_s$ | potential in the substrate surface |
| $\boldsymbol{\phi_s}$ | semiconductor work function |
| $\phi(x_d)$ | potential at the edge of the depleted region |
| $\psi_s$ | bending of the energy bands at the oxide-semiconductor interface |
| $\Psi_{metal}$ | electron wavefunction in the metal |
| $\Psi_{bulk}$ | electron wavefunction in the substrate |
| $\psi(\vec{r}, t)$ | wavefunction |
| $\omega$ | angular frequency associated with a wavefunction or signal |
| $\vartheta$ | number of vectors in E-R algorithm |

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